

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus

DEVICE	A OUTPUT	B OUTPUT	LOGIC
SN74ALS651A, 'AS651	3-State	3-State	Inverting
SN54ALS652, SN74ALS652A, 'AS652	3-State	3-State	True
'ALS653	Open Collector	3-State	Inverting
SN74ALS654	Open Collector	3-State	True

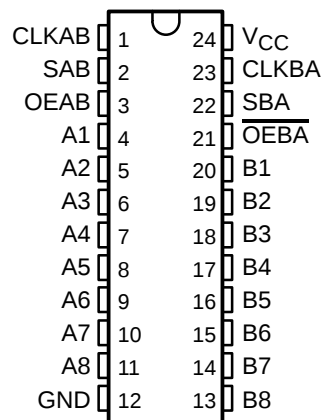
description

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers

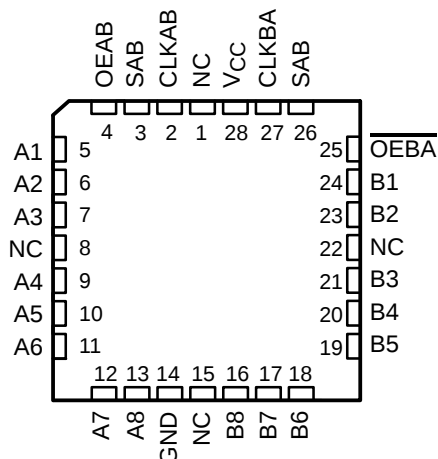
Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The -1 versions of the SN74ALS651A and SN74ALS652A are identical to the standard versions except that the recommended maximum I_{OL} for the -1 versions is increased to 48 mA. There are no -1 versions of the SN54ALS652, SN54ALS653, SN74ALS653, and SN74ALS654.

SN54ALS', SN54AS' ... JT PACKAGE
SN74ALS', SN74AS' ... DW OR NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' ... FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

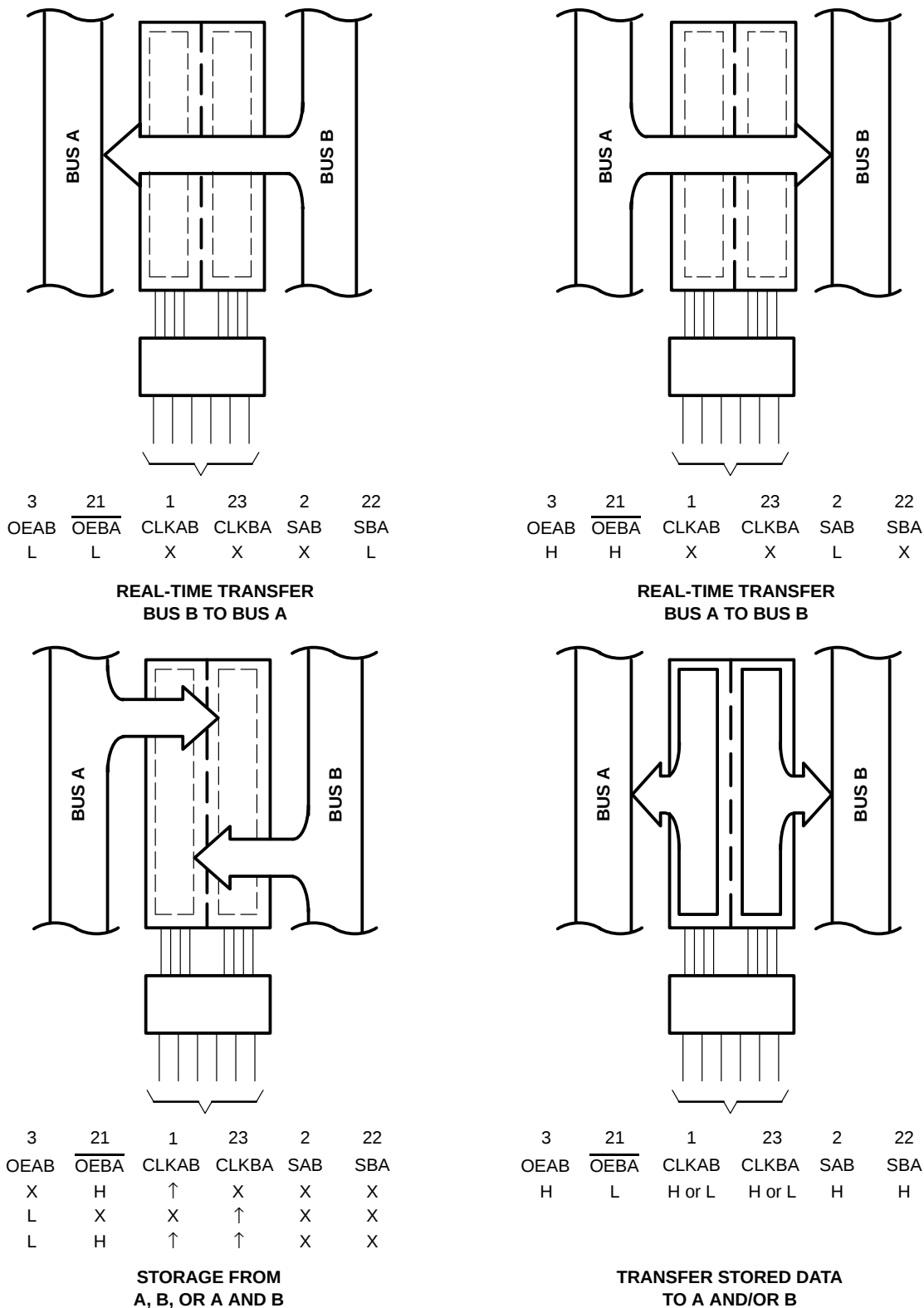
ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – NT	Tube	SN74ALS651ANT	SN74ALS651ANT
			SN74ALS652ANT	SN74ALS652ANT
			SN74ALS653NT	SN74ALS653NT
			SN74ALS654NT	SN74ALS654NT
			SN74AS651NT	SN74AS651NT
			SN74AS652NT	SN74AS652NT
	SOIC – DW	Tube	SN74ALS651ADW	ALS651A
		Tape and reel	SN74ALS651ADWR	
		Tube	SN74ALS652ADW	ALS652A
		Tape and reel	SN74ALS652ADWR	
		Tube	SN74ALS653DW	ALS653
		Tape and reel	SN74ALS653DWR	
		Tube	SN74ALS654DW	ALS654
		Tape and reel	SN74ALS654DWR	
		Tube	SN74AS651DW	AS651
		Tape and reel	SN74AS651DWR	
		Tube	SN74AS652DW	AS652
		Tape and reel	SN74AS652DWR	
–55°C to 125°C	CDIP – JT	Tube	SNJ54ALS652JT	SNJ54ALS652JT
			SNJ54ALS653JT	SNJ54ALS653JT
			SNJ54AS651JT	SNJ54AS651JT
			SNJ54AS652JT	SNJ54AS652JT
	LCCC – FK	Tube	SNJ54ALS652FK	SNJ54ALS652FK
			SNJ54ALS653FK	SNJ54ALS653FK
			SNJ54AS651FK	SNJ54AS651FK
			SNJ54AS652FK	SNJ54AS652FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000



Pin numbers shown are for the DW, JT, and NT packages.

Figure 1. Bus-Management Functions

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

Function Tables

SN54ALS653, SN54AS651,
SN74ALS651A, SN74ALS653, SN74AS651

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified [‡]	Store A, hold B
H	H	↑	↑	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	↑	↑	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

[†] The data output functions can be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

[‡] Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered to load both registers.

SN54ALS652, SN54AS652,
SN74ALS652A, SN74ALS654, SN74AS652

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified [‡]	Store A, hold B
H	H	↑	↑	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	↑	↑	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions can be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

[‡] Select control = L: clocks can occur simultaneously.

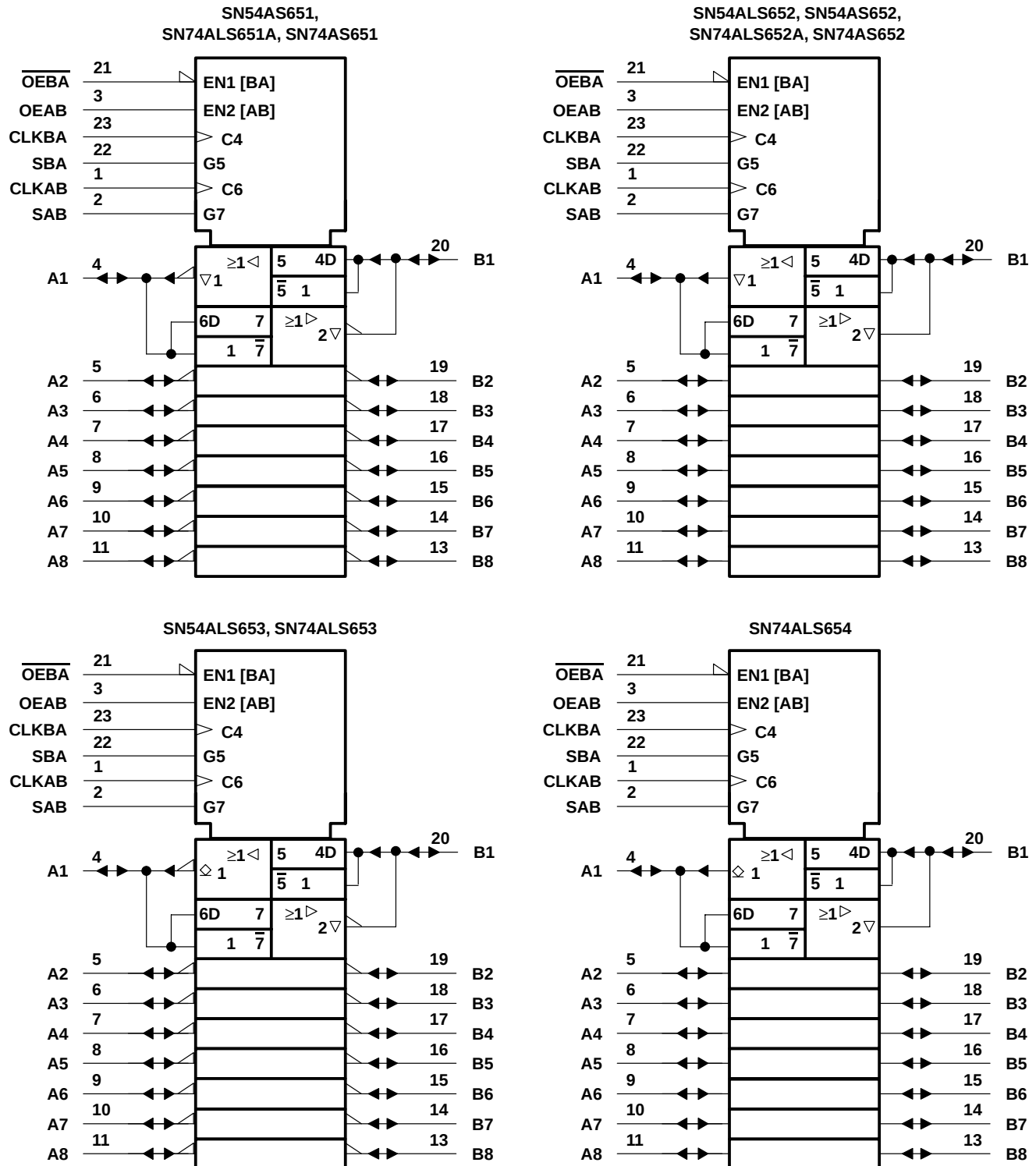
Select control = H: clocks must be staggered to load both registers.



SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

logic symbols†

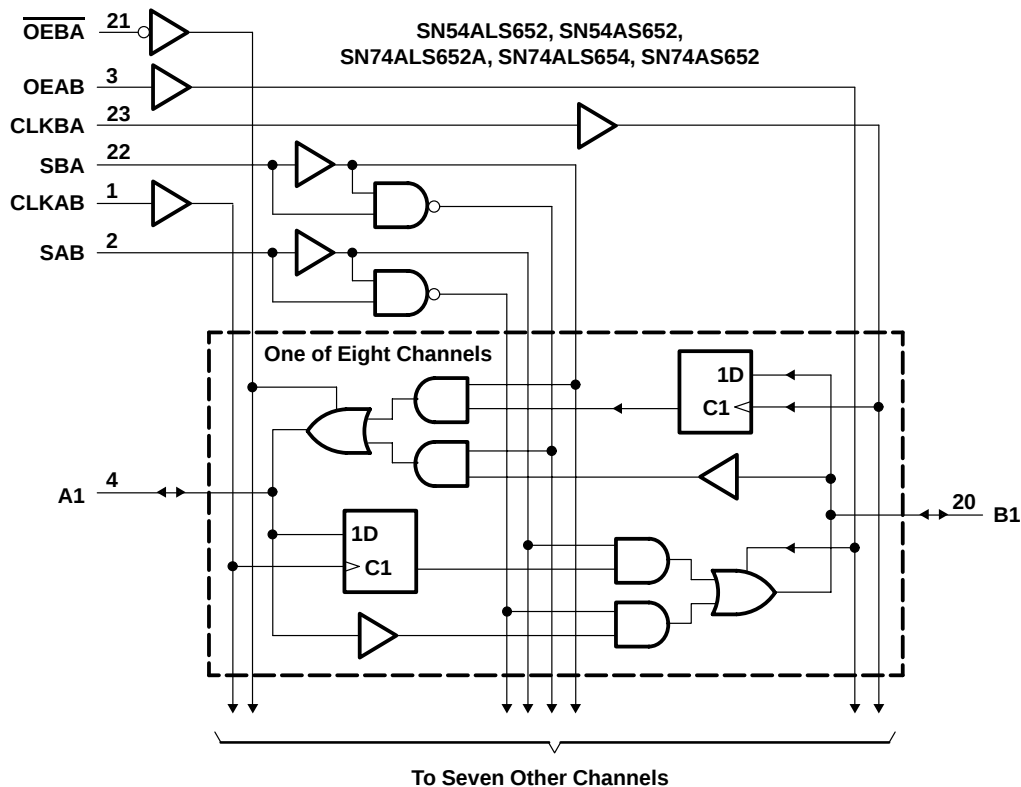
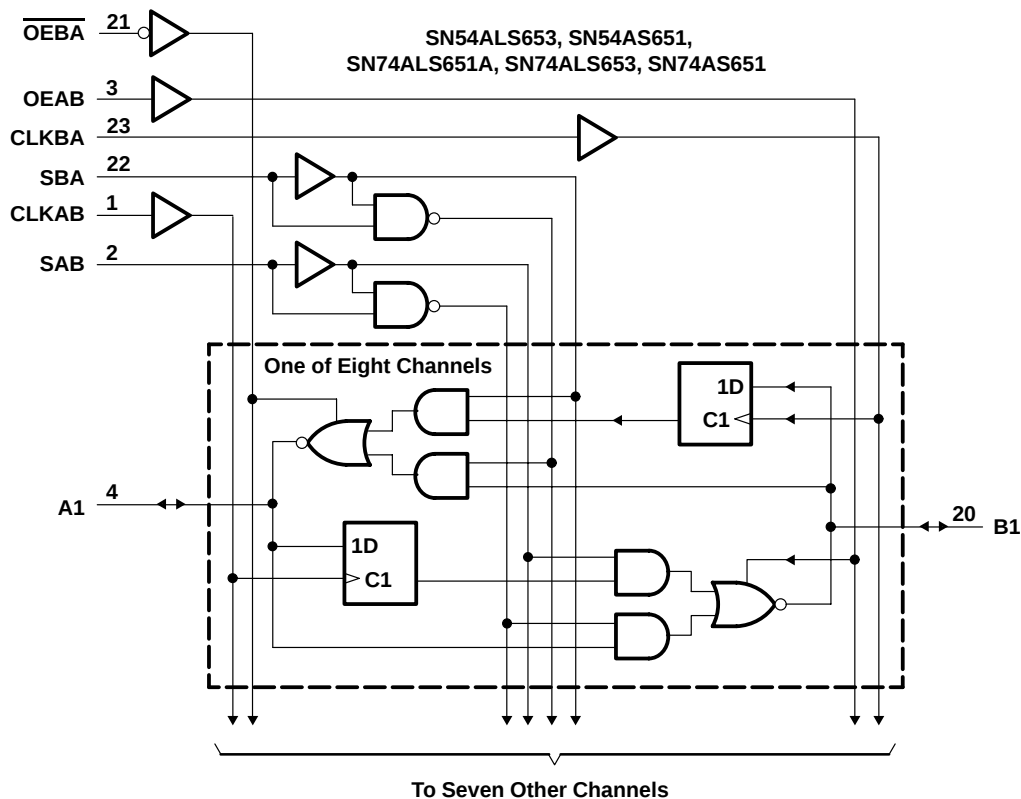


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

logic diagrams (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I : Control inputs	–0.5 V to 7 V
I/O ports	–0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	46°C/W
NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		SN74ALS651A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			24	mA
				48 [‡]	
f_{clock}	Clock frequency	0		40	MHz
t_w	Pulse duration	CLKBA or CLKAB high		12.5	ns
		CLKBA or CLKAB low		12.5	
t_{su}	Setup time before CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		10	ns
t_h	Hold time after CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		0	ns
T_A	Operating free-air temperature	0		70	°C

[‡] Applies only to the SN74ALS651A-1 and only if V_{CC} is maintained between 4.75 V and 5.25 V

recommended operating conditions

		SN54ALS652			SN74ALS652A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
							48 [‡]	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration	CLKBA or CLKAB high		14.5	12.5			ns
		CLKBA or CLKAB low		14.5	12.5			
t_{su}	Setup time before CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		15	10			ns
t_h	Hold time after CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		5	0			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

[‡] Applies only to the SN74ALS652A-1 and only if V_{CC} is maintained between 4.75 V and 5.25 V



**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS651A		UNIT
				MIN	TYP†	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2		V
		V _{CC} = 4.5 V	I _{OH} = −3 mA	2.4	3.2	
			I _{OH} = −15 mA	2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	V
			I _{OL} = 24 mA	0.35	0.5	
		V _{CC} = 4.75 V, I _{OL} = 48 mA (-1 versions)		0.35	0.5	
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V	0.1		mA	
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V	0.1			
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V	20		μA	
	A or B ports‡		20			
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V	−0.2		mA	
	A or B ports‡		−0.2			
I _O [§]		V _{CC} = 5.5 V, V _O = 2.25 V	−30	−112	mA	
I _{CC}		V _{CC} = 5.5 V	Outputs high	42	68	mA
			Outputs low	52	82	
			Outputs disabled	52	82	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS652			SN74ALS652A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA	−1.2			−1.2			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA	V _{CC} − 2			V _{CC} − 2			V
		V _{CC} = 4.5 V	I _{OH} = −3 mA		2.4	3.2	2.4	3.2	
			I _{OH} = −12 mA		2				
			I _{OH} = −15 mA				2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA		0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA				0.35	0.5	
		V _{CC} = 4.75 V, I _{OL} = 48 mA (-1 versions)					0.35		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V	0.1			0.1			
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA
	A or B ports‡		20			20			
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V	−0.2			−0.2			mA
	A or B ports‡		−0.2			−0.2			
I _O [§]		V _{CC} = 5.5 V, V _O = 2.25 V	−20	−112		−30	−112		mA
I _{CC}		V _{CC} = 5.5 V	Outputs high		47	76	47	76	mA
			Outputs low		55	88	55	88	
			Outputs disabled		55	88	55	88	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS651A		
			MIN	MAX	
f _{max}			40		MHz
t _{PLH}	CLKBA or CLKAB	A or B	8	32	ns
t _{PHL}			5	17	
t _{PLH}	A or B	B or A	2	18	ns
t _{PHL}			2	10	
t _{PLH}	SBA or SAB‡ (with A or B high)	A or B	8	38	ns
t _{PHL}			6	21	
t _{PLH}	SBA or SAB‡ (with A or B low)	A or B	8	25	ns
t _{PHL}			7	21	
t _{PZH}	$\overline{\text{OEBA}}$	A	3	20	ns
t _{PZL}			5	18	
t _{PHZ}	$\overline{\text{OEBA}}$	A	2	9	ns
t _{PLZ}			3	12	
t _{PZH}	OEAB	B	3	22	ns
t _{PZL}			6	21	
t _{PHZ}	OEAB	B	2	12	ns
t _{PLZ}			2	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS652		SN74ALS652A		
			MIN	MAX	MIN	MAX	
f _{max}			35		40		MHz
t _{PLH}	CLKBA or CLKAB	A or B	10	35	8	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A or B	B or A	5	20	4	18	ns
t _{PHL}			3	15	3	12	
t _{PLH}	SBA or SAB [‡] (with A or B high)	A or B	15	40	8	35	ns
t _{PHL}			6	23	6	20	
t _{PLH}	SBA or SAB [‡] (with A or B low)	A or B	8	30	8	25	ns
t _{PHL}			5	24	5	20	
t _{PZH}	$\overline{\text{OEBA}}$	A	3	20	3	17	ns
t _{PZL}			5	22	5	18	
t _{PHZ}	$\overline{\text{OEBA}}$	A	1	12	1	10	ns
t _{PLZ}			2	20	2	16	
t _{PZH}	OEAB	B	8	25	3	22	ns
t _{PZL}			6	21	5	18	
t _{PHZ}	OEAB	B	1	12	1	10	ns
t _{PLZ}			2	21	2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I : Control inputs	–0.5 V to 7 V
I/O ports	–0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	46°C/W
NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		SN54ALS653			SN74ALS653			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage	A ports		5.5	5.5			V
I_{OH}	High-level output current	B ports		–12	–15			mA
I_{OL}	Low-level output current			12	24			mA
f_{clock}	Clock frequency	0		25	0		35	MHz
t_w	Pulse duration	CLKBA or CLKAB high		20	14.5			ns
		CLKBA or CLKAB low		20	14.5			
t_{su}	Setup time before CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		15	10			ns
t_h	Hold time after CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		5	0			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

recommended operating conditions

		SN74ALS654			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage	A ports		5.5	V
I_{OH}	High-level output current	B ports		–15	mA
I_{OL}	Low-level output current			24	mA
f_{clock}	Clock frequency	0		35	MHz
t_w	Pulse duration	CLKBA or CLKAB high		14.5	ns
		CLKBA or CLKAB low		14.5	
t_{su}	Setup time before CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		10	ns
t_h	Hold time after CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B		0	ns
T_A	Operating free-air temperature	0		70	°C



**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS653			SN74ALS653			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	B ports	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2			V _{CC} − 2			V
		V _{CC} = 4.5 V	I _{OH} = −3 mA	2.4	3.2	2.4	3.2			
			I _{OH} = −12 mA	2						
			I _{OH} = −15 mA			2				
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V		
			I _{OL} = 24 mA			0.35	0.5			
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA	
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V	0.1			0.1				
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA	
	A or B ports‡		20			20				
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V	−0.2			−0.2			mA	
	A or B ports‡		−0.2			−0.2				
I _{OH}	A ports	V _{CC} = 4.5 V, V _{OH} = 5.5 V	0.1			0.1			mA	
I _O [§]	B ports	V _{CC} = 5.5 V, V _O = 2.25 V	−20	−112	−30	−112	mA			
I _{CC}		V _{CC} = 5.5 V	Outputs high	47	76	47	76	mA		
			Outputs low	55	88	55	88			
			Outputs disabled	55	88	55	88			

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS654			UNIT
				MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				-1.2	V
V_{OH}	B ports	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			V
		$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.2		
			$I_{OH} = -15\text{ mA}$	2			
V_{OL}		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$		0.25	0.4	V
			$I_{OL} = 24\text{ mA}$		0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$				0.1	mA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$				0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$				20	μA
	A or B ports [‡]					20	
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$				-0.2	mA
	A or B ports [‡]					-0.2	
I_{OH}	A ports	$V_{CC} = 4.5\text{ V}$, $V_{OH} = 5.5\text{ V}$				0.1	mA
$I_O^{\S}$	B ports	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$		-30		-112	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$	Outputs high		47	76	mA
			Outputs low		55	88	
			Outputs disabled		55	88	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T _A = MIN to MAX [†]				UNIT
			SN54ALS653		SN74ALS653		
			MIN	MAX	MIN	MAX	
f _{max}			25		35		MHz
t _{PLH}	CLKBA	A	16	71	16	64	ns
t _{PHL}			6	24	6	22	
t _{PLH}	CLKAB	B	10	35	10	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A	B	5	20	5	18	ns
t _{PHL}			1.5	18	2	15	
t _{PLH}	B	A	8	63	12	56	ns
t _{PHL}			2	18	2	15	
t _{PLH}	SBA [‡] (with B high)	A	12	68	19	62	ns
t _{PHL}			5	27	5	25	
t _{PLH}	SBA [‡] (with B low)	A	12	68	19	62	ns
t _{PHL}			5	27	5	25	
t _{PLH}	SAB [‡] (with A high)	B	8	30	15	35	ns
t _{PHL}			6	25	6	22	
t _{PLH}	SAB [‡] (with A low)	B	12	40	8	25	ns
t _{PHL}			6	25	6	22	
t _{PLH}	$\overline{\text{OEBA}}$	A	6	35	6	30	ns
t _{PHL}			6	27	6	24	
t _{PZH}	OEAB	B	7	25	8	22	ns
t _{PZL}			6	25	6	22	
t _{PHZ}	OEAB	B	1	16	1	14	ns
t _{PLZ}			2	21	2	16	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T _A = MIN to MAX [†]		UNIT
			SN74ALS654		
			MIN	MAX	
f _{max}			35		MHz
t _{PLH}	CLKBA	A	16	64	ns
t _{PHL}			6	22	
t _{PLH}	CLKAB	B	10	30	ns
t _{PHL}			5	17	
t _{PLH}	A	B	5	18	ns
t _{PHL}			2	15	
t _{PLH}	B	A	12	56	ns
t _{PHL}			2	21	
t _{PLH}	SBA [‡] (with B low)	A	19	62	ns
t _{PHL}			5	25	
t _{PLH}	SBA [‡] (with B high)	A	19	62	ns
t _{PHL}			5	25	
t _{PLH}	SAB [‡] (with A low)	B	15	35	ns
t _{PHL}			6	22	
t _{PLH}	SAB [‡] (with A high)	B	8	25	ns
t _{PHL}			6	22	
t _{PLH}	$\overline{\text{OEBA}}$	A	6	30	ns
t _{PHL}			6	24	
t _{PZH}	OEAB	B	6	22	ns
t _{PZL}			6	22	
t _{PHZ}	OEAB	B	1	14	ns
t _{PLZ}			2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I : Control inputs	–0.5 V to 7 V
I/O ports	–0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	46°C/W
NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				–12			–15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0*		75*	0		90	MHz
t_w	Pulse duration	CLKBA or CLKAB high	6*			5			ns
		CLKBA or CLKAB low	7*			6			
t_{su}	Setup time before CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B	7*			6			ns
t_h	Hold time after CLKAB $\uparrow$ or CLKBA	A or B	0*			0			ns
T_A	Operating free-air temperature		–55		125	0		70	°C

* On products compliant to MIL-PRF-38535, this parameter is based on characterized data but is not production tested.



SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS651 SN54AS652		SN74AS651 SN74AS652		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2		−1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA		V _{CC} − 2		V _{CC} − 2		V
		V _{CC} = 4.5 V	I _{OH} = −3 mA	2.4	3.2	2.4	3.2	
			I _{OH} = −12 mA	2				
			I _{OH} = −15 mA			2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 32 mA	0.25	0.5			V
			I _{OL} = 48 mA			0.35	0.5	
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA	
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V	0.1		0.1			
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA	
	A or B ports‡		70		70			
I _{IL}	Control input	V _{CC} = 5.5 V, V _I = 0.4 V	−0.5		−0.5		mA	
	A or B ports‡		−0.75		−0.75			
I _O [§]		V _{CC} = 5.5 V, V _O = 2.25 V	−30	−112	−30	−112	mA	
I _{CC}	‘AS651	V _{CC} = 5.5 V	Outputs high	110	185	110	185	mA
			Outputs low	120	195	120	195	
			Outputs disabled	130	195	130	195	
	‘AS652	V _{CC} = 5.5 V	Outputs high	120	195	120	195	
			Outputs low	130	211	130	211	
			Outputs disabled	130	211	130	211	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f _{max}			75*		90		MHz
t _{PLH}	CLKBA or CLKAB	A or B	2	11	2	8.5	ns
t _{PHL}			2	10	2	9	
t _{PLH}	A or B	B or A	2	12	2	8	ns
t _{PHL}			1	8	1	7	
t _{PLH}	SBA or SAB‡	A or B	2	15	2	11	ns
t _{PHL}			2	11	2	9	
t _{PZH}	$\overline{\text{OEBA}}$	A	2	11	2	10	ns
t _{PZL}			3	18	3	16	
t _{PHZ}	$\overline{\text{OEBA}}$	A	2	10	2	9	ns
t _{PLZ}			2	10	2	9	
t _{PZH}	OEAB	B	3	12	3	11	ns
t _{PZL}			3	20	3	16	
t _{PHZ}	OEAB	B	2	11	2	10	ns
t _{PLZ}			2	12	2	11	

* On products compliant to MIL-PRF-38535, this parameter is based on characterized data but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V TO 5.5 V, C _L = 50 PF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN TO MAX [†]				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	TYP	MAX	
f _{max}			75*		90		MHz
t _{PLH}	CLKBA or CLKAB	A or B	2	11	2	8.5	ns
t _{PHL}			2	10	2	9	
t _{PLH}	A or B	B or A	2	12	2	9	ns
t _{PHL}			1	8	1	7	
t _{PLH}	SBA or SAB [‡]	A or B	2	15	2	11	ns
t _{PHL}			2	11	2	9	
t _{PZH}	$\overline{\text{OEBA}}$	A	2	11	2	10	ns
t _{PZL}			3	18	3	16	
t _{PHZ}	$\overline{\text{OEBA}}$	A	2	10	2	9	ns
t _{PLZ}			2	10	2	9	
t _{PZH}	OEAB	B	3	12	3	11	ns
t _{PZL}			3	20	3	16	
t _{PHZ}	OEAB	B	2	11	2	10	ns
t _{PLZ}			2	12	2	11	

* On products compliant to MIL-PRF-38535, this parameter is based on characterized data but is not production tested.

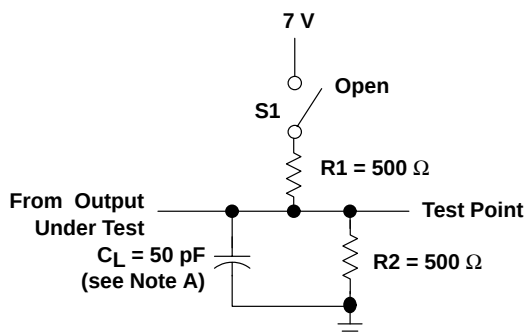
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066G – DECEMBER 1983 – REVISED DECEMBER 2000

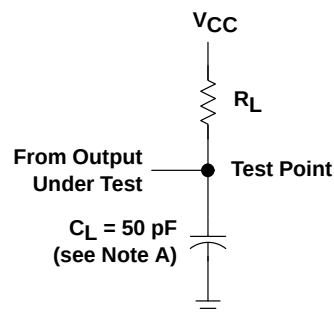
PARAMETER MEASUREMENT INFORMATION



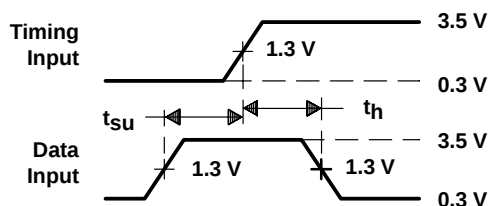
LOAD CIRCUIT
FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

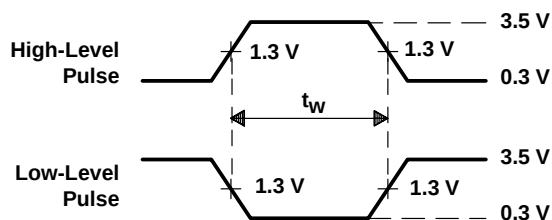
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



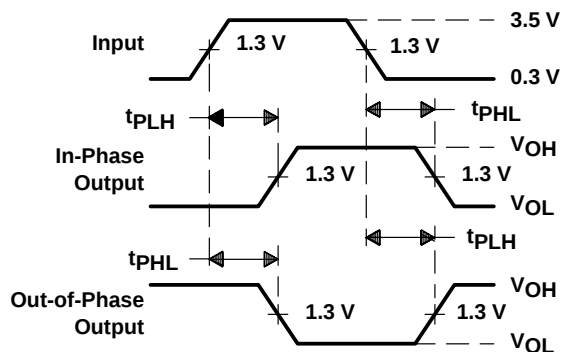
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



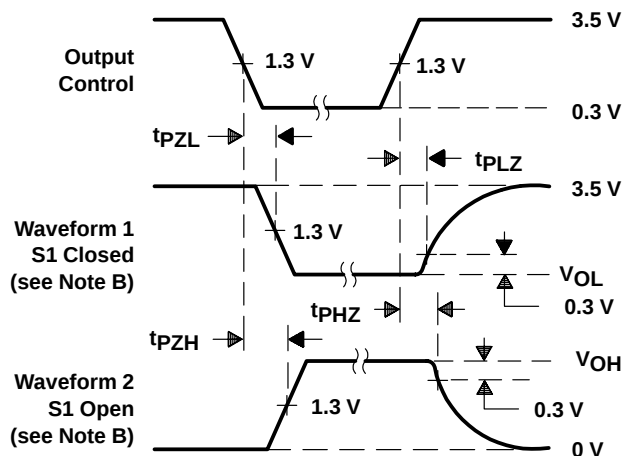
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_0 = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-88673013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
5962-8867301KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	Samples Not Available
5962-8867301LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
5962-88687013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
5962-8868701KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
5962-8868701LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
5962-88753013A	OBSOLETE	LCCC	FK	28		TBD	Call TI	Call TI	Samples Not Available
5962-8875301KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	Samples Not Available
5962-89687013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
5962-8968701KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
5962-8968701LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN54ALS652JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN54AS651JT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI	Samples Not Available
SN54AS652JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN74ALS651A-1DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS651A-1DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS651A-1NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS651ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS651ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS652A-1DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652A-1DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652A-1DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652A-1NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS652A-1NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS652ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS652ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS652ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS652ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS653-1DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS653-1NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS653DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS653DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS653DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS653DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS653DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS653DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS653NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS653NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS654DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS654DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS654DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS654DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS654DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS654DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS654NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS654NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74AS651DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74AS651DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74AS651NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
SN74AS652DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74AS652DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74AS652DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74AS652NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74AS652NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SNJ54ALS652FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54ALS652JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54ALS652W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	Samples Not Available
SNJ54ALS653FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54ALS653JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54ALS653W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54AS651JT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI	Samples Not Available
SNJ54AS652FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54AS652JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54AS652W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

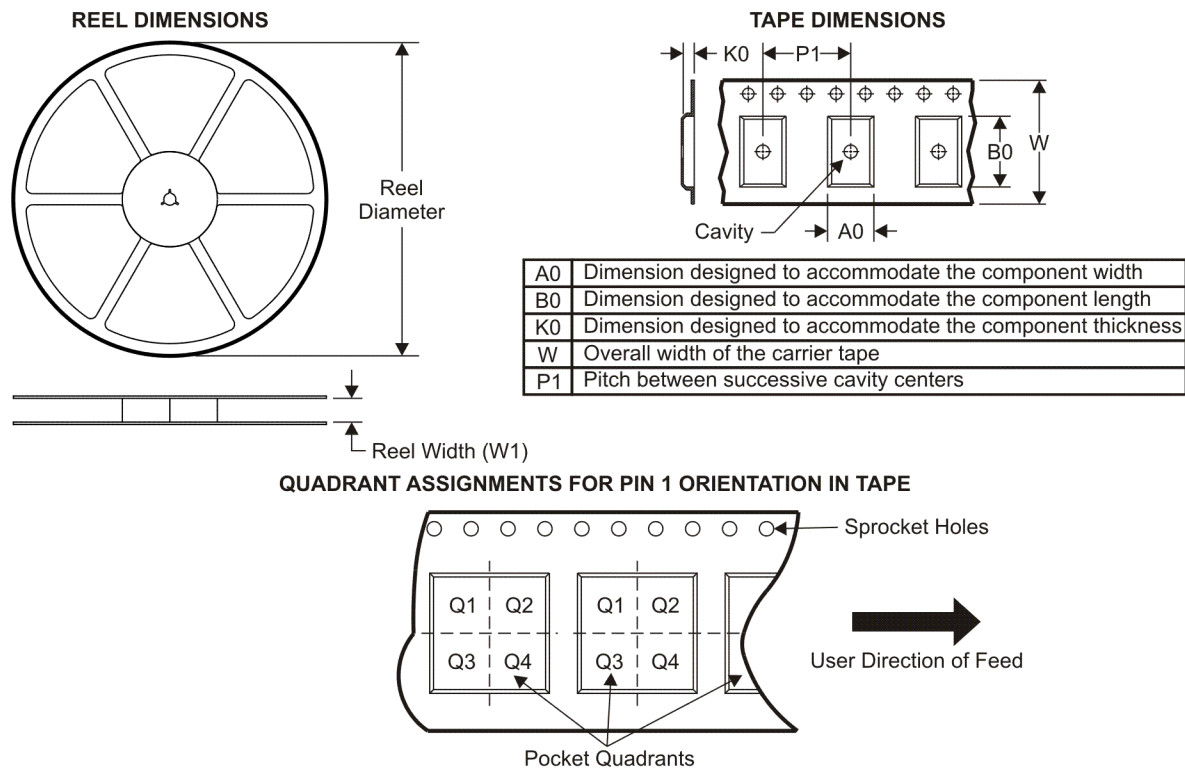
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS652, SN54ALS653, SN54AS651, SN54AS652, SN74ALS653, SN74AS651, SN74AS652 :

- Catalog: [SN74ALS652](#), [SN74ALS653](#), [SN74AS651](#), [SN74AS652](#)
- Military: [SN54ALS653](#), [SN54AS651](#), [SN54AS652](#)

NOTE: Qualified Version Definitions:

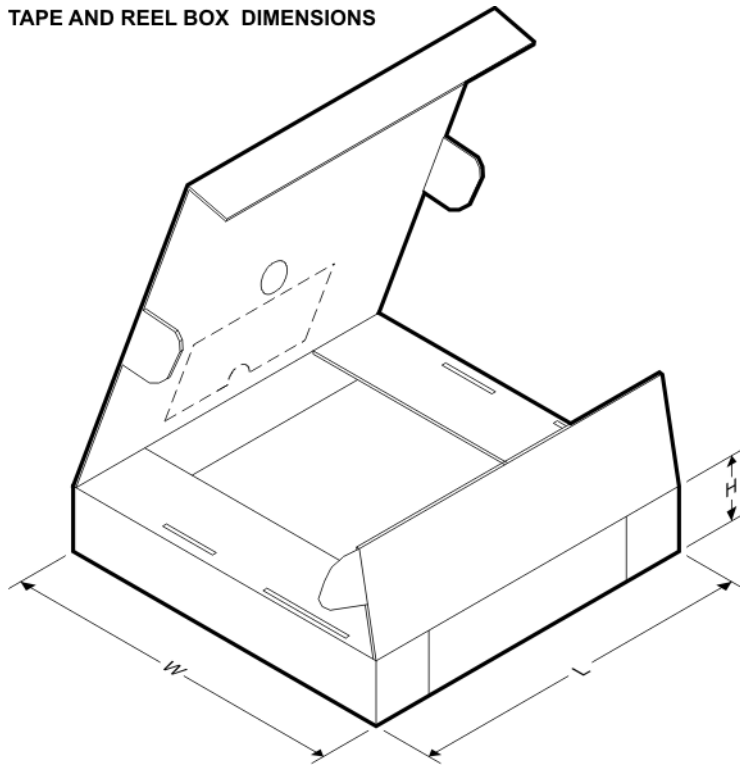
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS652ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ALS653DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ALS654DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



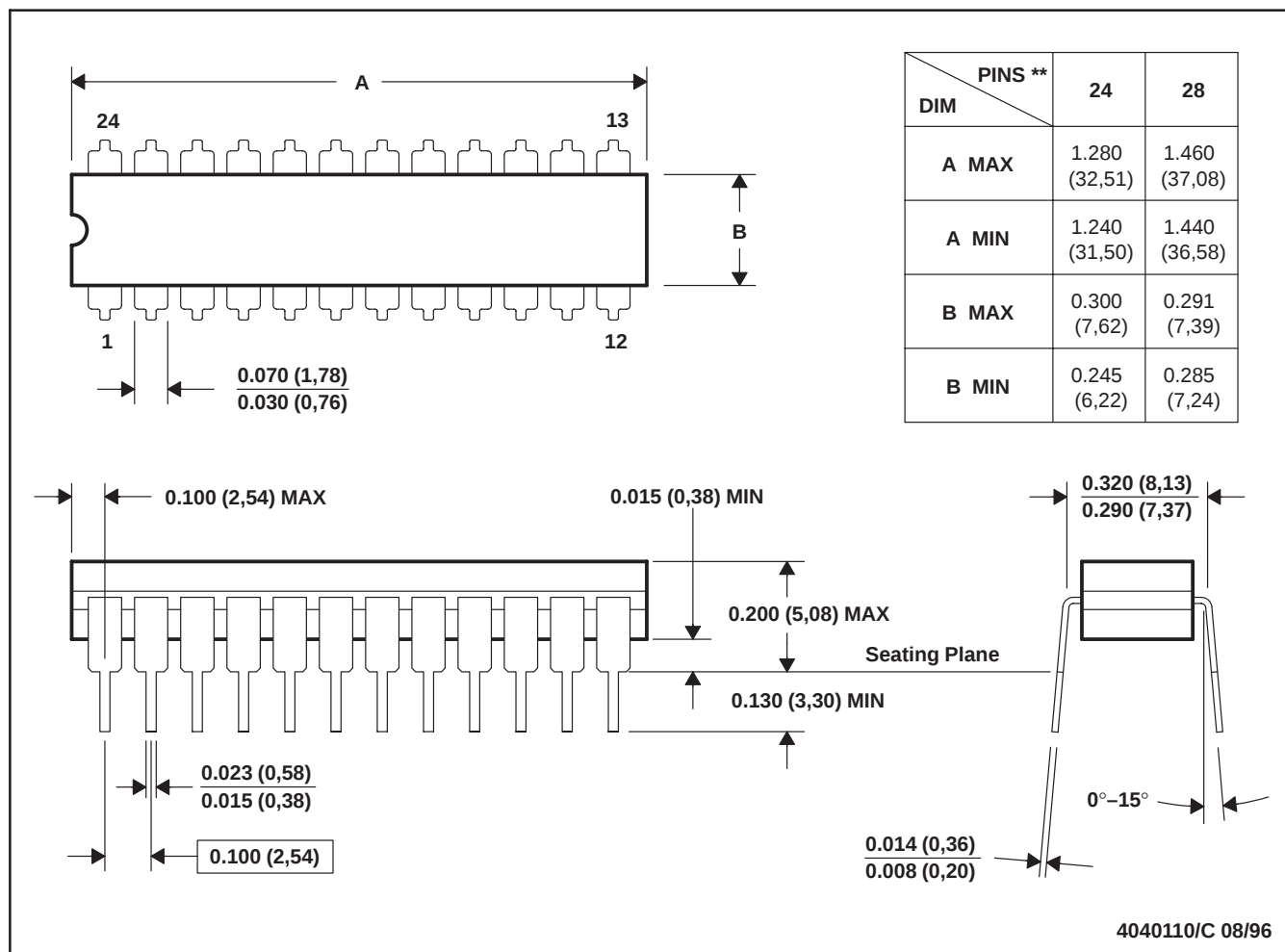
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS652ADWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74ALS653DWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74ALS654DWR	SOIC	DW	24	2000	346.0	346.0	41.0

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

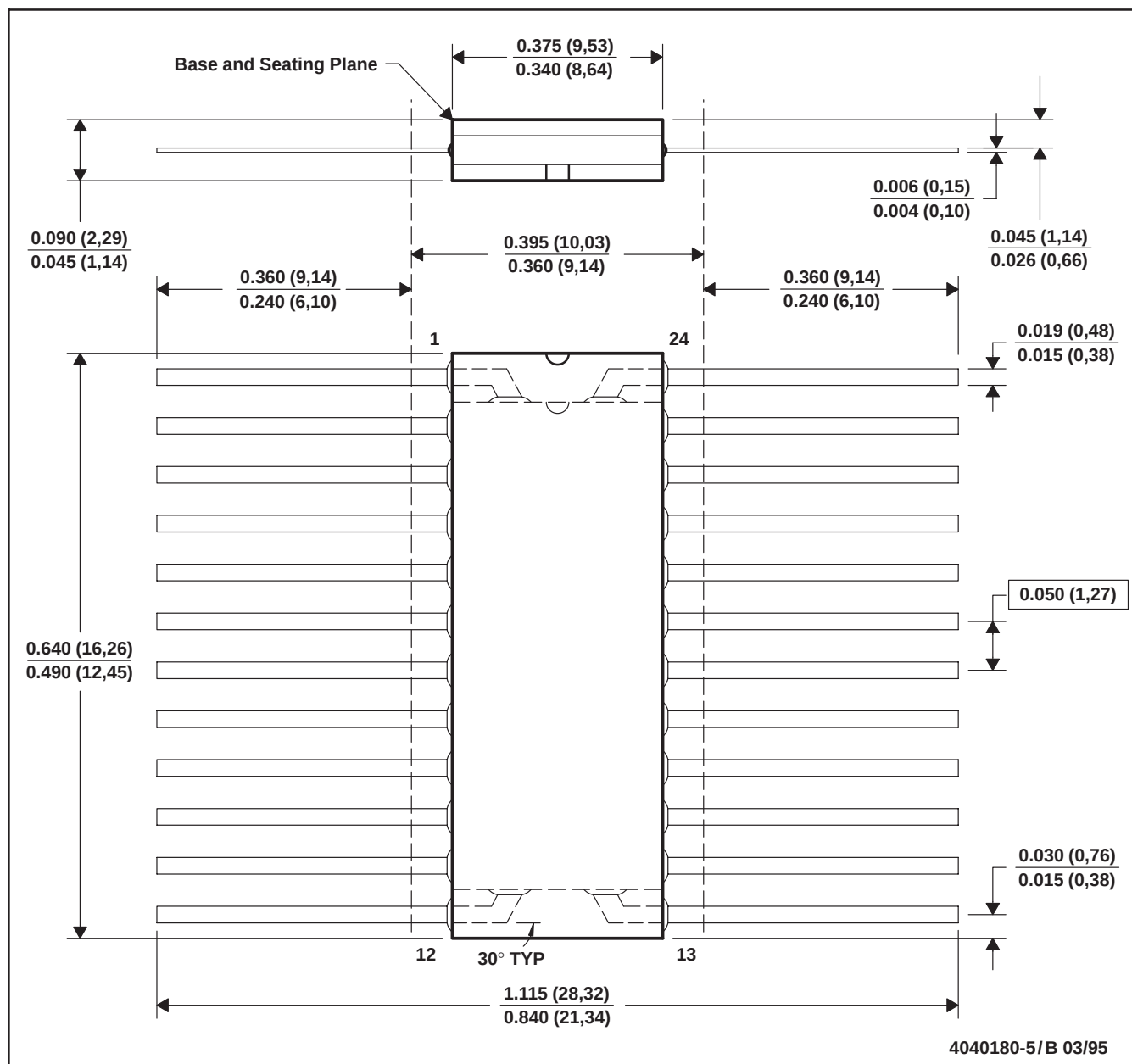
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

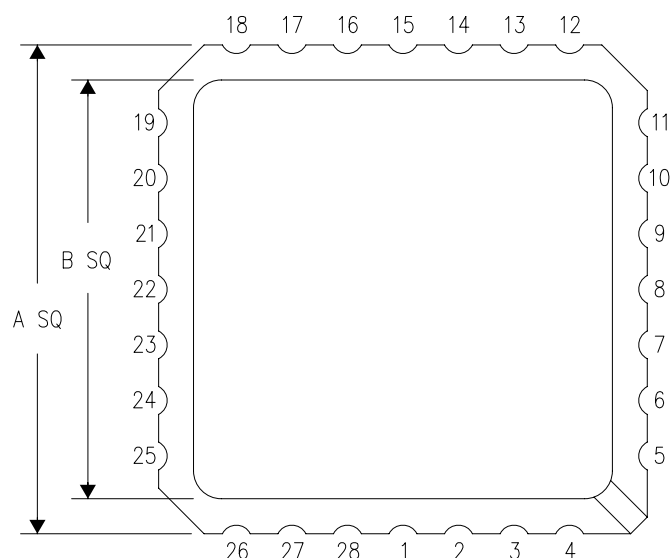


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.

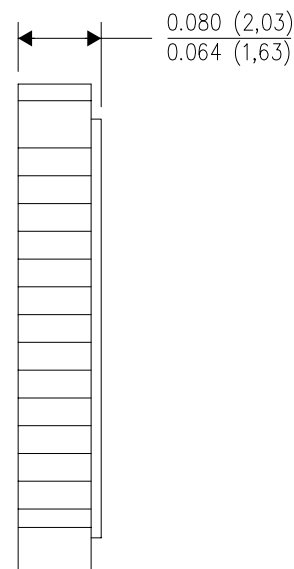
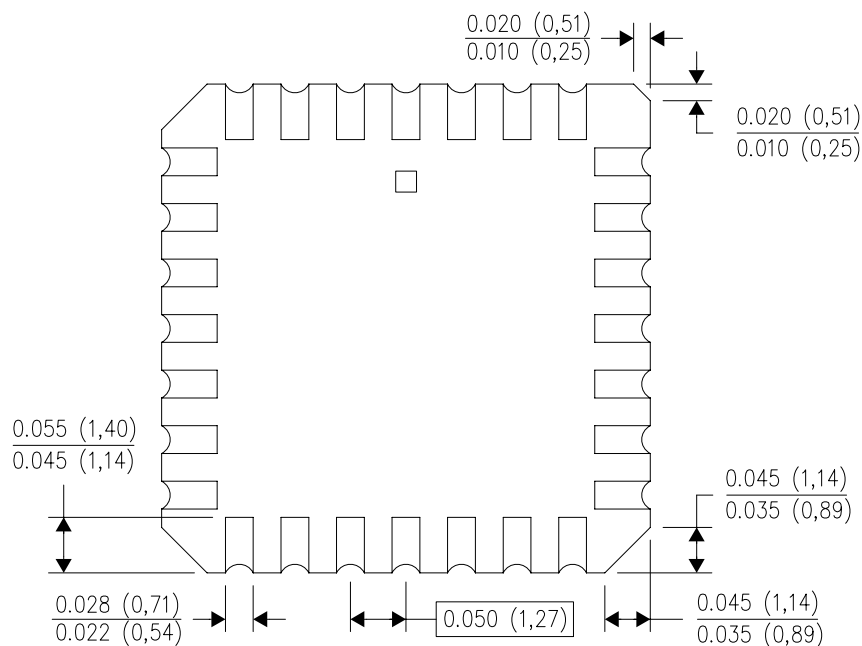
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

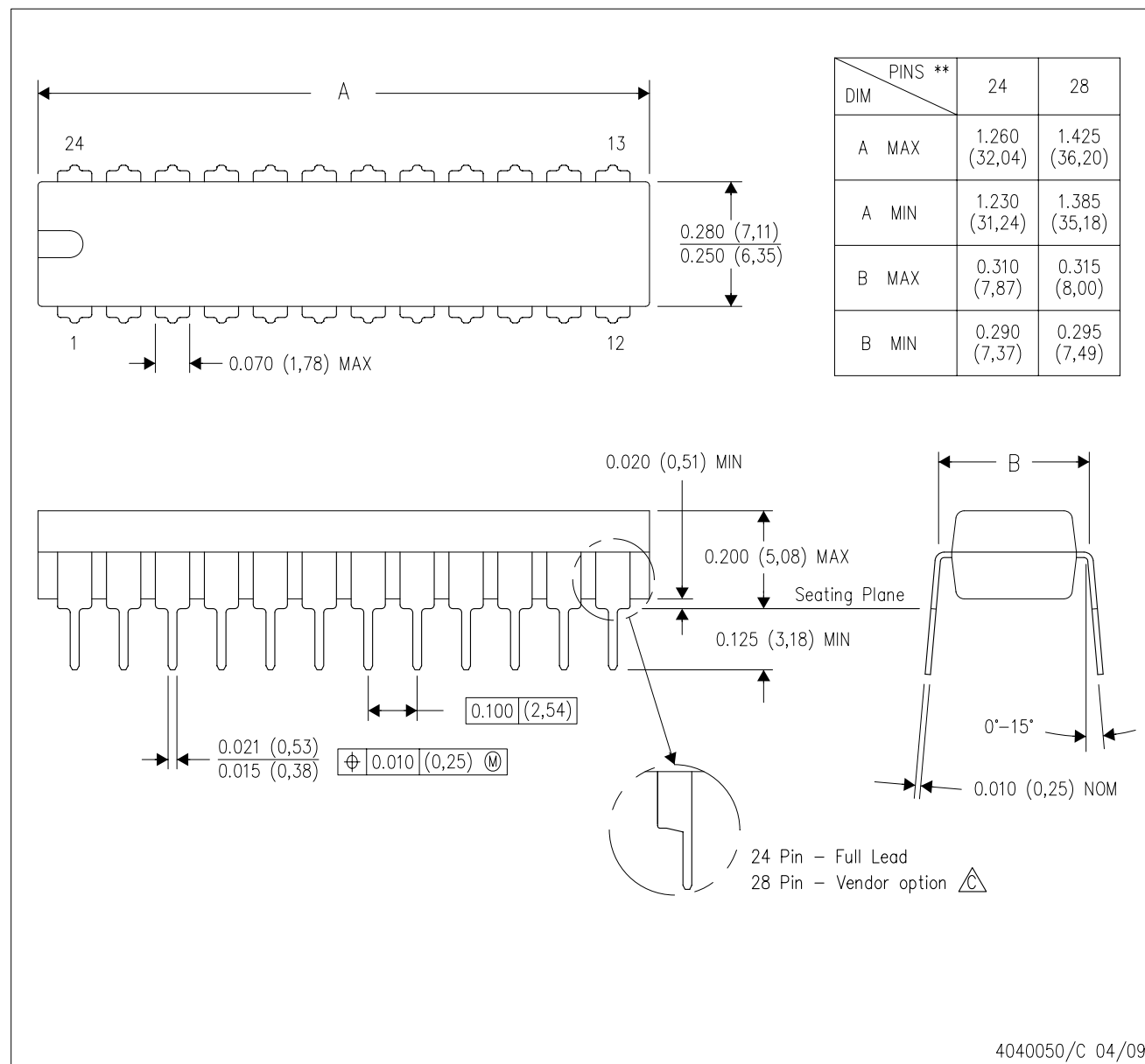
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

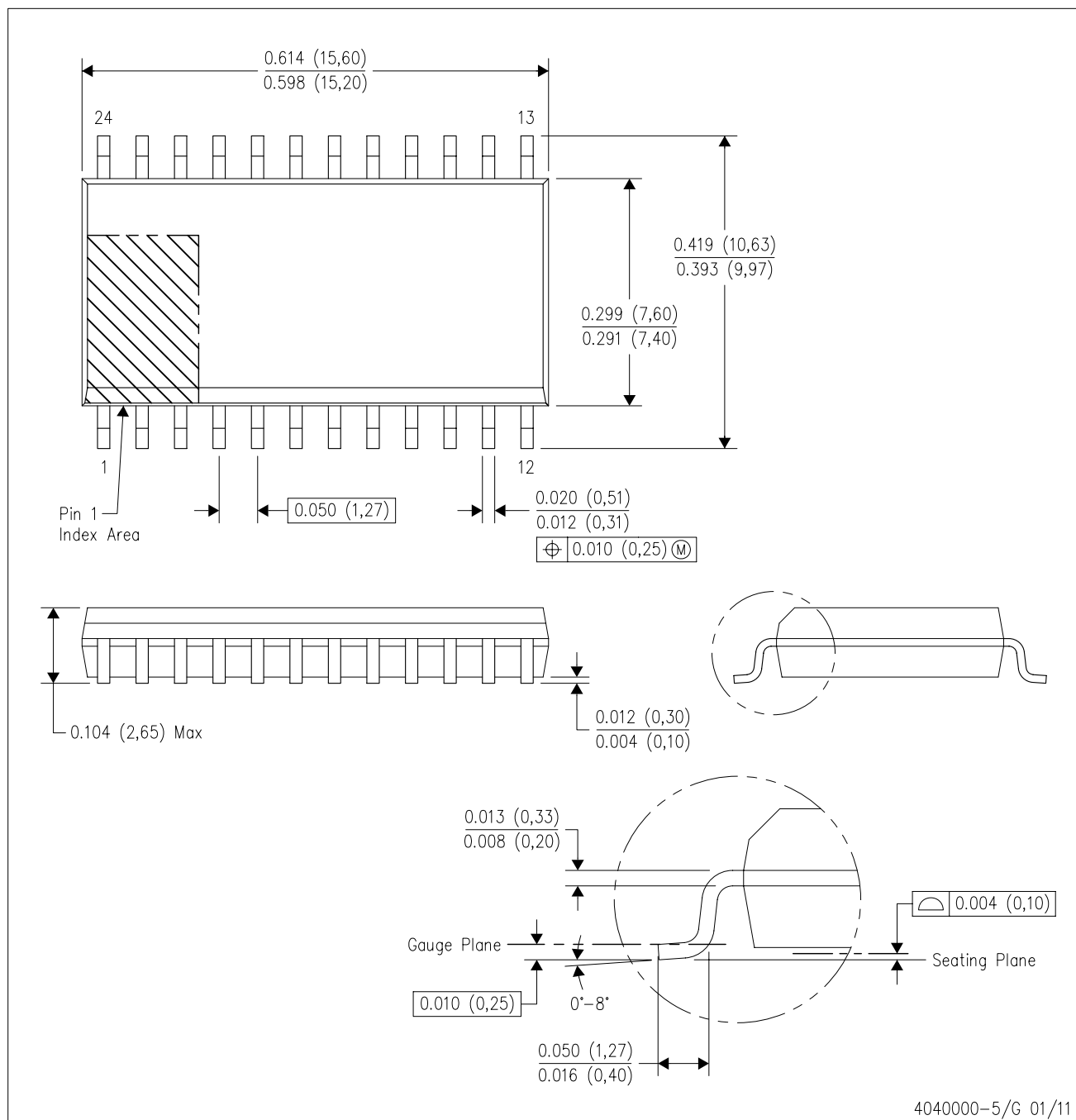
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - $\triangle C$ The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated