SGDS024 - FEBRUARY 2002

 Q Devices Meet Automotive Performance Requirements 	DW OR PW PACKAGE (TOP VIEW)
 Customer-Specific Configuration Control Can Be Supported Along with Major-Change Approval 	1 OE
 EPIC™ (Enhanced-Performance Implanted CMOS) Process 	1A2
 Inputs Are TTL-Voltage Compatible 	1A3 [] 6 15 [] 2A3
 Latch-Up Performance Exceeds 250 mA Per 	2Y2 [7 14] 1Y3
JESD 17	1A4 🛛 8 13 🗓 2A2
	2Y1 [] 9 12 [] 1Y4
description	GND 🛛 10 🔀 11 🗍 2A1

This octal buffer/driver is designed specifically to improve both the performance and density of

3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHCT244Q is organized as two 4-bit buffers/line drivers with separate output-enable (OE) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC - D	Tape and reel	SN74AHCT244QDWR	AHCT244Q
-40 C to 125 C	TSSOP - PW	Tape and reel	SN74AHCT244QPWR	HB244Q

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 4-bit buffer/driver)

INP	JTS	OUTPUT
Œ	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

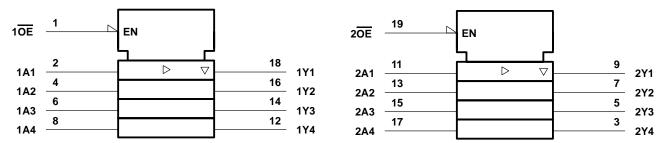


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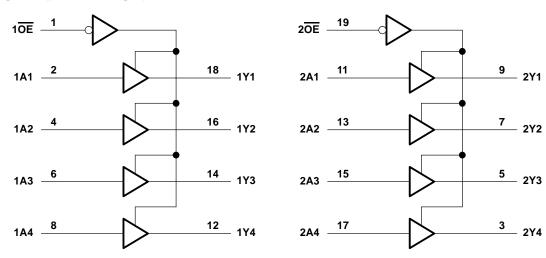


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

–0.5 V to 7 V
–0.5 V to 7 V
\dots -0.5 V to V _{CC} + 0.5 V
–20 mA
±20 mA
±25 mA
±75 mA
58°C/W
83°C/W
–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7



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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
٧ _I	Input voltage	0	5.5	V
Vo	Output voltage	0	VCC	V
ЮН	High-level output current		-8	mA
loL	Low-level output current		8	mA
TA	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T _A = 25°C			MIN	MAX	UNIT		
	TEST CONDITIONS		vcc	MIN	TYP	MAX	IVIIIN	WAX	UNIT	
Voн	I _{OH} = -50 μA		4.5 V	4.4	4.5		4.4		V	
VOH	$I_{OH} = -8 \text{ mA}$		4.5 V	3.94			3.8		٧	
Vai	I _{OL} = 50 μA		4.5 V			0.1		0.1	٧	
V _{OL}	I _{OL} = 8 mA		4.5 V	4.5 V			0.36		0.44	٧
loz	$V_O = V_{CC}$ or GND		5.5 V			±0.25		±2.5	μΑ	
lį	$V_I = 5.5 \text{ V or GND}$		0 V to 5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND,	= 0	5.5 V			4		40	μΑ	
ΔI _{CC} †	One input at 3.4 V, Other inputs at V _{CC} or GND		5.5 V			1.35		1.5	mA	
C _i	$V_I = V_{CC}$ or GND	·	5 V		2.5	10			pF	
Co	$V_O = V_{CC}$ or GND		5 V		3				pF	

This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

•			-						
PARAMETER	FROM	то	то	TO LOAD	T _A = 25°C		MIN MA	MAV	K UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	MAX	UNII
^t PLH	А	Y	C _L = 15 pF		5.4	7.4	1	8.5	20
^t PHL	A	Y	CL = 15 pr		5.4	7.4	1	8.5	ns
^t PZH		Y	C _I = 15 pF		7.7	10.4	1	12	ns
^t PZL	ŌĒ	Y	OL = 13 pi		7.7	10.4	1	12	110
^t PHZ	ŌĒ	Y	C _I = 15 pF		5	9.4	1	10	ns
^t PLZ	OE		OL = 13 pi		5	9.4	1	10	115
^t PLH	А	Y	C ₁ = 50 pF		5.9	8.4	1	9.5	20
^t PHL	A	Ť	C[= 50 pr		5.9	8.4	1	9.5	ns
^t PZH	ŌĒ	Y	C _L = 50 pF		8.2	11.4	1	13	20
tPZL	OE	Ť	CL = 50 pr		8.2	11.4	1	13	ns
^t PHZ		Y	C _L = 50 pF		8.8	11.4	1	13	20
tPLZ	ŌĒ		GL = 30 pr		8.8	11.4	1	13	ns
tsk(o)			C _L = 50 pF			1		_	ns



SN74AHCT244Q **OCTAL BUFFER/DRIVER** WITH 3-STATE OUTPUTS SGDS024 – FEBRUARY 2002

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

	PARAMETER	MIN	TYP	MAX	UNIT
VOH(V)	Quiet output, minimum dynamic V _{OH}		4.1		V
V _{IH(D)}	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

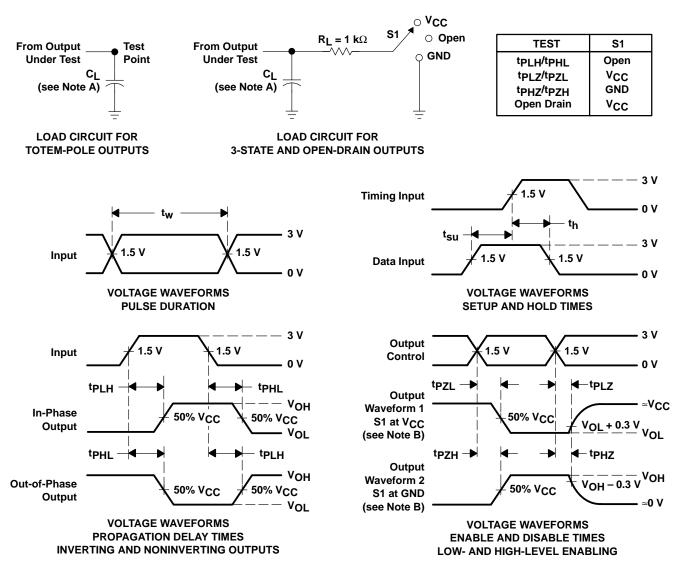
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	8.2	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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