- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

SN54ABT2245 . . . J OR W PACKAGE
SN74ABT2245 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)

DIR	1	20 V_{CC}
A1	2	19 $\overline{OE}$
A2	3	18 B1
A3	4	17 B2
A4	5	16 B3
A5	6	15 B4
A6	7	14 B5
A7	8	13 B6
A8	9	12 B7
GND	10	11 B8

SN54ABT2245 . . . FK PACKAGE
(TOP VIEW)

Top pins: A2 (3), A1 (2), DIR (1), V_{CC} (20), $\overline{OE}$ (19)

A3	4	18 B1
A4	5	17 B2
A5	6	16 B3
A6	7	15 B4
A7	8	14 B5

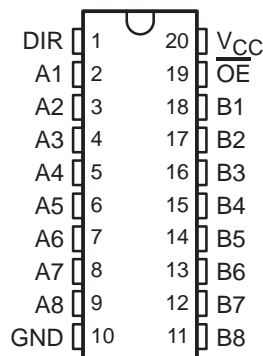Bottom pins: A8 (9), GND (10), B8 (11), B7 (12), B6 (13)

description

These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.
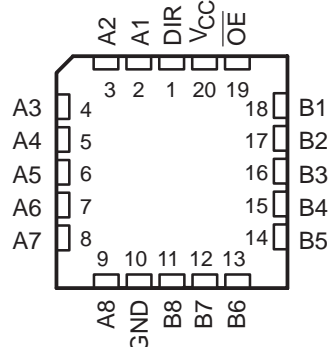
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT2245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
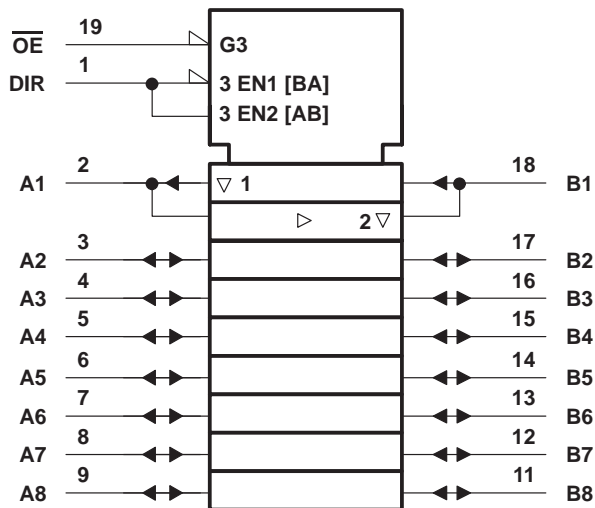
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TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic symbol†

```
           19        ┌─────────────────┐
 OE ───────────────▷│ G3              │
            1        │                 │
 DIR ──────────●───▷│ 3 EN1 [BA]      │
               └────│ 3 EN2 [AB]      │
                    └──┐           ┌──┘
            2          │ ▽ 1       │        18
 A1 ──────────●──◄────│           │────◄──●──────── B1
              └───────│      ▷  2 ▽│───────┘
            3          │           │        17
 A2 ──────────◄►──────│           │──────◄►──────── B2
            4          │           │        16
 A3 ──────────◄►──────│           │──────◄►──────── B3
            5          │           │        15
 A4 ──────────◄►──────│           │──────◄►──────── B4
            6          │           │        14
 A5 ──────────◄►──────│           │──────◄►──────── B5
            7          │           │        13
 A6 ──────────◄►──────│           │──────◄►──────── B6
            8          │           │        12
 A7 ──────────◄►──────│           │──────◄►──────── B7
            9          │           │        11
 A8 ──────────◄►──────│           │──────◄►──────── B8
                      └───────────┘
```

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Seven Other Channels

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

schematic of A-port outputs
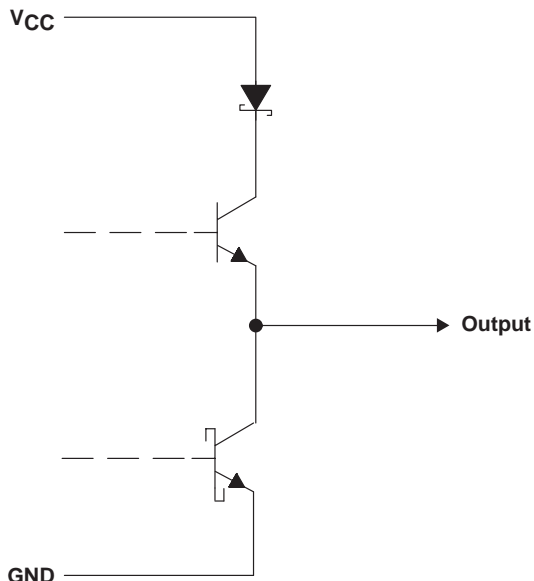
schematic of B-port outputs
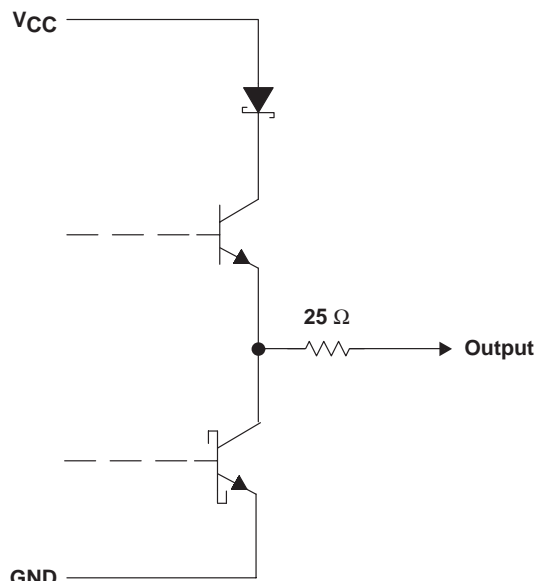
All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V

Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V

Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V

Current into any output in the low state, I_O: SN54ABT2245 (except B port) .... 96 mA

SN74ABT2245 (except B port) .... 128 mA

B port .... 30 mA

Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA

Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA

Package thermal impedance, θ_{JA} (see Note 2): DB package .... 115°C/W

DW package .... 97°C/W

N package .... 67°C/W

PW package .... 128°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT2245		SN74ABT2245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3:   Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$ MIN	TYP†	MAX	SN54ABT2245 MIN	SN54ABT2245 MAX	SN74ABT2245 MIN	SN74ABT2245 MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2		-1.2		-1.2	V
V_{OH}	B port	$V_{CC} = 4.5$ V,	$I_{OH} = -1$ mA	3.35			3.3		3.35		V
		$V_{CC} = 5$ V,	$I_{OH} = -1$ mA	3.85			3.8		3.85		
		$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA				3		3.1		
			$I_{OH} = -12$ mA	2.6					2.6		
	A port	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}	B port	$V_{CC} = 4.5$ V	$I_{OL} = 8$ mA			0.65		0.8		0.65	V
			$I_{OL} = 12$ mA			0.8				0.8	
	A port		$I_{OL} = 48$ mA			0.55		0.55			
			$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	$V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND				±1		±1		±1	µA
	A or B ports	$V_{CC} = 2.1$ V to 5.5 V, $V_I = V_{CC}$ or GND				±20		±20		±20	
I_{OZH}‡		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V				10		10		10	µA
I_{OZL}‡		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V				-10		-10		-10	µA
I_{OZPU}§		$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZPD}§		$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{off}		$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}	Outputs high	$V_{CC} = 5.5$ V,	$V_O = 5.5$ V			50		50		50	µA
I_O¶	B port	$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	-25		-100	-25	-100	-25	-100	mA
	A port			-50	-100	-180	-50	-180	-50	-180	
I_{CC}	A or B ports	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high	1		250		250		250	µA
			Outputs low	24		32		32		32	mA
			Outputs disabled	0.5		250		250		250	µA
ΔI_{CC}#	Data inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i		$V_I = 2.5$ V or 0.5 V			3						pF
C_{io}		$V_O = 2.5$ V or 0.5 V			6						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ This parameter is characterized but not production tested.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS INSTRUMENTS

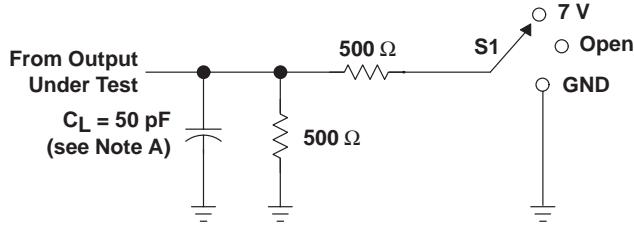POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2245		SN74ABT2245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	2.5	3.4	1	4	1	3.8	ns
t_{PHL}			1	3.2	4.2	1	4.6	1	4.5	
t_{PLH}	B	A	1	2.2	3.2	1	3.8	1	3.6	ns
t_{PHL}			1	2.7	3.6	1	4.2	1	4	
t_{PZH}	$\overline{OE}$	A	1	3.3	4.6	1	5.6	1	5.5	ns
t_{PZL}			1	3.2	4.7	1	6	1	5.7	
t_{PHZ}	$\overline{OE}$	A	2	4	5.1	2	5.7	2	5.6	ns
t_{PLZ}			1	2.9	4	1	4.6	1	4.5	
t_{PZH}	$\overline{OE}$	B	1.5	3.6	4.9	1.5	6.3	1.5	6.1	ns
t_{PZL}			1.5	3.9	5.3	1.5	6.6	1.5	6.3	
t_{PHZ}	$\overline{OE}$	B	1.5	3.6	4.7	1.5	5.5	1.5	5.3	ns
t_{PLZ}			1.5	3.3	4.4	1.5	4.9	1.5	4.8	

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

From Output Under Test

$C_L = 50$ pF (see Note A)

500 Ω   500 Ω   S1

7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

Input t_w 1.5 V   1.5 V   3 V   0 V
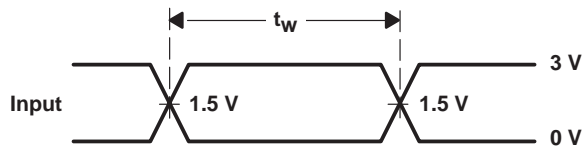
VOLTAGE WAVEFORMS
PULSE DURATION

Timing Input   1.5 V   3 V   0 V

Data Input t_{su} t_h 1.5 V   1.5 V   3 V   0 V
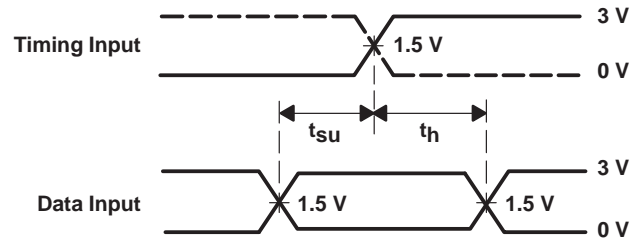
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Input   1.5 V   1.5 V   3 V   0 V

t_{PLH} t_{PHL}

Output   1.5 V   1.5 V V_{OH} V_{OL}

t_{PHL} t_{PLH}

Output   1.5 V   1.5 V V_{OH} V_{OL}
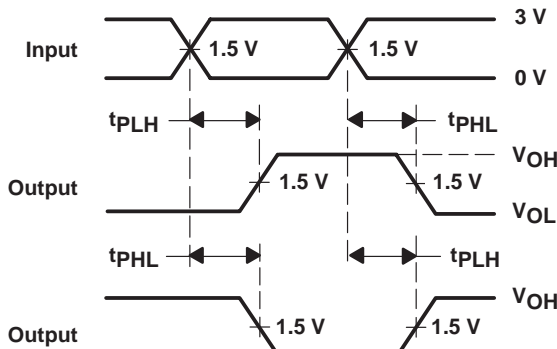
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

Output Control   1.5 V   1.5 V   3 V   0 V

t_{PZL} t_{PLZ}

Output Waveform 1 S1 at 7 V (see Note B)   1.5 V   3.5 V $V_{OL} + 0.3$ V V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 S1 at Open (see Note B)   1.5 V $V_{OH} - 0.3$ V V_{OH} ≈ 0 V
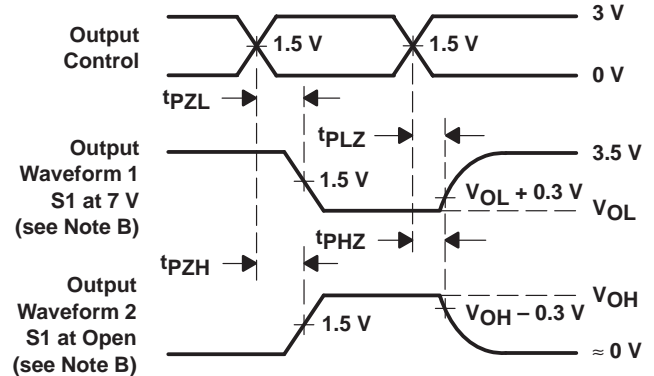
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω, $t_r ≤ 2.5$ ns, $t_f ≤ 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
5962-9560601Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9560601QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9560601QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN74ABT2245DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74ABT2245DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ABT2245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ABT2245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74ABT2245PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	
SN74ABT2245PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT2245PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ABT2245FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ABT2245J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54ABT2245W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ABT2245, SN74ABT2245 :

- Catalog: SN74ABT2245

- Military: SN54ABT2245

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
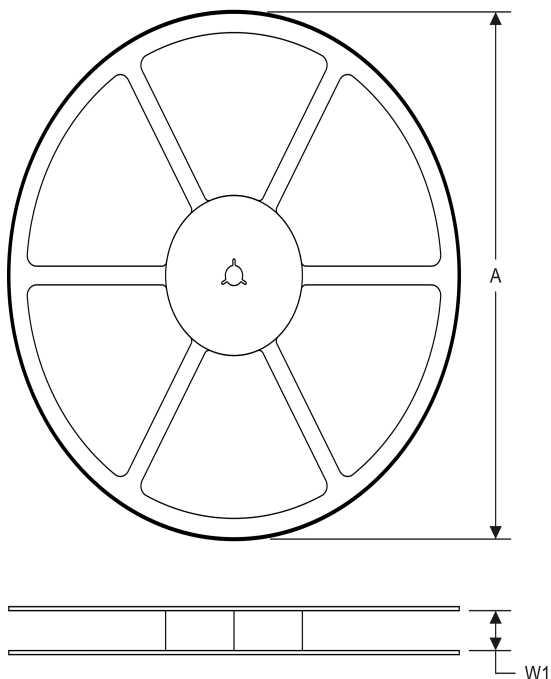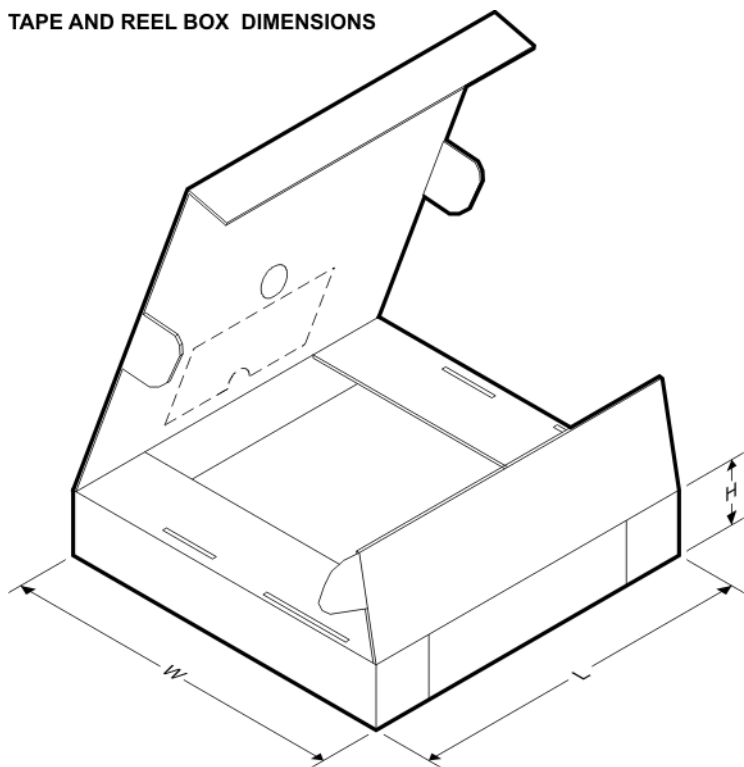
TAPE DIMENSIONS
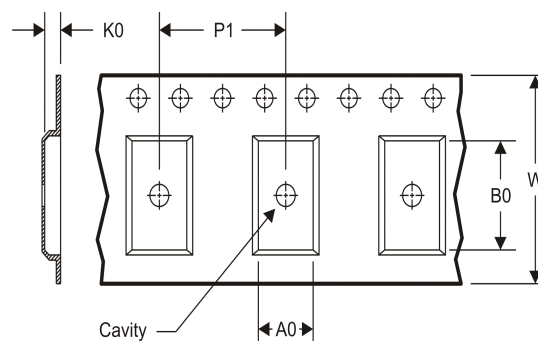
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT2245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ABT2245NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74ABT2245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2245DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74ABT2245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABT2245NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ABT2245PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

J (R−GDIP−T**)

CERAMIC DUAL IN−LINE PACKAGE

14 LEADS SHOWN
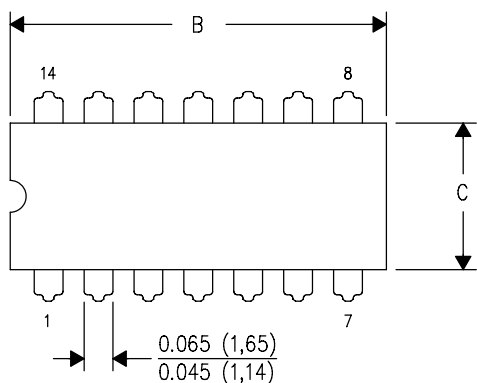
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°−15°

0.026 (0,66)
0.014 (0,36)
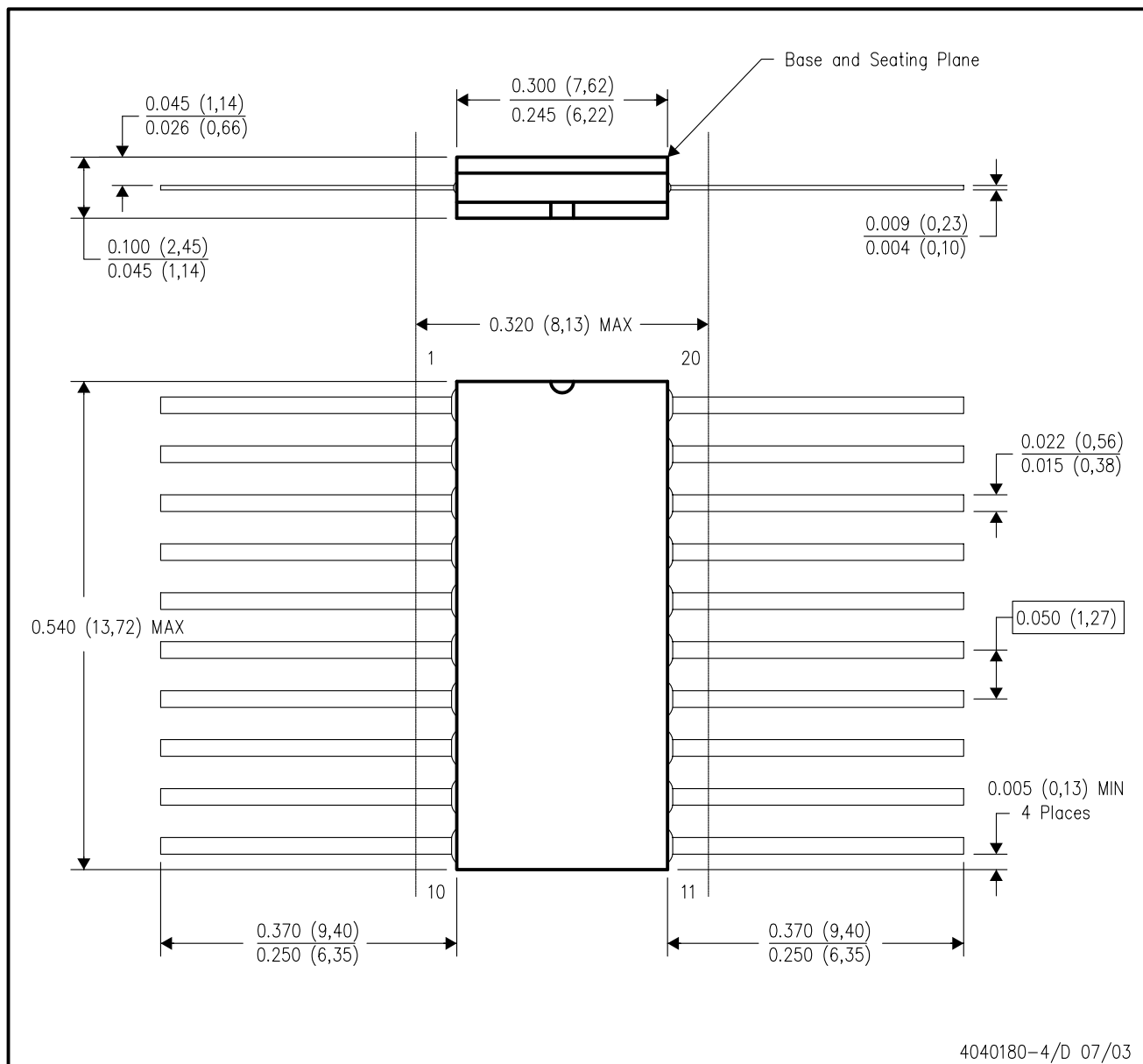
0.100 (2,54)

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.300\ (7,62)}{0.245\ (6,22)}$

$\dfrac{0.100\ (2,45)}{0.045\ (1,14)}$

$\dfrac{0.009\ (0,23)}{0.004\ (0,10)}$

0.320 (8,13) MAX

1   20

$\dfrac{0.022\ (0,56)}{0.015\ (0,38)}$

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$

4040180−4/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
   E.   Falls within Mil−Std 1835 GDFP2−F20

FK (S−CQCC−N**)
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER
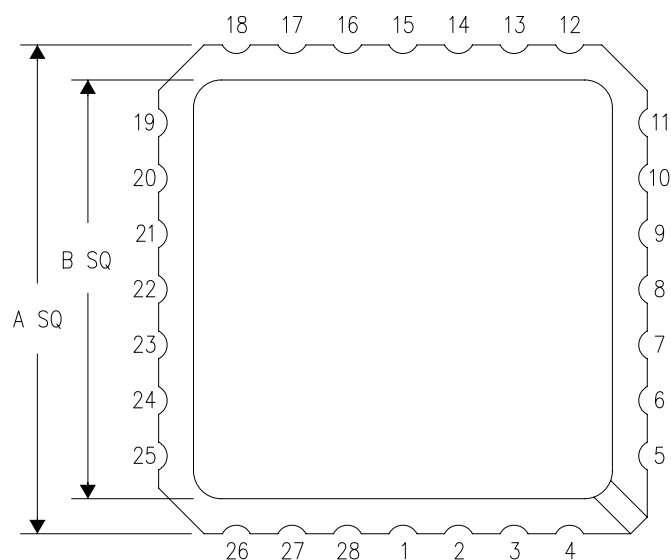
| NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)
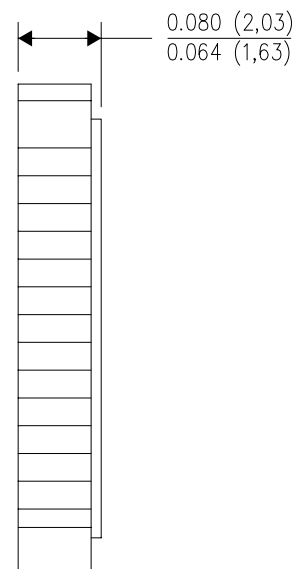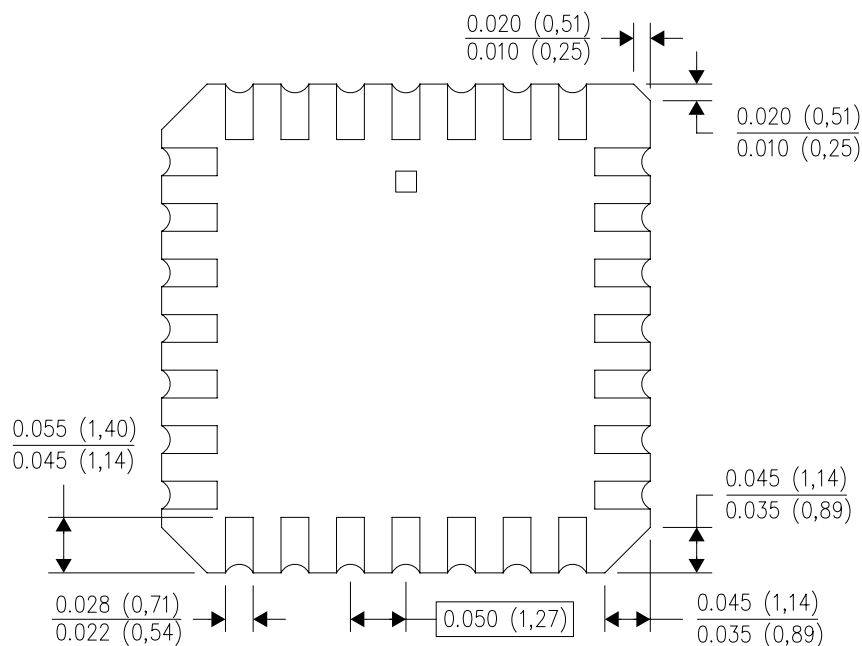
4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a metal lid.
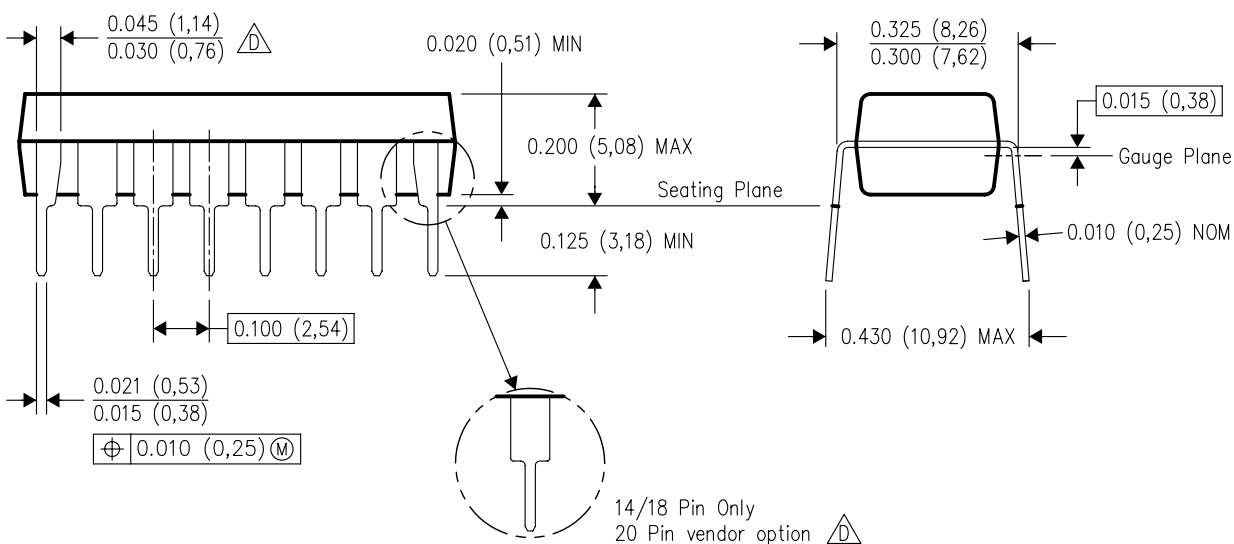   D. Falls within JEDEC MS−004

N (R-PDIP-T)**   PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN
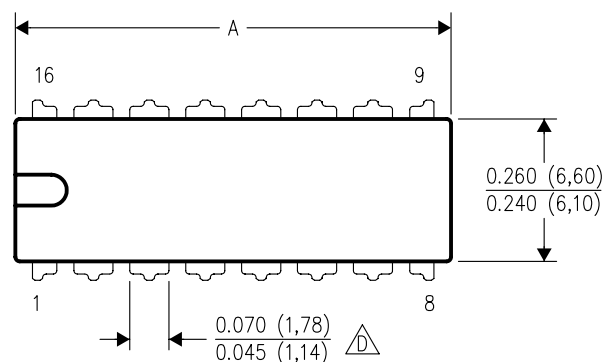
DIM	PINS **	14	16	18	20
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION		AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX
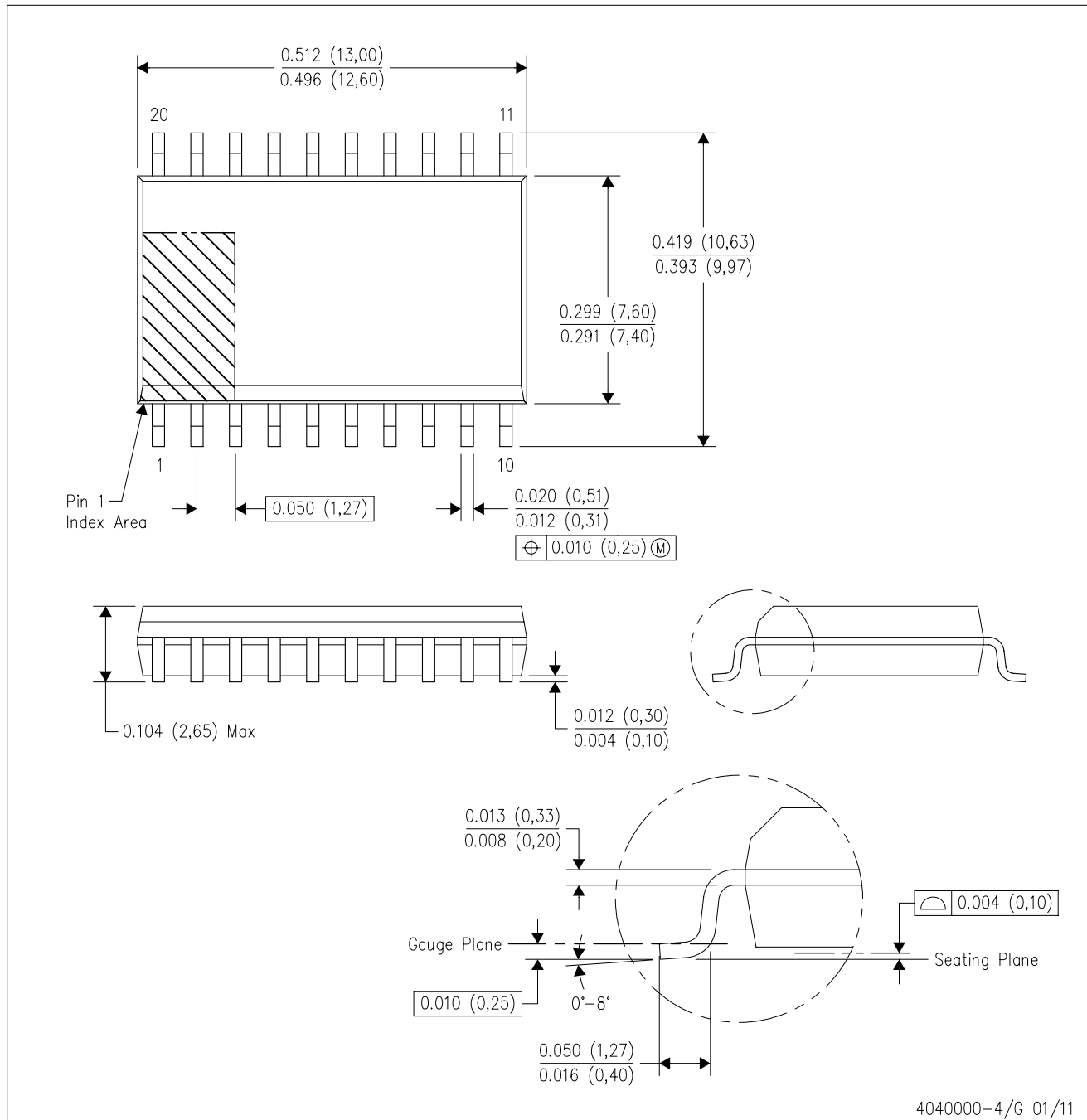
14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.
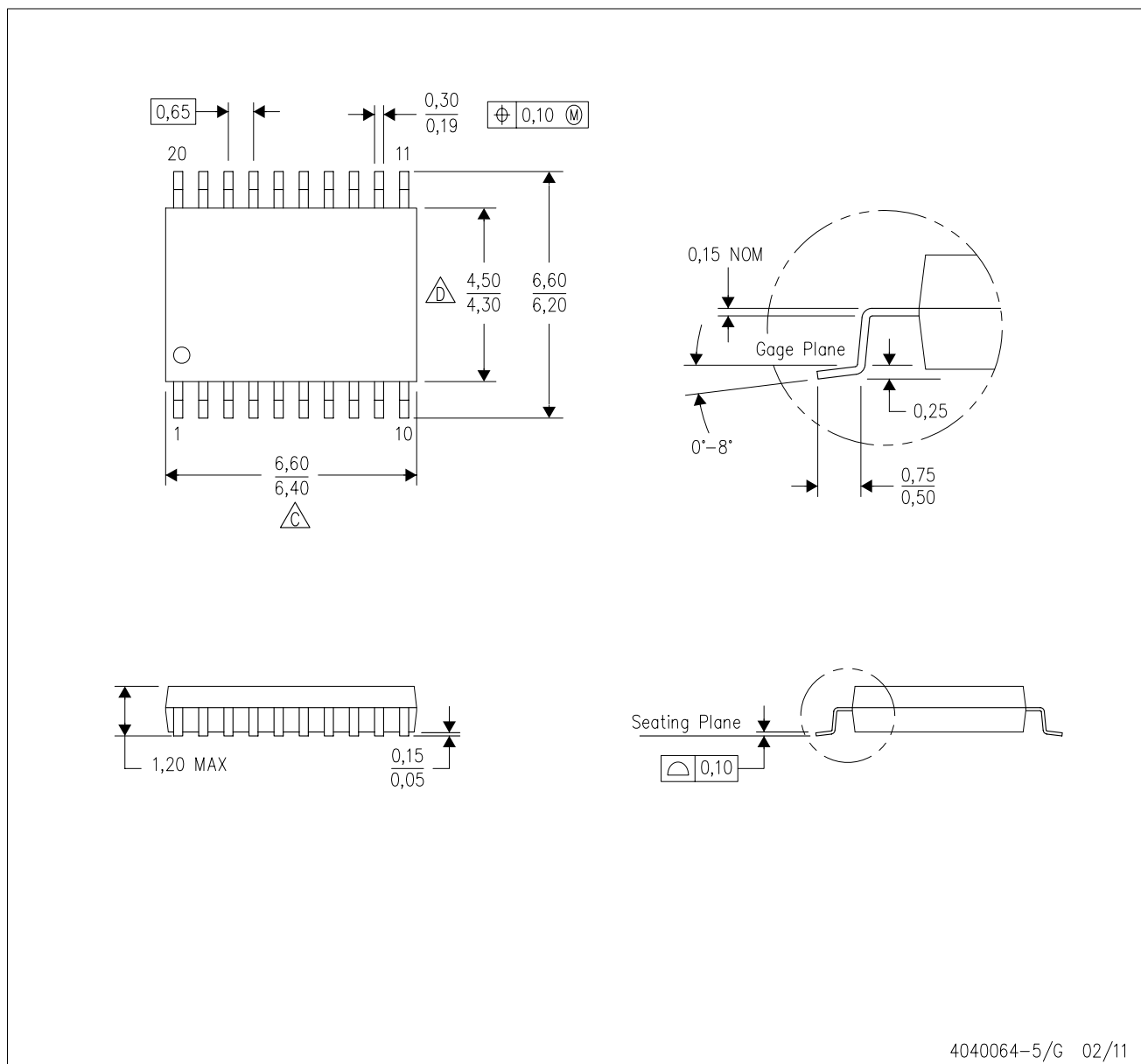
DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

$\frac{0.512\ (13,00)}{0.496\ (12,60)}$

20   11

$\frac{0.419\ (10,63)}{0.393\ (9,97)}$

$\frac{0.299\ (7,60)}{0.291\ (7,40)}$

1   10

Pin 1
Index Area

0.050 (1,27)

$\frac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\frac{0.012\ (0,30)}{0.004\ (0,10)}$

$\frac{0.013\ (0,33)}{0.008\ (0,20)}$

⌂ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

$\frac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−4/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AC.
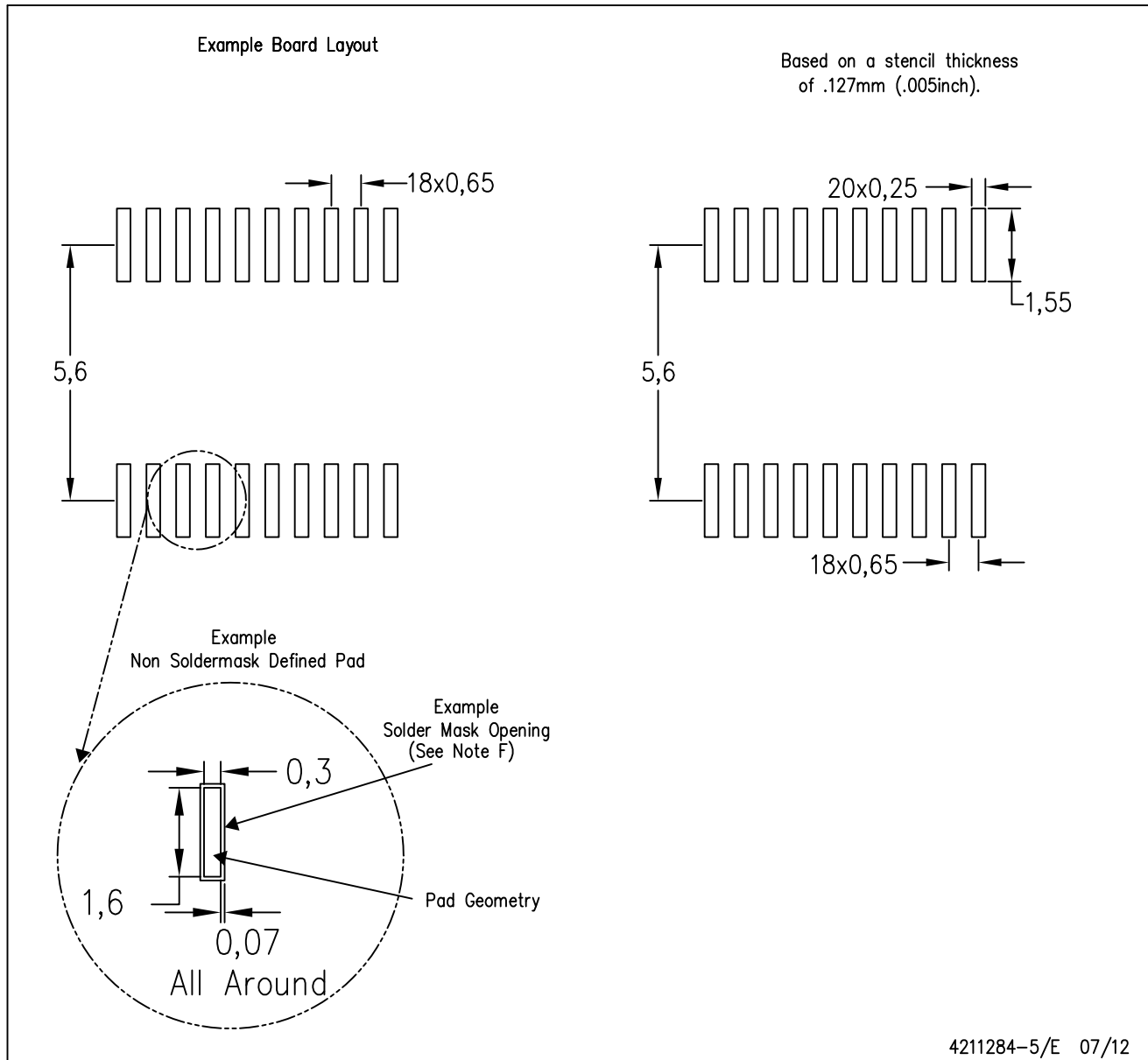
**TEXAS
INSTRUMENTS**
www.ti.com

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   → |←   →| ← 0,30 / 0,19   ⊕ 0,10 Ⓜ

20   11

⟨D⟩   4,50 / 4,30   6,60 / 6,20

1   10

6,60 / 6,40

⟨C⟩

0,15 NOM

Gage Plane

0°−8°

0,25

0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane

◁ 0,10

4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153

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PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

5,6

5,6

1,55

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/E 07/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

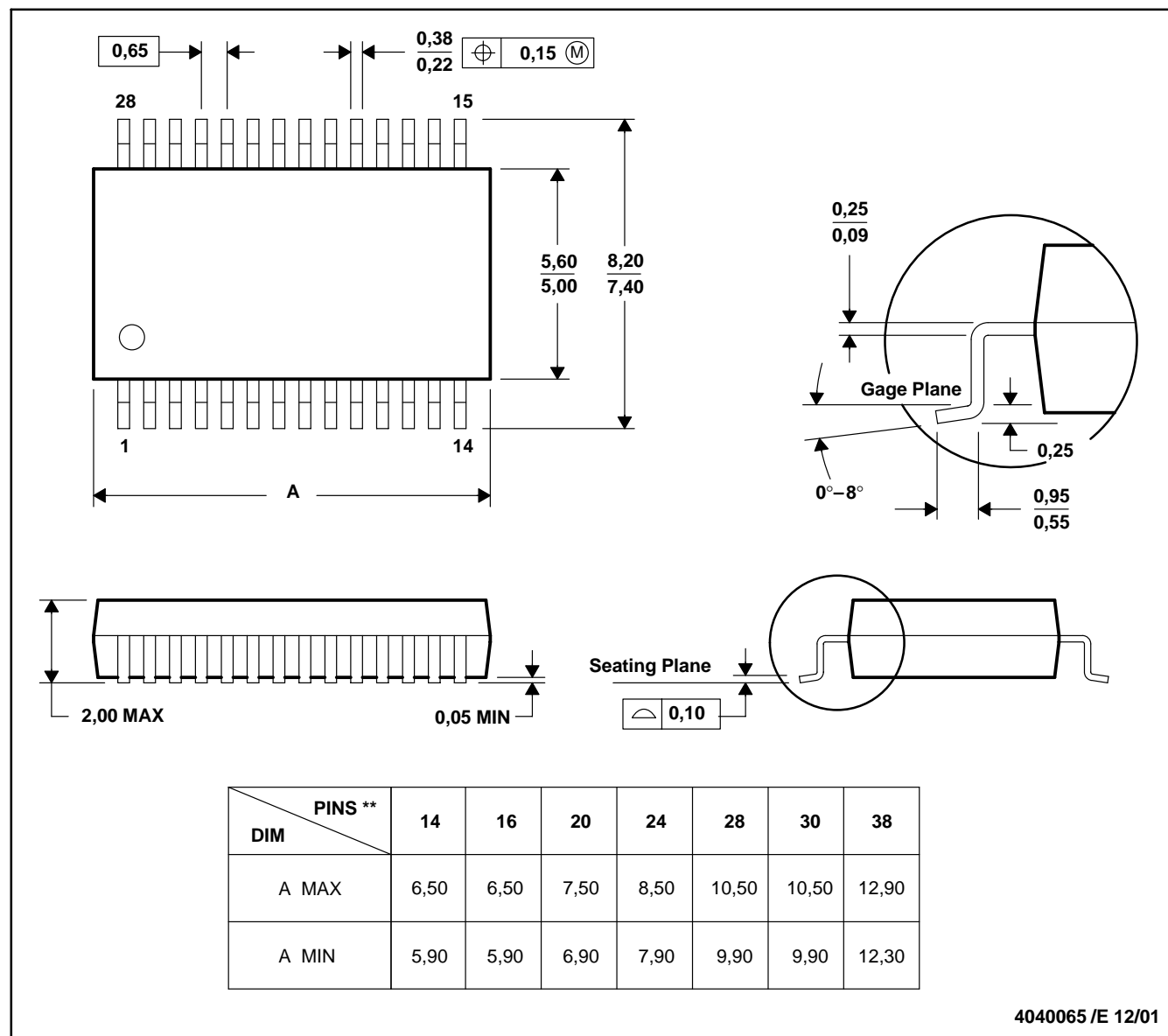| DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

	PINS **	14	16	20	24	28	30	38
DIM								
A MAX		6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN		5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A.   All linear dimensions are in millimeters.
        B.   This drawing is subject to change without notice.
        C.   Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D.   Falls within JEDEC MO-150

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