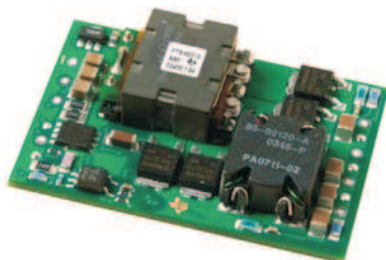


DUAL COMPLEMENTARY-OUTPUT DC/DC CONVERTER FOR DSL

FEATURES

- Dual Complementary Outputs (± 5 V, ± 12 V, or ± 15 V)
- Input Voltage Range: 36 V to 75 V
- On/Off Enable for Sequencing
- 1500 VDC Isolation
- Over-Current Protection
- Over-Voltage Protection (PTB48511 only)
- Over-Temperature Shutdown
- Under-Voltage Lockout
- Temp Range: -40°C to 85°C
- Industry Standard Outline
- Fixed Frequency Operation
- Synchronizes with PTB48500
- Powers Line Driver ICs for AC-7 and Other xDSL Chipsets
- Safety Approvals:
 - EN 60950
 - UL/cUL 60950



DESCRIPTION

The PTB4851x series of isolated DC/DC converter modules produce a complementary pair of regulated supply voltages for powering line-driver ICs in xDSL telecom applications. The modules operate from a standard telecom (-48 V) central office (CO) supply and can provide up to a 72 W of power in a balanced load configuration.

The A-suffix module (± 5 V) is designed to power the line driver ICs for the AC-7 ADSL chipset. Other voltage options will power other analog applications requiring a complementary supply with relatively balanced loads.

Both the PTB48510 and PTB48511 include an "on/off" enable control, output current limit, over-temperature protection, and input under-voltage lockout (UVLO). The PTB48511 adds output over-voltage protection (OVP).

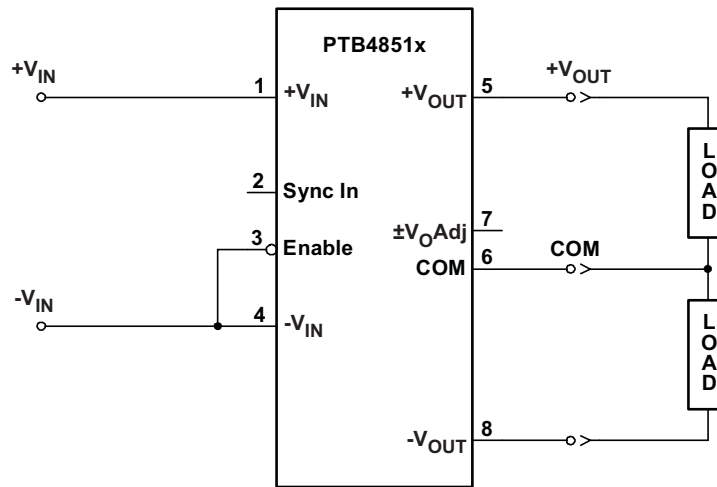
The control inputs, *Enable* and *Sync In*, are compatible with the *EN Out* and *Sync Out* signals of the PTB48500 DC/DC converter. This allows the power-up and switching frequency of the PTB4851x modules to be directly controlled from a PTB48500. Together the PTB48500 and PTB4851xA converters meet all the system power and sequencing requirements of the AC- ADSL chipset.

The PTB4851x uses double-sided surface mount technology construction. The package size is based on the industry standard outline and does not require a heatsink. Both through-hole and surface mount pin configurations are available.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

STAND-ALONE APPLICATION



ORDERING INFORMATION

Base Part No. (PTB4851xxx)		Output Voltage (PTB4851xx)		Package Options (PT4851xx)		
Order Prefix	Description	Code	Voltage	Code	Description	Pkg Ref. ⁽¹⁾
PTB48510xxx	Basic Model	A	±5 V	AH	Horiz. T/H	(ERK)
PTB48511xxx	Adds Output OVP ⁽²⁾	B	±12 V	AS	SMD, Standard ⁽³⁾	(ERL)
		C	±15 V ⁽⁴⁾			

- (1) Reference the applicable package reference drawing for the dimensions and PC board layout.
(2) Output Over-Voltage Protection
(3) *Standard* option specifies 63/37, Sn/Pb pin solder material.
(4) ±15-V output is not available with the PTB48511.

Environmental and General Specifications

(Unless otherwise stated, all voltages are with respect to $-V_{in}$)

			VALUE	UNIT
V_{in}	Input Voltage Range	Over output load range	36 to 75	VDC
	Isolation Voltage	Input-output/input/case	1500	V
	Capacitance	Input to output	1500	pF
	Resistance	Input to output	10	mΩ
T_A	Operating Temperature Range	Over V_{in} Range	−40 to 85	°C
OTP	Over-Temperature Protection	Shutdown threshold	115 ⁽¹⁾	°C
		Hysteresis	10	
T_{reflow}	Solder Reflow Temperature	Surface temperature of module body or pins	235 ⁽²⁾	°C
T_s	Storage Temperature		−40 to 125	°C
	Mechanical Shock	Per Mil-STD-883D, Method 2002.3 1 msec, 1/2 Sine, mounted	T/H 500	G's
			SMD 250	
	Mechanical Vibration Mil-STD-883D	Mil-STD-883D, Method 2007.2 20-2000 Hz	T/H 10	G's
			SMD 5	
	Weight		28	grams
	Flammability	Meets UL 94V-O		

- (1) This parameter is assured by design.
(2) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, $T_A = 25^\circ\text{C}$, $V_{in} = 48\text{ V}$, $C_{in} = 0\text{ }\mu\text{F}$, $\pm C_O = 0\text{ }\mu\text{F}$, $|+I_O| = |-I_O|$, and $|\pm I_O| = 0.5 |\pm I_{Omax}|$)

PARAMETER		TEST CONDITIONS	PTB4851xA			UNIT				
			MIN	TYP	MAX					
P _o	Output Power	Total output power from ±V _o	0	65 ⁽¹⁾		W				
±I _o	Output Current	Over V _{in} range, +I _o − − I _o ≤ 0.1 A	0	6.5 ⁽²⁾		A				
+I _o − −I _o	Output Load Imbalance	+I _o ≥0.1 A, −I _o ≥0.1 A	0	1 ⁽³⁾		A				
±V _o	Output Voltage	Includes set point, line, load, +I _o − − I _o ≤ 0.1 A, −40°C ≤ T _A ≤ 85°C	4.75 ⁽²⁾	5	5.25 ⁽²⁾	V				
ΔReg _{temp}	Temperature Variation	−40°C ≤ T _A ≤ 85°C, ±I _o = 0.1 A	+V _o	±1		%V _o				
			−V _o	±1						
ΔReg _{line}	Line Regulation	Over V _{in} range, balanced load	±V _o	±0.1	±0.4	%V _o				
ΔReg _{load}	Load Regulation	Over ±I _o range, balanced load	±V _o	±0.2	±0.4	%V _o				
η	Efficiency				86%					
V _r	V _o Ripple (pk-pk)	20 MHz bandwidth, C _o = 10 μF tantalum capacitor			20	30 ⁽⁴⁾	mV _{pp}			
t _{tr}	Transient Response	0.11 A/μs load step, 50% to 75% ±I _o max			30		μs			
ΔV _{tr}		±V _o over/undershoot			±1.0		%V _o			
I _o trip	Over Current Threshold	V _I = 36 V, reset followed by auto-recovery			6.8	7.5	10	A		
±V _o trip	Over Voltage Threshold	Outputs latched off ⁽⁵⁾	PTB48510	NA		NA		V		
			PTB48511	5.9		7				
	Short Circuit Current	Continuous over-current trip, +I _o = −I _o	±I _o I _{pk}	12.5				A		
			Duty	10%						
±V _o _{adj}	Output Voltage Adjust Range	+V _o and −V _o adjust simultaneously			3.5	5.5		V		
f _s	Switching Frequency	Over V _{in} and I _o ranges			440	470 ⁽⁶⁾	500	kHz		
V _{in} on	Under-Voltage Lockout	V _{in} increasing			33			V		
V _{in} off		V _{in} decreasing			32					
	On/Off Enable (pin 3)	Referenced to −V _{in} (pin 4)						V		
V _{IH}	Input High Voltage				3.6				75 ⁽⁷⁾	
V _{IL}	Input Low Voltage				−0.2				0.8	
I _{IL}	Input Low Current								−1	
I _{in} standby	Standby Input Current	Pin 3 connected			2			mA		
t _{on}	Start-up Time	±I _o = 1 A, ±V _o rising 0 to 0.95 ±V _o _{typ}			6	10	22	ms		
C _{in}	Internal Input Capacitance				3			μF		
±C _o	External Output Capacitance	Capacitance from either output to COM (pin 6)			0	5000 ⁽⁸⁾		μF		
MTBF	Reliability	Per Telcordia SR-332 50% stress, T _A = 40°C, ground benign	PTB48510A	2.7			10 ⁶ Hrs			
			PTB48511A	2.5						

- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
- (2) Under balanced load conditions, load current flowing out of $+V_O$ is balanced to within $\pm 0.1\text{ A}$ of that flowing into $-V_O$.
- (3) A load imbalance is the difference in current flowing from $+V_O$ to $-V_O$. The module can operate with a higher imbalance but with reduced specifications.
- (4) Output voltage ripple is measured with a $10\text{ }\mu\text{F}$ tantalum capacitor connected from $+V_O$ (pin 5) or $-V_O$ (pin 8), to COM (pin 6).
- (5) If the over-voltage threshold is exceeded by either regulated output the module will shut down, turning both outputs off. This is a latched condition, which can only be reset by removing and then re-applying the module's input power.
- (6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
- (7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to $+V_{in}$. The open-circuit voltage is 5 V max. If it is left open circuit the converter will operate when input power is applied.
- (8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

ELECTRICAL CHARACTERISTICS(Unless otherwise stated, $T_A = 25^\circ\text{C}$, $V_{in} = 48\text{ V}$, $C_{in} = 0\text{ }\mu\text{F}$, $\pm C_O = 0\text{ }\mu\text{F}$, $|+I_O| = |-I_O|$, and $|\pm I_O| = 0.5 |\pm I_O|_{\text{max}}$)

PARAMETER		TEST CONDITIONS	PTB4851xB			UNIT
			MIN	TYP	MAX	
P_O	Output Power	Total output power from $\pm V_O$	0		72 ⁽¹⁾	W
$ \pm I_O $	Output Current	Over V_{in} range, $ +I_O - -I_O \leq 0.1\text{ A}$	0		3 ⁽²⁾	A
$ +I_O - -I_O $	Output Load Imbalance	$ +I_O \geq 0.1\text{ A}$, $ -I_O \geq 0.1\text{ A}$	0		1 ⁽³⁾	A
$ \pm V_O $	Output Voltage	Includes set point, line, load, $ +I_O - -I_O \leq 0.1\text{ A}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	11.6 ⁽²⁾	12	12.4 ⁽²⁾	V
$\Delta\text{Reg}_{\text{temp}}$	Temperature Variation	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $ \pm I_O = 0.1\text{ A}$		± 1		% V_O
$\Delta\text{Reg}_{\text{line}}$	Line Regulation	Over V_{in} range, balanced load		± 0.05	± 0.5	% V_O
$\Delta\text{Reg}_{\text{load}}$	Load Regulation	Over $\pm I_O$ range, balanced load		± 0.1	± 1	% V_O
η	Efficiency			89%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, $C_O = 10\text{ }\mu\text{F}$ tantalum capacitor		20	80 ⁽⁴⁾	mV _{pp}
t_{tr}	Transient Response	0.1 A/ μs load step, 50% to 75% $\pm I_O$ max		30		μs
ΔV_{tr}		$ \pm V_O $ over/undershoot		± 1		% V_O
$I_{O\text{trip}}$	Over Current Threshold	$V_I = 36\text{ V}$, reset followed by auto-recovery	3.3	3.8	5	A
$ \pm V_O _{\text{trip}}$	Over Voltage Threshold	Outputs latched off ⁽⁵⁾	PTB48510A	NA	NA	V
			PTB48511A	14	15.8	
	Short Circuit Current	Continuous over-current trip, $ +I_O = -I_O $	$ \pm I_O _{pk}$		6	A
			Duty		10%	
$ \pm V_O _{\text{adj}}$	Output Voltage Adjust Range	$ +V_O $ and $ -V_O $ adjust simultaneously	6.5		13.4	V
f_S	Switching Frequency	Over V_{in} and I_O ranges	440	480 ⁽⁶⁾	500	kHz
$V_{in\text{ on}}$	Under-Voltage Lockout	V_{in} increasing		33		V
$V_{in\text{ off}}$		V_{in} decreasing		32		
	On/Off Enable (pin 3)	Referenced to $-V_{in}$ (pin 4)				
V_{IH}	Input High Voltage		3.6		75 ⁽⁷⁾	V
V_{IL}	Input Low Voltage		-0.2		0.8	
I_{IL}	Input Low Current				-1	
$I_{in\text{ standby}}$	Standby Input Current	Pin 3 open circuit		2		mA
t_{on}	Start-up Time	$ \pm I_O = 1\text{ A}$, $ \pm V_O $ rising 0 to 0.95 $ \pm V_O _{\text{typ}}$	6	12	18	ms
C_{in}	Internal Input Capacitance			3		μF
$\pm C_O$	External Output Capacitance	Capacitance from either output to COM (pin 6)	0		3000 ⁽⁸⁾	μF
MTBF	Reliability	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$, ground benign	PTB48510B	2.8		10^6 Hrs
			PTB48511B	2.5		

- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
- (2) Under balanced load conditions, load current flowing out of $+V_O$ is balanced to within $\pm 0.1\text{ A}$ of that flowing into $-V_O$.
- (3) A load imbalance is the difference in current flowing from $+V_O$ to $-V_O$. The module can operate with a higher imbalance but with reduced specifications.
- (4) Output voltage ripple is measured with a $10\text{ }\mu\text{F}$ tantalum capacitor connected from $+V_O$ (pin 5) or $-V_O$ (pin 8), to COM (pin 6).
- (5) If the over-voltage threshold is exceeded by either regulated output the module will shut down, turning both outputs off. This is a latched condition, which can only be reset by removing and then re-applying the module's input power.
- (6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
- (7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to $+V_{in}$. The open-circuit voltage is 5 V max. If it is left open circuit the converter will operate when input power is applied.
- (8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, $T_A = 25^\circ\text{C}$, $V_{in} = 48\text{ V}$, $C_{in} = 0\text{ }\mu\text{F}$, $\pm C_O = 0\text{ }\mu\text{F}$, $|+I_O| = |-I_O|$, and $|\pm I_O| = 0.5 |\pm I_O|_{\text{max}}$)

PARAMETER		TEST CONDITIONS	PTB4851xB			UNIT
			MIN	TYP	MAX	
P_O	Output Power	Total output power from $\pm V_O$	0		66 ⁽¹⁾	W
$ \pm I_O $	Output Current	Over V_{in} range, $ +I_O - -I_O \leq 0.1\text{ A}$	0		2.2 ⁽²⁾	A
$ +I_O - -I_O $	Output Load Imbalance	$ +I_O \geq 0.1\text{ A}$, $ -I_O \geq 0.1\text{ A}$	0		1 ⁽³⁾	A
$ \pm V_O $	Output Voltage	Includes set point, line, load, $ +I_O - -I_O \leq 0.1\text{ A}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	14.5 ⁽²⁾	15	15.5 ⁽²⁾	V
$\Delta\text{Reg}_{\text{temp}}$	Temperature Variation	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $ \pm I_O = 0.1\text{ A}$		± 1		% V_O
$\Delta\text{Reg}_{\text{line}}$	Line Regulation	Over V_{in} range, balanced load		± 0.05	± 0.5	% V_O
$\Delta\text{Reg}_{\text{load}}$	Load Regulation	Over $\pm I_O$ range, balanced load		± 0.1	± 1	% V_O
η	Efficiency	$ \pm I_O = \pm I_O _{\text{max}}$		90%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, $C_O = 10\text{ }\mu\text{F}$ tantalum capacitor		50	100 ⁽⁴⁾	mV _{pp}
t_{tr}	Transient Response	0.1 A/ μs load step, 50% to 75% $\pm I_O$ max		30		μs
ΔV_{tr}		$ \pm V_O $ over/undershoot		± 1		% V_O
$I_{O\text{trip}}$	Over Current Threshold	$V_I = 36\text{ V}$, reset followed by auto-recovery	2.45	3	3.85	A
	Short Circuit Current	Continuous over-current trip, $ +I_O = -I_O $		$ \pm I_O _{pk}$	4.5	A
				Duty	10%	
$ \pm V_O _{\text{adj}}$	Output Voltage Adjust Range	$ +V_O $ and $ -V_O $ adjust simultaneously	7.2		16.7	V
f_S	Switching Frequency	Over V_{in} and I_O ranges	440	480 ⁽⁵⁾	520	kHz
$V_{in\text{ on}}$	Under-Voltage Lockout	V_{in} increasing		33		V
$V_{in\text{ off}}$		V_{in} decreasing		32		
	On/Off Enable (pin 3)	Referenced to $-V_{in}$ (pin 4)				V
V_{IH}	Input High Voltage		3.6		75 ⁽⁶⁾	
V_{IL}	Input Low Voltage		-0.2		0.8	
I_{IL}	Input Low Current				-1	mA
$I_{in\text{ standby}}$	Standby Input Current	Pin 3 open circuit		2		mA
t_{on}	Start-up Time	$ \pm I_O = 1\text{ A}$, $ \pm V_O $ rising 0 to 0.95 $ \pm V_O _{\text{typ}}$	6	12	18	ms
C_{in}	Internal Input Capacitance			3		μF
$\pm C_O$	External Output Capacitance	Capacitance from either output to COM (pin 6)	0		3000 ⁽⁷⁾	μF
MTBF	Reliability	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$, ground benign	2.8			10 ⁶ Hrs

- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
- (2) Under balanced load conditions, load current flowing out of $+V_O$ is balanced to flowing into $-V_O$.
- (3) A load imbalance is the difference in current flowing from $+V_O$ to $-V_O$. The module can operate with a higher imbalance but with reduced specifications.
- (4) Output voltage ripple is measured with a 10 μF tantalum capacitor connected from $+V_O$ (pin 5) or $-V_O$ (pin 8), to COM (pin 6).
- (5) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
- (6) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to $+V_{in}$. The open-circuit voltage is 5 V max. If it is left open circuit the converter will operate when input power is applied.
- (7) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
+Vin ⁽¹⁾	1	The positive input supply for the module with respect to $-V_{in}$. When powering the module from a -48 V telecom central office supply, this input is connected to the primary system ground.
Sync In	2	This pin is used when the PTB4851x and PTB4850x DC/DC converter modules are used together. Connecting this pin to the <i>Sync Out</i> of the PTB4850x module allows the PTB4851x to be synchronized to the same switch conversion frequency as the PTB4850x.
Enable ⁽²⁾	3	This is an open-collector (open-drain) negative logic input that enables the module output. This pin is referenced to $-V_{in}$. A logic 0 at this pin enables the module's outputs, and a high impedance disables the outputs. If this feature is not used the pin should be connected to $-V_{in}$. Note: Connecting this input directly to the <i>EN Out</i> pin of the PTB4850x enables the output voltages from both converters (PTB4850x and PTB4851x) to power up in sequence.
$-V_{in}$	4	The negative input supply for the module, and the 0 VDC reference for the <i>Enable</i> , ⁽³⁾ and <i>Sync In</i> signals. When the module is powered from a $+48\text{-V}$ supply, this input is connected to the 48-V Return.
+Vout	5	The positive output supply voltage, which is referenced to the <i>COM</i> node. The voltage at +Vout has the same magnitude, but is the complement to that at $-V_{out}$.
$-V_{out}$	8	The negative output supply voltage, which is referenced to the <i>COM</i> node. The voltage at $-V_{out}$ has the same magnitude, but is the complement to that at +Vout.
COM	6	The secondary return reference for the module's regulated output voltages. This node is dc isolated from the input supply pins.
$\pm V_o$ Adjust	7	Using a single resistor, this pin allows the magnitude of both +Vout and $-V_{out}$ to be adjusted together, either higher or lower than their preset value. If not used, this pin should be left open circuit.

(1) Shaded functions indicate signals that are referenced to $-V_{in}$.

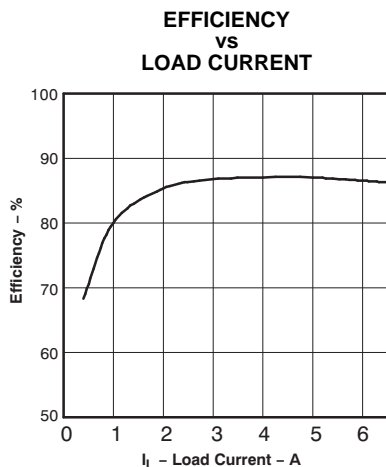
(2) Denotes negative logic: Open = Output Off, $-V_{in}$ = Normal operation

(3) Denotes negative logic: Open = Output Off, $-V_{in}$ = Normal operation

TYPICAL CHARACTERISTICS

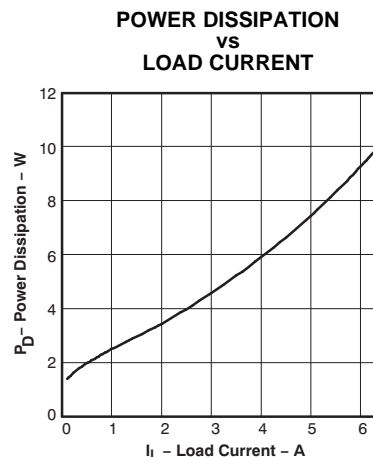
PTB4851xA CHARACTERISTIC DATA at $V_{IN} = 48\text{ V}$

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.



- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 1.



- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 2.

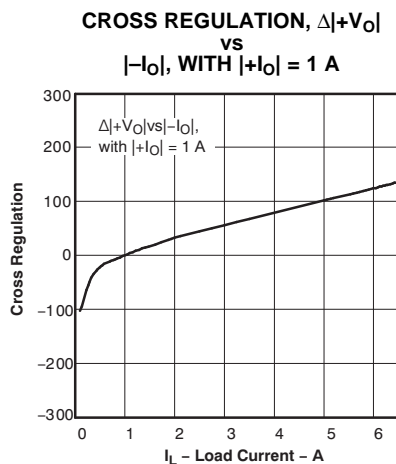


Figure 3.

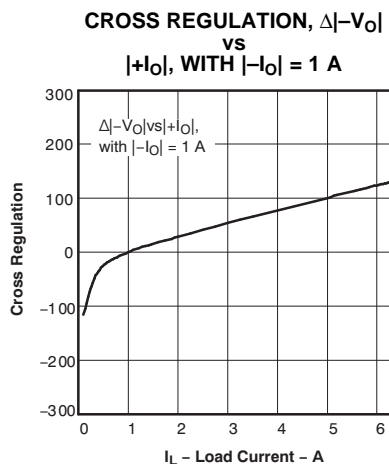


Figure 4.

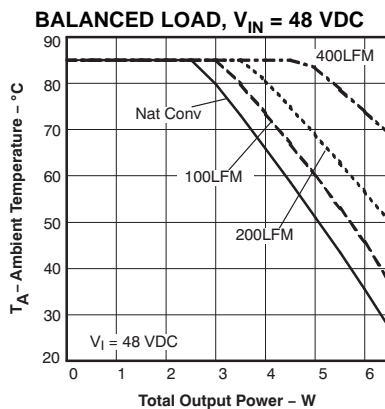
SAFE OPERATING AREA PTB4851xA

SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating

TYPICAL CHARACTERISTICS (continued)

SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.



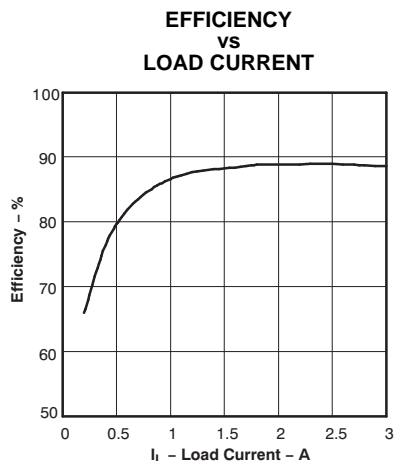
- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 5.

TYPICAL CHARACTERISTICS (Continued)

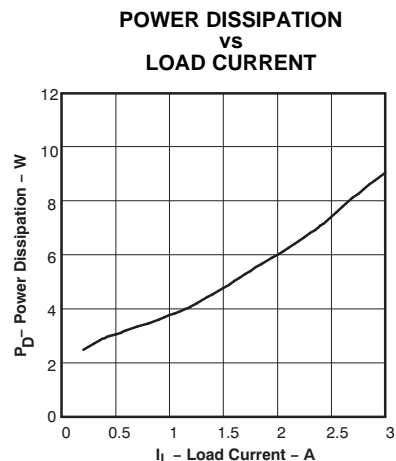
PTB4851xB CHARACTERISTIC DATA at $V_{IN} = 48\text{ V}$

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.



- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 6.



- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 7.

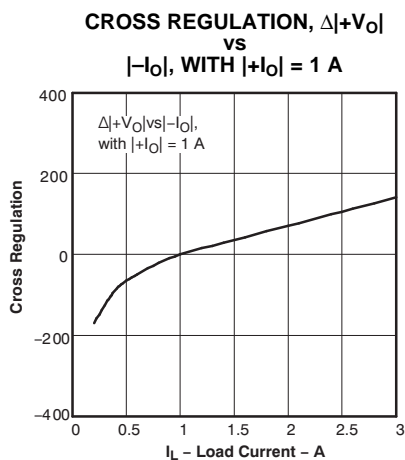


Figure 8.

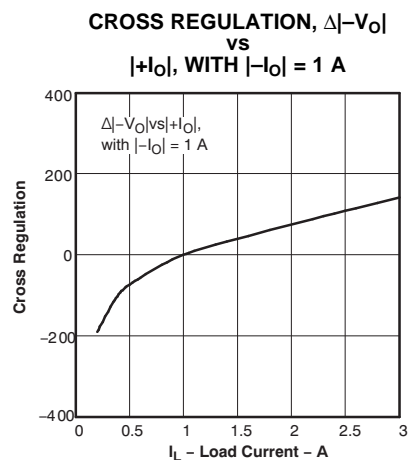


Figure 9.

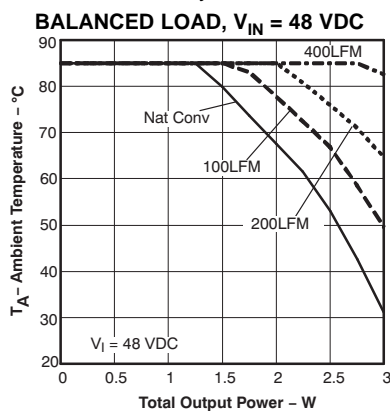
SAFE OPERATING AREA PTB4851xB

SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating

TYPICAL CHARACTERISTICS (Continued) (continued)

SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.



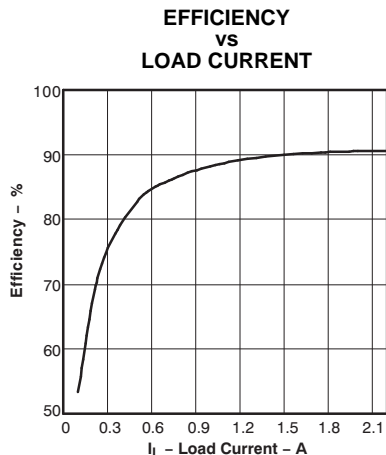
- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 10.

TYPICAL CHARACTERISTICS (Continued)

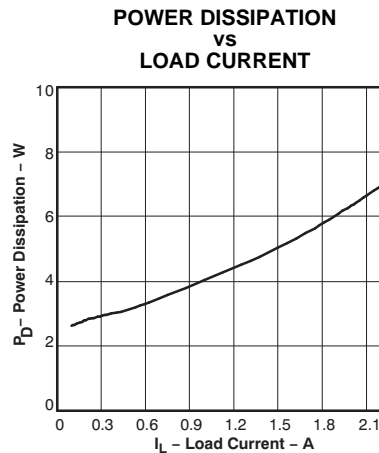
PTB48502A CHARACTERISTIC DATA at $V_{IN} = 48\text{ V}$

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.



- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 11.



- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 12.

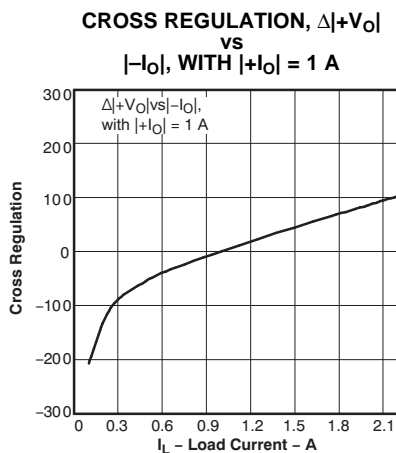


Figure 13.

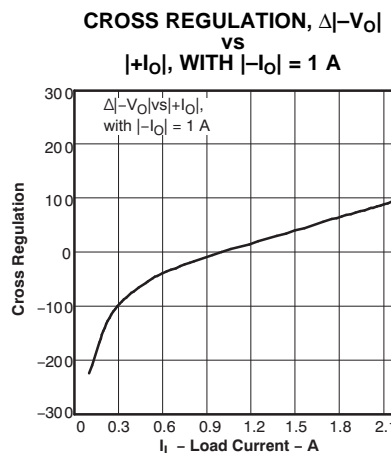


Figure 14.

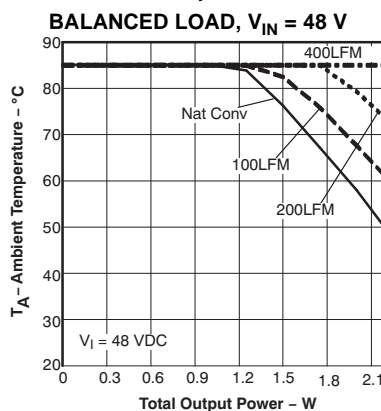
SAFE OPERATING AREA PTB48510C

SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating

TYPICAL CHARACTERISTICS (Continued) (continued)

SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.



- A. Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.

Figure 15.

APPLICATION INFORMATION

ADJUSTING THE LOWER OUTPUT VOLTAGE OF THE PTB4850X SERIES OF DC/DC CONVERTERS

The PTB48510 and PTB48511 DC/DC converters produce a balanced pair of complimentary output voltages. They are identified $+V_{OUT}$ and $-V_{OUT}$, respectively. The magnitude of both output voltages can be adjusted together as a pair, higher or lower, by up to $\pm 10\%$ of their nominal. The adjustment method uses a single external resistor.¹ The value of the resistor determines the adjustment magnitude, and its placement determines whether the magnitude is increased or decreased. The resistor values can be calculated using the appropriate formula (see below). The formula constants are given in Table 1. The placement of each resistor is as follows.

Adjust Up:³ To increase the magnitude of both output voltages, place a resistor R_1 between $\pm V_{OAdj}$ (pin 7) and the $-V_{OUT}$ (pin 8) voltage rail; see Figure 16.

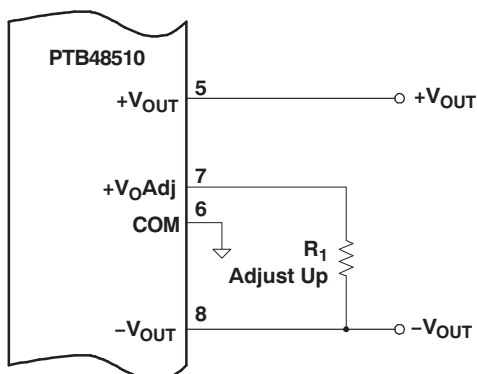


Figure 16. TITLE??

Adjust Down: To decrease the magnitude of both output voltages, add a resistor (R_2), between V_{OAdj} (pin 7) and the $+V_{OUT}$ (pin 5) voltage rail; see Figure 17.

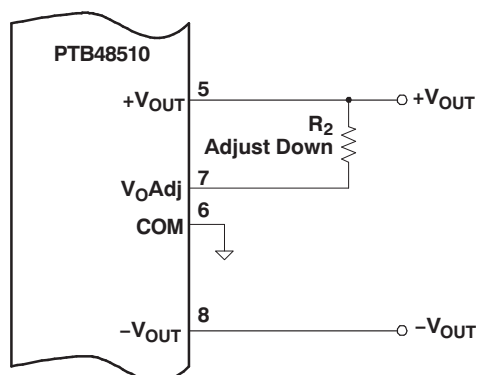


Figure 17. TITLE??

CALCULATION OF RESISTOR ADJUST VALUES

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R_1 to adjust up, or (R_2) to adjust down.

$$R_1 [\text{Adjust Up}] = \frac{V_r R_o}{2(V_a - V_o)} - R_s \text{ k}\Omega \quad (1)$$

$$(R_2) [\text{Adjust Down}] = \frac{R_o(2V_a - V_r)}{2(V_o - V_a)} - R_s \text{ k}\Omega \quad (2)$$

Where:

V_o = Magnitude of the original $\pm V_{OUT}$

V_a = Magnitude of the adjusted voltage

V_r = The reference voltage from Table 1

R_o = The resistance value in Table 1

R_s = The series resistance from Table 1

Table 1. Adjustment Range and Formula Parameters

Series Part No.	PTB4851xA	PTB4851xB	PTB48510C
$V_o(\text{nom})$	5 V	1.2 V	15 V
$V_a(\text{min})$	3.5 V	6.5 V	7.2 V
$V_a(\text{max})$	5.5 V	13.4 V	16.7V
V_r	2.495 V	2.495 V	2.495 V
$R_n \text{ (k}\Omega\text{)}$	7.5	18.2	22.1
$R_s \text{ (k}\Omega\text{)}$	9.09	16.9	16.9

NOTES:

1. A 0.05 W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/ $^{\circ}\text{C}$ or better. Place the resistor in either the R_1 or (R_2) location, as close to the converter as possible.
2. Never connect capacitors to the $\pm V_{OAdj}$ pin. Capacitance added to this pin can affect the stability of the regulated output.
3. **The over-voltage protection (PTB48511x)** is nominally set to 25% above the original output voltage set-point. Increasing the magnitude of the output voltages reduces the margin between the output voltage and the overvoltage (OV) protection threshold. This could make the module more sensitive to OV faults, as a result of random noise and load transients.

Note: An OV fault is a latched condition that shuts down the converter's outputs. The fault can only be cleared by cycling the Enable pin, or by momentarily removing input power to the module.o

CONFIGURING THE PTB4850x and PTB4851x DC/DC CONVERTERS FOR DSL APPLICATIONS

When operated as a pair, the PTB4850x and PTB4851x converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB4851x produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB4851x may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. [Figure 19](#) shows the required cross-connects between the two converters to enable these two features.

SWITCHING FREQUENCY SYNCHRONIZATION

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

POWER-UP SEQUENCING

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be assured if the PTB4850x and PTB4851x are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the *EN Out* pin of the PTB4850x is directly connected to the activelow *Enable* input of the PTB4851x (see [Figure 19](#)). This allows the PTB4850x to momentarily hold off the outputs from the PTB4851x until the logic-level voltages have risen first. [Figure 19](#) shows the power-up waveforms of all four supply voltages from the schematic of [Figure 19](#).

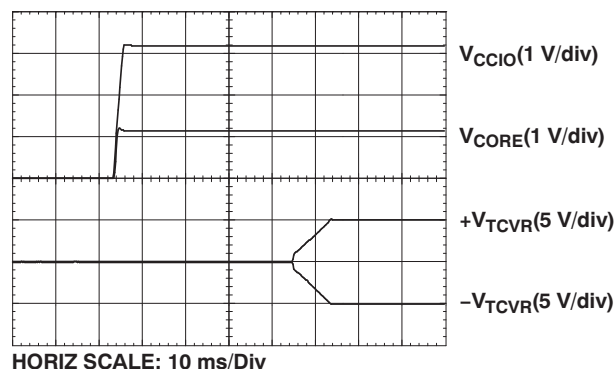


Figure 18. Power-Up Sequencing Waveforms

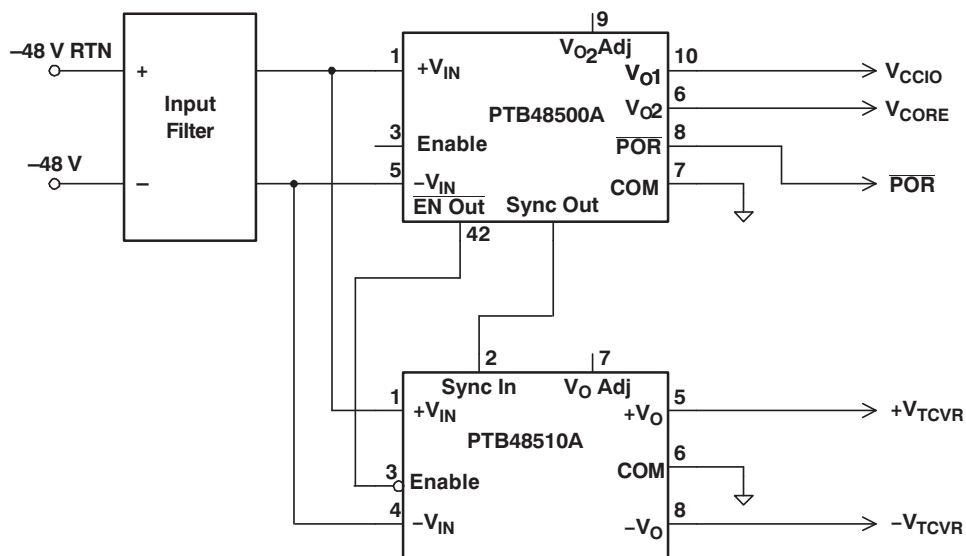


Figure 19. Example of PTB4850x and PTB4851x Modules Configured for DSL Applications

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PTB48510AAH	ACTIVE	DIP MOD ULE	ERK	8	9	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTB48510AAS	ACTIVE	DIP MOD ULE	ERL	8	9	TBD	Call TI	Level-1-235C-UNLIM
PTB48510AAZ	ACTIVE	DIP MOD ULE	BRL	8	9	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR
PTB48510BAH	ACTIVE	DIP MOD ULE	ERK	8	9	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTB48510BAS	ACTIVE	DIP MOD ULE	ERL	8	9	TBD	Call TI	Level-1-235C-UNLIM
PTB48510BAZ	ACTIVE	DIP MOD ULE	ERL	8	9	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR
PTB48510CAH	ACTIVE	DIP MOD ULE	ERK	8	9	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTB48510CAS	ACTIVE	DIP MOD ULE	ERL	8	9	TBD	Call TI	Level-1-235C-UNLIM
PTB48510CAZ	ACTIVE	DIP MOD ULE	ERL	8	9	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR
PTB48511AAH	ACTIVE	DIP MOD ULE	ERK	8	9	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTB48511AAS	ACTIVE	DIP MOD ULE	ERL	8	9	TBD	Call TI	Level-1-235C-UNLIM
PTB48511AAZ	ACTIVE	DIP MOD ULE	ERL	8	9	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR
PTB48511BAH	ACTIVE	DIP MOD ULE	ERK	8	9	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTB48511BAS	ACTIVE	DIP MOD ULE	ERL	8	9	TBD	Call TI	Level-1-235C-UNLIM
PTB48511BAZ	ACTIVE	DIP MOD ULE	ERL	8	9	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

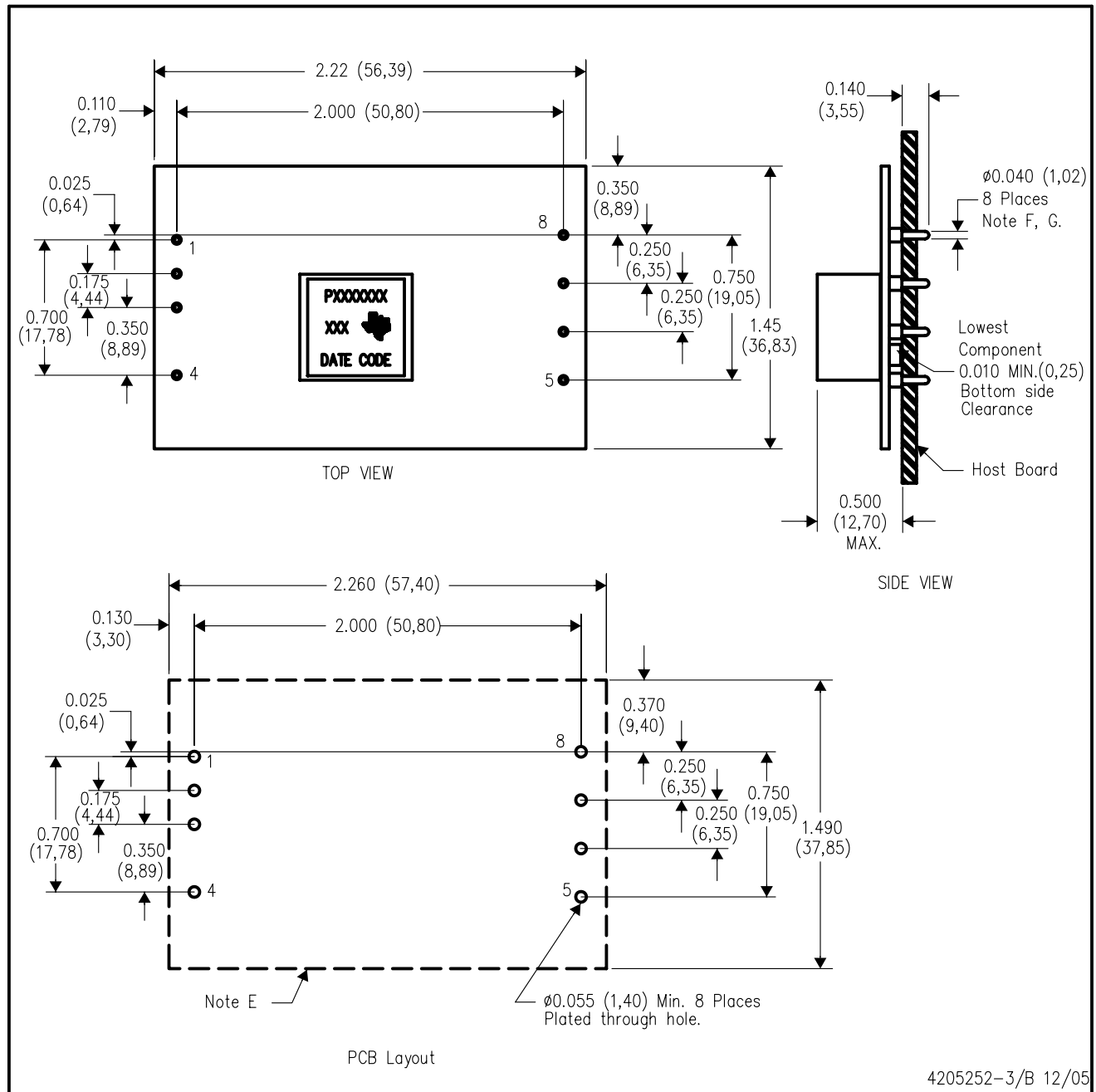
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ERK (R-PDSS-T8)

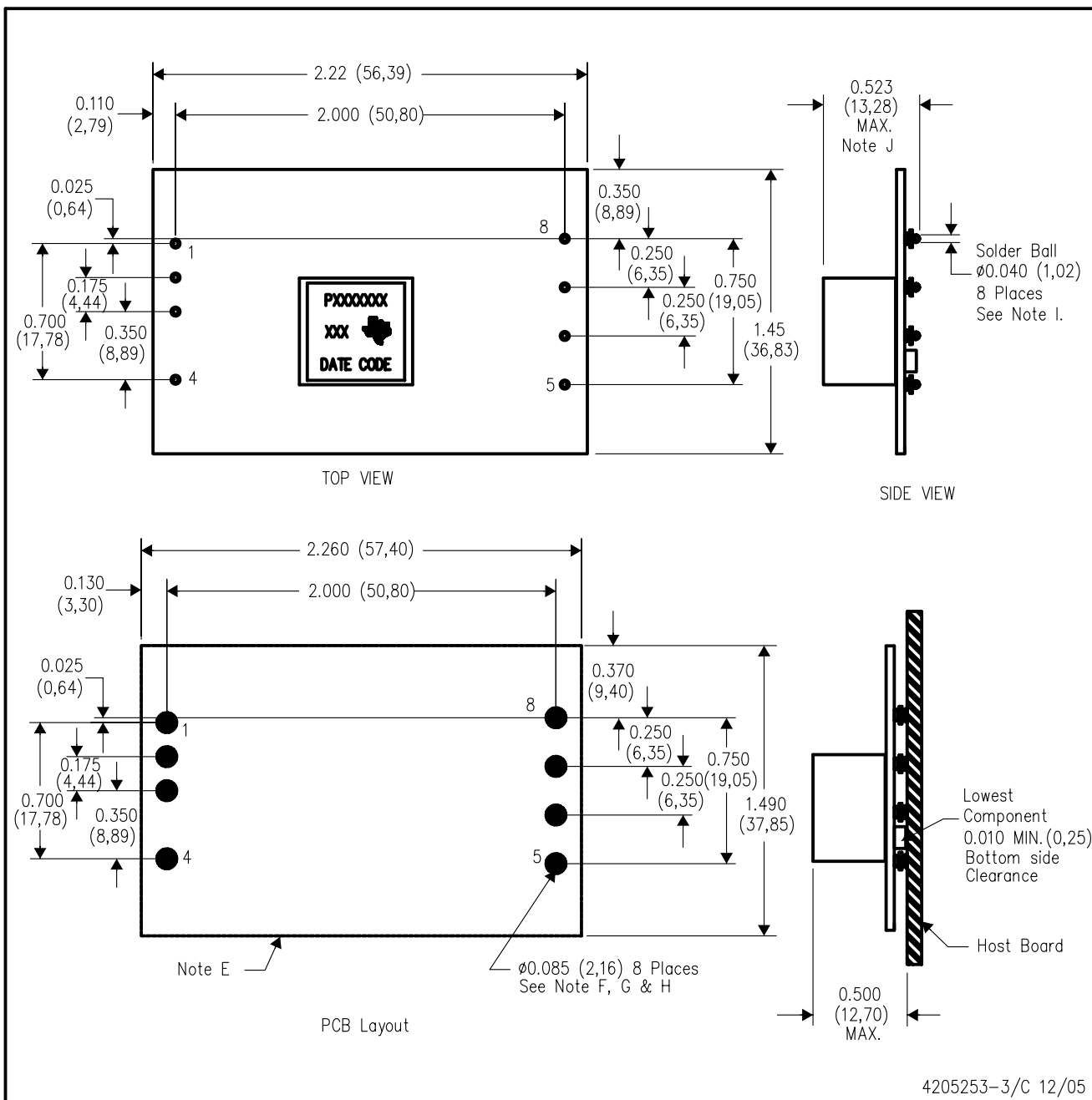
DOUBLE SIDED MODULE



4205252-3/B 12/05

ERL (R-PDSS-B8)

DOUBLE SIDED MODULE



- NOTES:
- | | |
|--|--|
| A. All linear dimensions are in inches (mm). | G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16).
Paste screen thickness: 0.006 (0,15). |
| B. This drawing is subject to change without notice. | H. Pad type: Solder mask defined. |
| C. 2 place decimals are ± 0.020 ($\pm 0,51\text{mm}$). | I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet. |
| D. 3 place decimals are ± 0.010 ($\pm 0,25\text{mm}$). | J. Dimension prior to reflow solder. |
| E. Recommended keep out area for user components. | |
| F. Power pin connection should utilize four or more vias
to the interior power plane of 0.025 (0,63) I.D. per input,
ground and output pin (or the electrical equivalent). | |

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