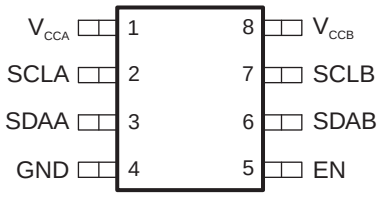
LEVEL-TRANSLATING I²C BUS REPEATER

Check for Samples: PCA9517

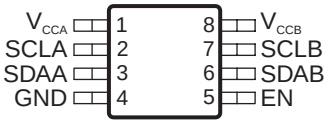
FEATURES

- **Two-Channel Bidirectional Buffer**
- **I²C Bus and SMBus Compatible**
- **Operating Supply Voltage Range of 0.9 V to 5.5 V on A Side**
- **Operating Supply Voltage Range of 2.7 V to 5.5 V on B Side**
- **Voltage-Level Translation From 0.9 V to 5.5 V and 2.7 V to 5.5 V**
- **Footprint and Function Replacement for PCA9515A**
- **Active-High Repeater-Enable Input**
- **Open-Drain I²C I/O**
- **5.5-V Tolerant I²C and Enable Input Support**
- **Mixed-Mode Signal Operation**
- **Lockup-Free Operation**
- **Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters**
- **Powered-Off High-Impedance I²C Pins**
- **400-kHz Fast I²C Bus**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

D PACKAGE
(TOP VIEW)



DGK PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This dual bidirectional I²C buffer is operational at 2.7 V to 5.5 V.

The PCA9517 is a BiCMOS integrated circuit intended for I²C bus and SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The PCA9517 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing two buses of 400-pF bus capacitance to be connected in an I²C application. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The PCA9517 has two types of drivers—A-side drivers and B-side drivers. All inputs and I/Os are overvoltage tolerant to 5.5 V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V).

ORDERING INFORMATION

T_A	PACKAGES(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tape and reel	PCA9517DR	PD517
	MSOP – DGK	Tape and reel	PCA9517DGKR	7E_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The B-side drivers operate from 2.7 V to 5.5 V and behave like the drivers in the PCA9515A. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released.

This type of design on the B side prevents it from being used in series with the PCA9515A and another PCA9517 (B side). This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

The A-side drivers operate from 0.9 V to 5.5 V and drive more current. They do not require the buffered low feature (or the static offset voltage). This means that a low signal on the B side translates to a nearly 0-V low on the A side, which accommodates smaller voltage swings of lower-voltage logic. The output pulldown on the A side drives a hard low, and the input level is set at 0.3 V_{CCA} to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.9 V.

The A side of two or more PCA9517s can be connected together to allow a star topography, with the A side on the common bus. Also, the A side can be connected directly to any other buffer with static- or dynamic-offset voltage. Multiple PCA9517s can be connected in series, A side to B side, with no buildup in offset voltage and with only time-of-flight delays to consider.

The PCA9517 drivers are enabled when V_{CCA} is above 0.8 V and V_{CCB} is above 2.5 V.

The PCA9517 has an active-high enable (EN) input with an internal pullup to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It should never change state during an I^2C operation, because disabling during a bus operation hangs the bus, and enabling part way through a bus cycle could confuse the I^2C parts being enabled. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

The PCA9517 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. V_{CCB} and V_{CCA} can be applied in any sequence at power up. After power up and with the EN high, a low level on the A side (below 0.3 V_{CCA}) turns the corresponding B-side driver (either SDA or SCL) on and drives the B side down to approximately 0.5 V. When the A side rises above 0.3 V_{CCA}, the B-side pulldown driver is turned off and the external pullup resistor pulls the pin high. When the B side falls first and goes below 0.3 V_{CCB}, the A-side driver is turned on and the A side pulls down to 0 V. The B-side pulldown is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above 0.7 V_{CCB}. If the B-side low voltage goes below 0.4 V, the B-side pulldown driver is enabled, and the B side is able to rise to only 0.5 V until the A side rises above 0.3 V_{CCA}. Then the B side continues to rise, being pulled up by the external pullup resistor. V_{CCA} is only used to provide the 0.3 V_{CCA} reference to the A-side input comparators and for the power-good-detect circuit. The PCA9517 logic and all I/Os are powered by the V_{CCB} pin.

As with the standard I^2C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The PCA9517 has standard open-collector configuration of the I^2C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode and Fast mode I^2C devices in addition to SMBus devices. Standard mode I^2C devices only specify 3 mA in a generic I^2C system, where Standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

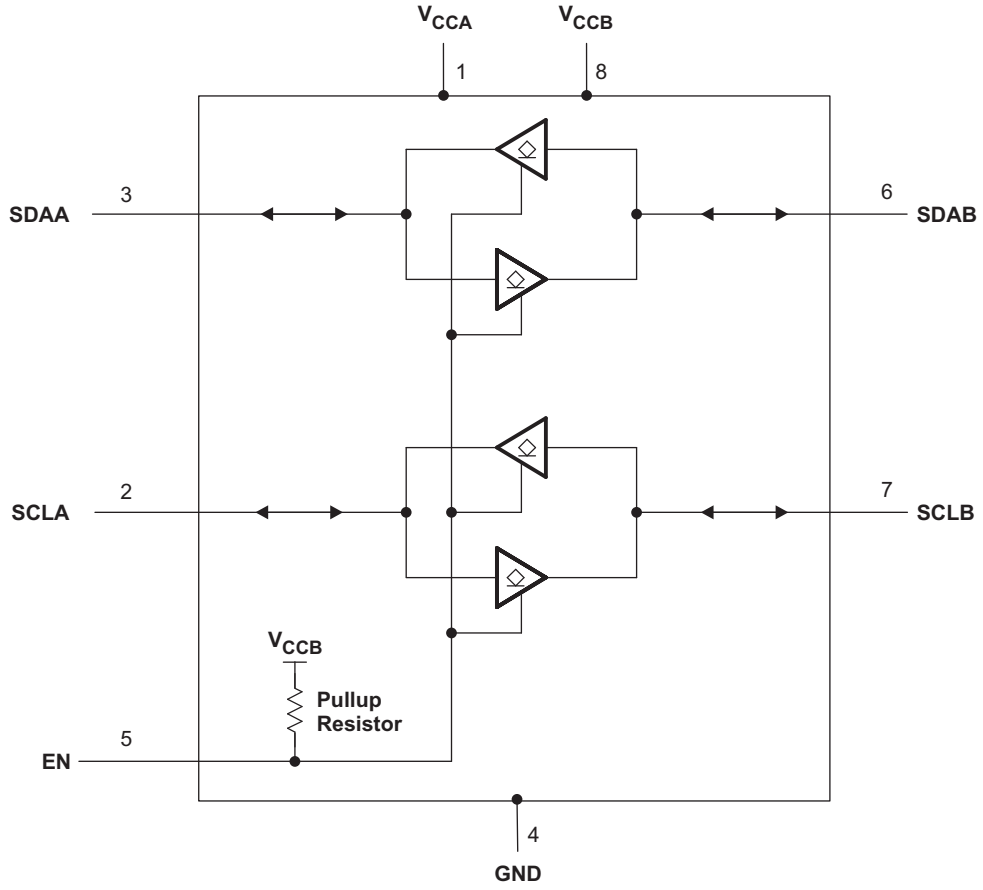
TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	V_{CCA}	A-side supply voltage (0.9 V to 5.5 V)
2	SCLA	Serial clock bus, A side. Connect to V_{CCA} through a pullup resistor.
3	SDAA	Serial data bus, A side. Connect to V_{CCA} through a pullup resistor.
4	GND	Supply ground
5	EN	Active-high repeater enable input
6	SDAB	Serial data bus, B side. Connect to V_{CCB} through a pullup resistor.
7	SCLB	Serial clock bus, B side. Connect to V_{CCB} through a pullup resistor.
8	V_{CCB}	B-side and device supply voltage (2.7 V to 5.5 V)

Table 1. FUNCTION TABLE

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

Figure 1. FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	7	V
V_{CCA}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL IMPEDANCE

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
θ_{JA}	Package thermal impedance(1)	D package		97	°C/W
		DGK package		172	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9(1)	5.5	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	$0.7 \times V_{CCA}$	5.5	V
		SDAB, SCLB	$0.7 \times V_{CCB}$	5.5	V
		EN	$0.7 \times V_{CCB}$	5.5	V
V_{IL}	Low-level input voltage	SDAA, SCLA	–0.5	$0.28 \times V_{CCA}$	V
		SDAB, SCLB	–0.5(2)	$0.3 \times V_{CCB}$	V
		EN	–0.5	$0.3 \times V_{CCB}$	V
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		6	mA
		V_{CCB} = 3 V		6	mA
T_A	Operating free-air temperature		–40	85	°C

(1) Low-level supply voltage
(2) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines.

ELECTRICAL CHARACTERISTICS

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	2.7 V to 5.5 V			–1.2	V
V_{OL}	Low-level output voltage	SDAB, SCLB	I_{OL} = 100 µA or 6 mA, V_{ILA} = V_{ILB} = 0 V	2.7 V to 5.5 V	0.45	0.52	0.7	V
		SDAA, SCLA	I_{OL} = 6 mA			0.1	0.2	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SDAB, SCLB		2.7 V to 5.5 V			70	mV
V_{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB		2.7 V to 5.5 V	–0.5	0.4		V
I_{CC}	Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I_{CC}	Quiescent supply current		Both channels high, SDAA = SCLA = V_{CCA} and SDAB = SCLB = V_{CCB} and EN = V_{CCB}	5.5 V		1.5	4	mA
			Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND			1.5	5	
			In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			1.5	5	
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.7 V to 5.5 V			±1	µA
			V_I = 0.2 V				10	
		SDAA, SCLA	V_I = V_{CCB}				±1	
			V_I = 0.2 V				10	
		EN	V_I = V_{CCB}				±1	
			V_I = 0.2 V			–10	–30	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V	2.7 V to 5.5 V			10	µA
		SDAA, SCLA					10	
C_I	Input capacitance	EN	V_I = 3 V or 0 V	3.3 V		6	7	pF
		SCLA, SCLB	V_I = 3 V or 0 V	3.3 V		6	9	
				0 V		6	8	
C_{IO}	Input/output capacitance	SDAA, SDAB	V_I = 3 V or 0 V	3.3 V		6	9	pF
				0 V		6	8	

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

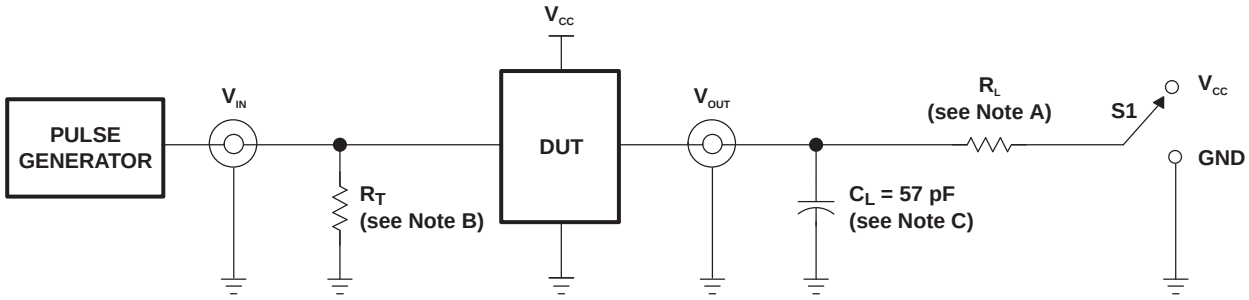
I²C INTERFACE TIMING REQUIREMENTS

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLZ}	Propagation delay		SDAB, SCLB(2) (see Figure 5)	SDAA, SCLA(2) (see Figure 5)		100	169	255	ns
			SDAA, SCLA(3) (see Figure 4)	SDAB, SCLB(3) (see Figure 4)		25	67	110	
t_{PZL}	Propagation delay		SDAB, SCLB	SDAA, SCLA	$V_{CCA} \le 2.7$ V (see Figure 3)	15	68(4)	110	ns
					2.7 V ≤ V_{CCA} ≤ 3 V (see Figure 3)	20	79	130	
					$V_{CCA} \ge 3$ V (see Figure 3)	10	103(5)	300	
			SDAA, SCLA(3) (see Figure 4)	SDAB, SCLB(3) (see Figure 4)		45	118	230	
t_{TLH}	Transition time	B side to A side (see Figure 4)	20%	80%		1	6	30	ns
		A side to B side (see Figure 3)				20	31	170	
t_{THL}	Transition time	B side to A side	80%	20%	$V_{CCA} \le 2.7$ V (see Figure 4)	1	3(4)	105	ns
					2.7 V ≤ V_{CCA} ≤ 3 V (see Figure 2)	1	6	120	
					$V_{CCA} \ge 3$ V (see Figure 4)	1	25(5)	175	
		A side to B side (see Figure 3)				1	12	90	

(1) Typical values were measured with $V_{CCA} = V_{CCB} = 2.7$ V at $T_A = 25°C$, unless otherwise noted.
(2) The t_{PLH} delay data from B to A side is measured at 0.5 V on the B side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
(3) The proportional delay data from A to B side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B side.
(4) Typical value measured with $V_{CCA} = 0.9$ V at $T_A = 25°C$
(5) Typical value measured with $V_{CCA} = 5.5$ V at $T_A = 25°C$

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

A. R_L = 167 Ω on the A side and 1.35 kΩ on the B side

B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

C. C_L includes probe and jig capacitance.

D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

E. The outputs are measured one at a time, with one transition per measurement.

F. t_{PLH} and t_{PHL} are the same as t_{pd}.

G. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

H. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 2. Test Circuit

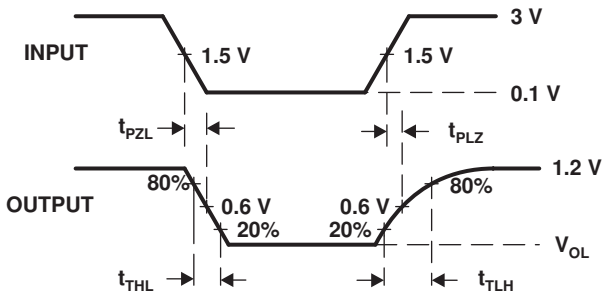


Figure 3. Waveform 1 – Propagation Delay and Transition Times for B Side to A Side

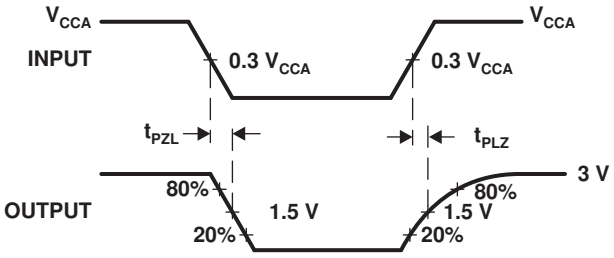


Figure 4. Waveform 2 – Propagation Delay and Transition Times for A Side to B Side

PARAMETER MEASUREMENT INFORMATION (continued)

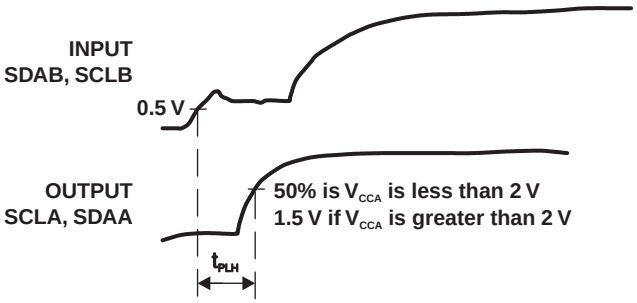


Figure 5. Waveform 3

APPLICATION INFORMATION

A typical application is shown in Figure 6. In this example, the system master is running on a 3.3-V I^2C bus, and the slave is connected to a 1.2-V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The PCA9517 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the A side of the PCA9517 is pulled low by a driver on the I^2C bus, a comparator detects the falling edge when it goes below 0.3 V_{CCA} and causes the internal driver on the B side to turn on, causing the B side to pull down to about 0.5 V. When the B side of the PCA9517 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 8 and Figure 9. If the bus master in Figure 6 were to write to the slave through the PCA9517, waveforms shown in Figure 8 would be observed on the A bus. This looks like a normal I^2C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the PCA9517, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9517. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the PCA9517 for a short delay, while the A-bus side rises above 0.3 V_{CCA} and then continues high.

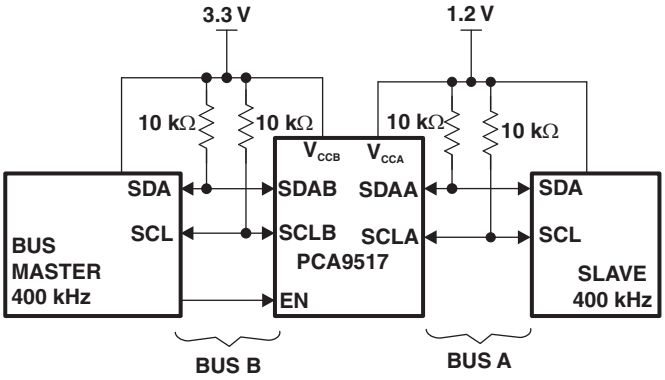


Figure 6. Typical Application

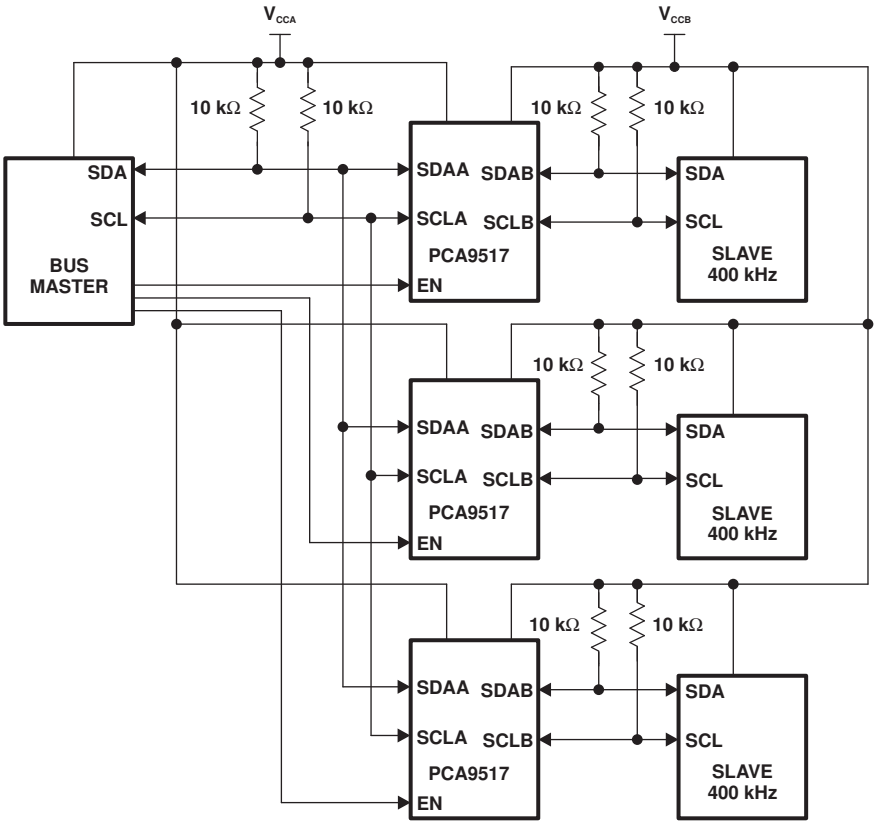


Figure 7. Typical Star Application

Multiple PCA9517 A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

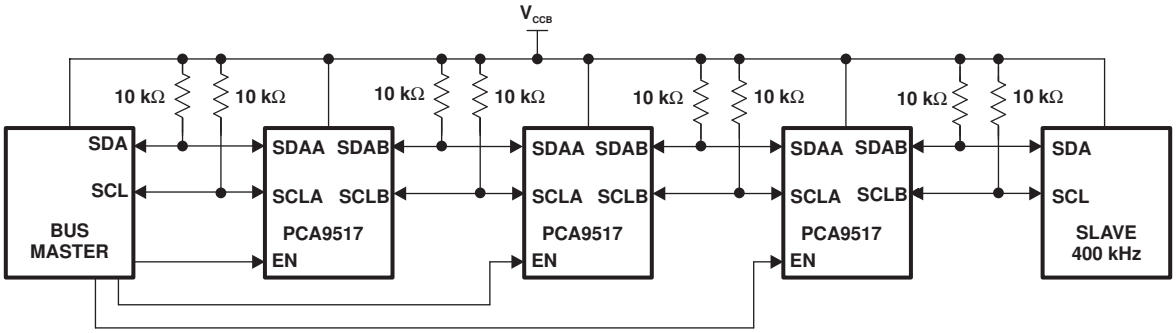


Figure 8. Typical Series Application

Multiple PCA9517s can be connected in series as long as the A side is connected to the B side. I^2C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

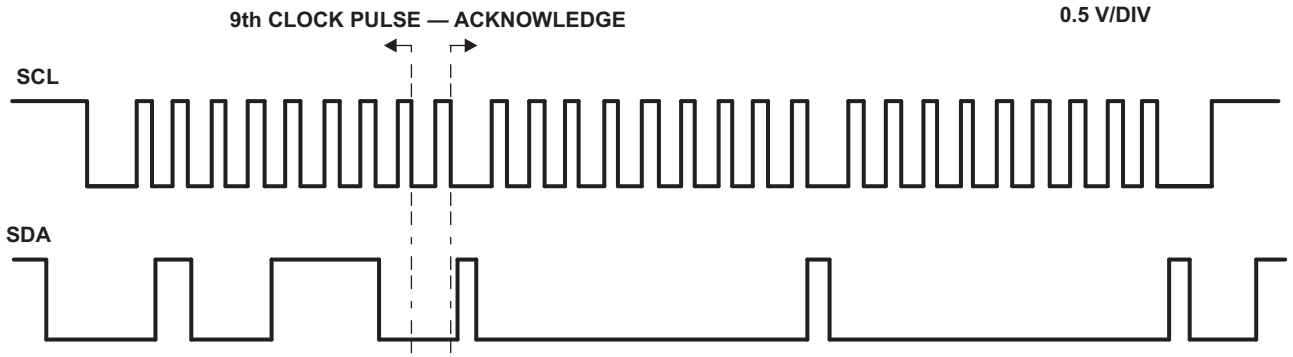


Figure 9. Bus A (0.9-V to 5.5-V Bus) Waveform

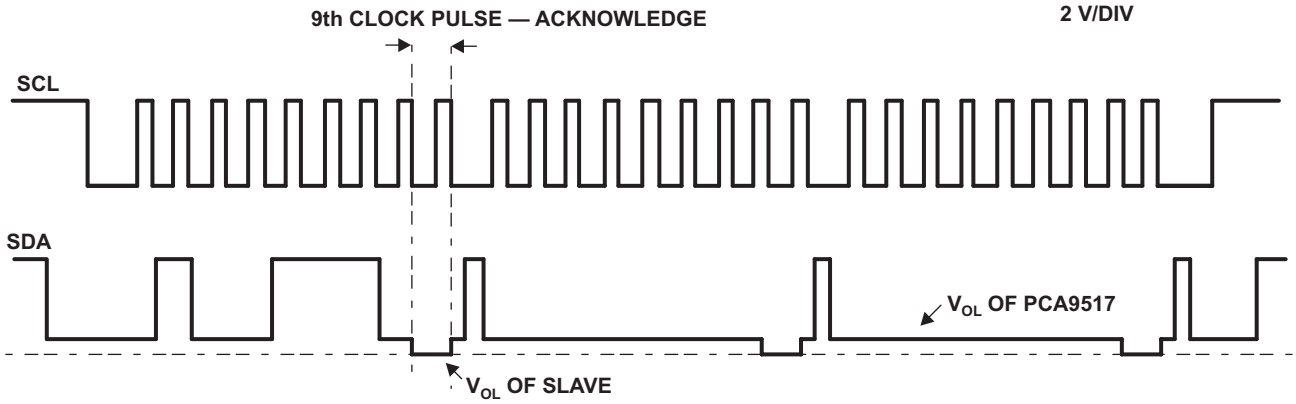


Figure 10. Bus B (2.7-V to 5.5-V Bus) Waveform

REVISION HISTORY

Changes from Revision B (May 2010) to Revision C	Page
• Deleted all references to arbitration and clock stretching support. This does not effect min/max specifications.	1

Changes from Revision C (February 2011) to Revision D	Page
• Updated the TOP-SIDE MARKING column of the ORDERING INFORMATION TABLE.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
HPA02225DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCA9517D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCA9517DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCA9517DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCA9517DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCA9517DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCA9517DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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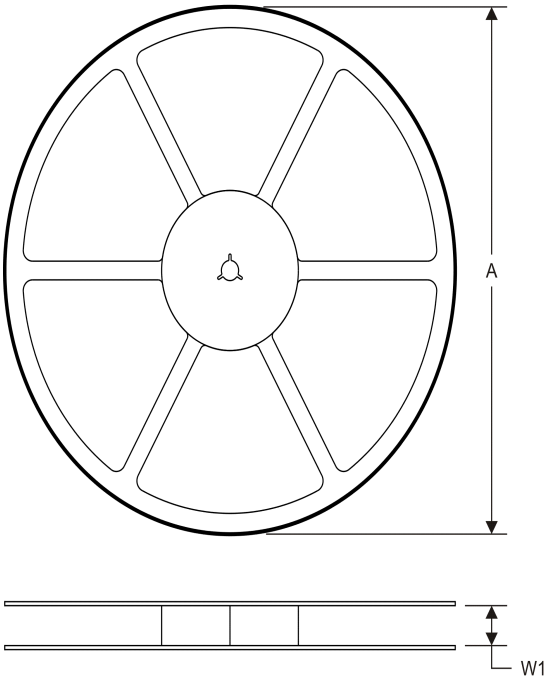
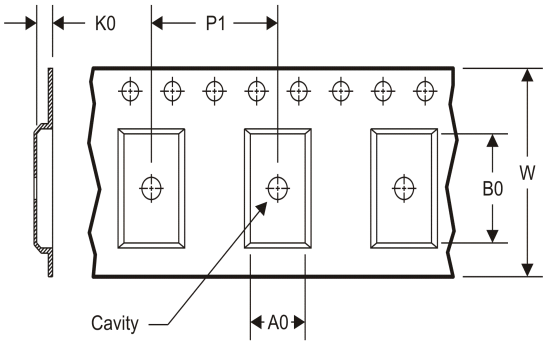
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



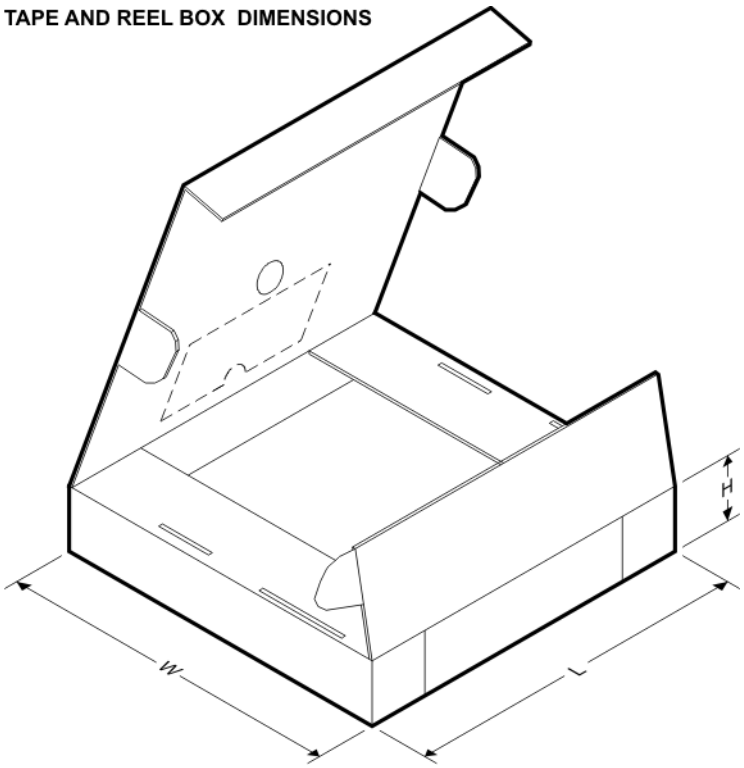
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9517DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PCA9517DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9517DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

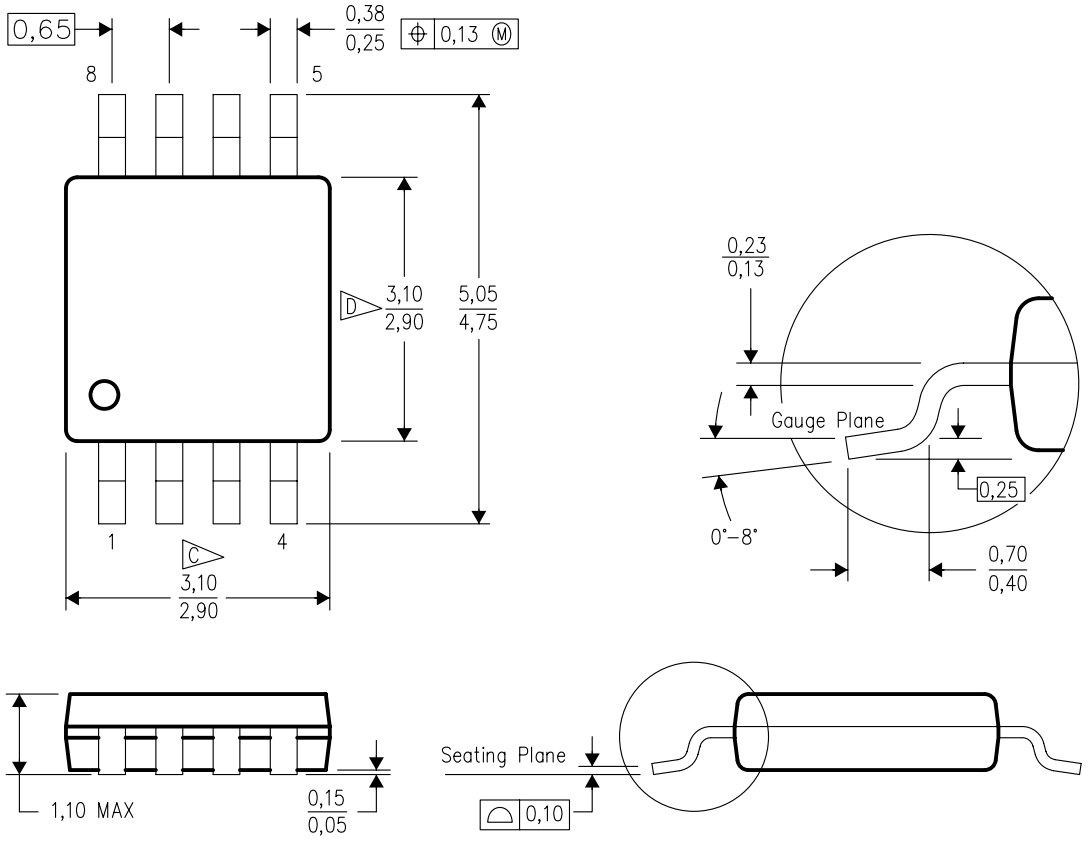
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9517DGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
PCA9517DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
PCA9517DR	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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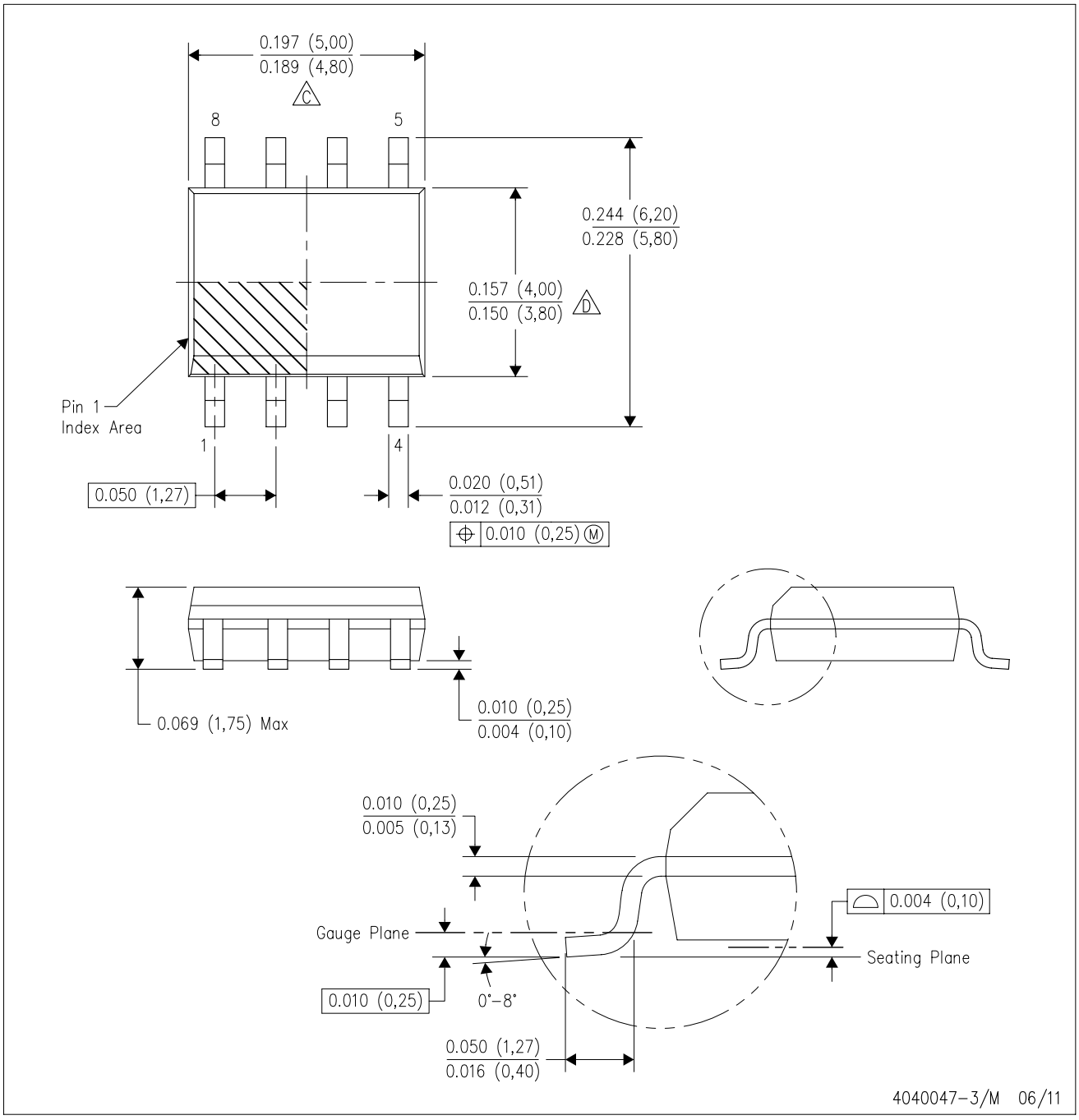
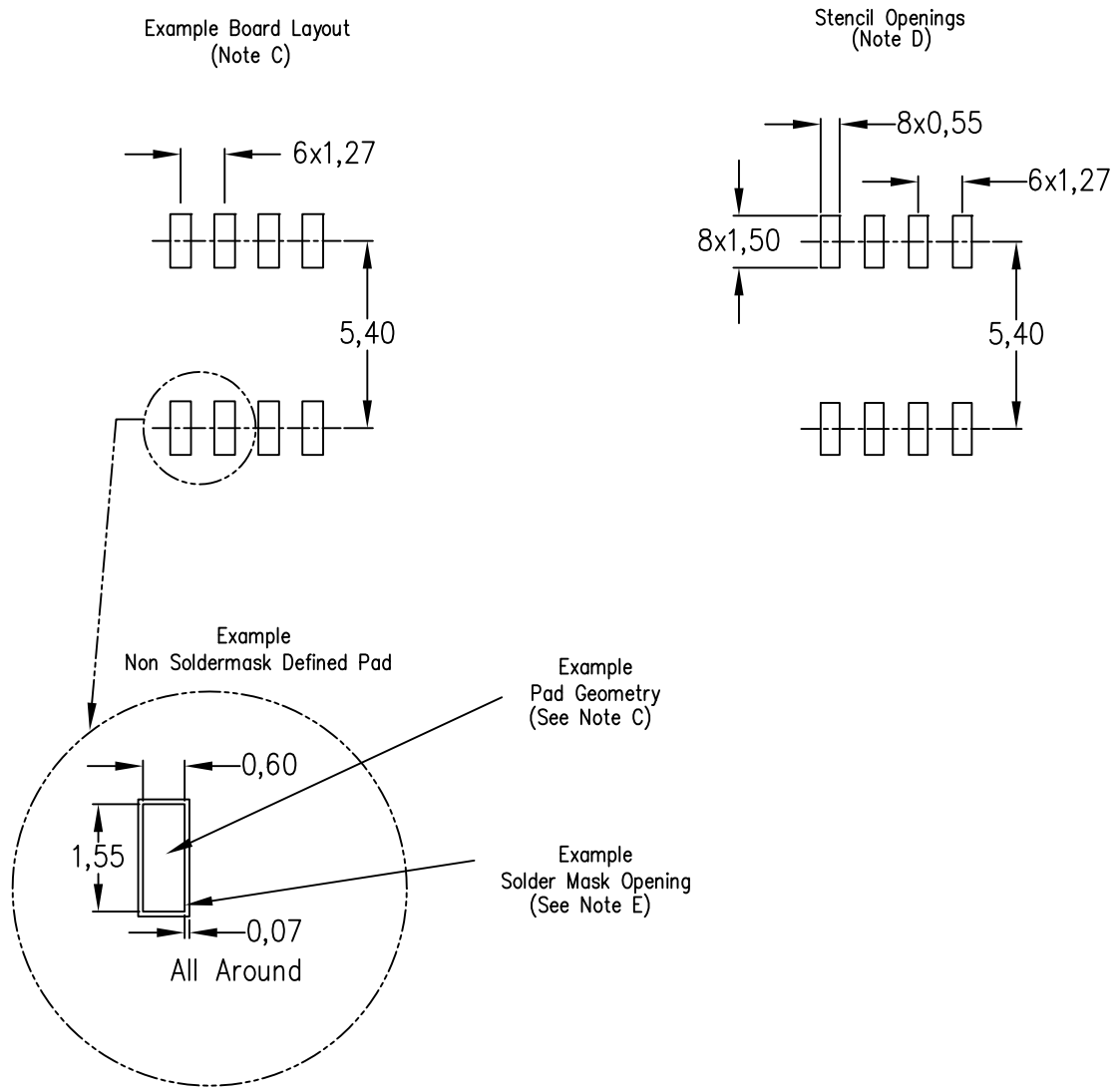
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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