

36V, Single-Supply, SOT553, General-Purpose OPERATIONAL AMPLIFIERS

Check for Samples: [OPA171](#), [OPA2171](#), [OPA4171](#)

FEATURES

- **Supply Range:** +2.7V to +36V, $\pm 1.35\text{V}$ to $\pm 18\text{V}$
- **Low Noise:** $14\text{nV}/\sqrt{\text{Hz}}$
- **Low Offset Drift:** $\pm 0.3\mu\text{V}/^\circ\text{C}$ (typ)
- **RFI Filtered Inputs**
- **Input Range Includes the Negative Supply**
- **Input Range Operates to Positive Supply**
- **Rail-to-Rail Output**
- **Gain Bandwidth:** 3MHz
- **Low Quiescent Current:** 475 μA per Amplifier
- **High Common-Mode Rejection:** 120dB (typ)
- **Low Input Bias Current:** 8pA
- **Industry-Standard Packages:**
 - 8-Pin SOIC
 - 8-Pin MSOP
 - 14-Pin TSSOP
- **microPackages:**
 - Single in SOT553
 - Dual in VSSOP-8

DESCRIPTION

The OPA171, OPA2171 and OPA4171 (OPAx171) are a family of 36V, single-supply, low-noise operational amplifiers with the ability to operate on supplies ranging from +2.7V ($\pm 1.35\text{V}$) to +36V ($\pm 18\text{V}$). These devices are available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps, which are specified at only one supply voltage, the OPAx171 family is specified from +2.7V to +36V. Input signals beyond the supply rails do not cause phase reversal. The OPAx171 family is stable with capacitive loads up to 300pF. The input can operate 100mV below the negative rail and within 2V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail.

The OPAx171 series of op amps are specified from -40°C to $+125^\circ\text{C}$.

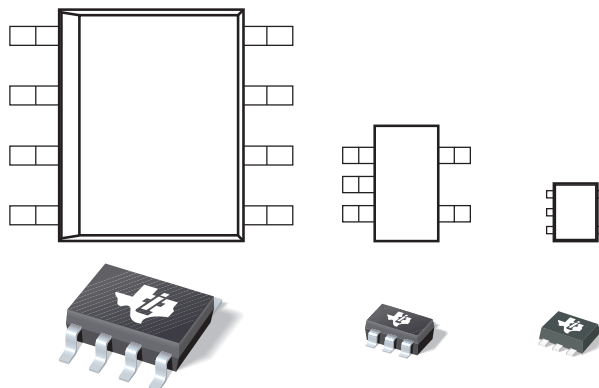
APPLICATIONS

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

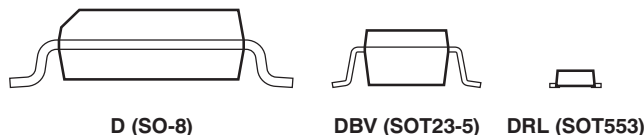
Product Family

DEVICE	PACKAGE
OPA171	SOT553, SOT23-5, SO-8
OPA2171 (dual)	VSSOP-8, SO-8, MSOP-8
OPA4171 (quad)	TSSOP-14, SO-14

Package Footprint Comparison (to Scale)



Package Height Comparison (to Scale)



Smallest Packaging for 36V Op Amps



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION ⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA171	SOT553	DRL	DAP	OPA171AIDRLT	Tape and Reel, 250
				OPA171AIDRLR	Tape and Reel, 4000
	SOT23-5	DBV	OSUI	OPA171AIDBVT	Tape and Reel, 250
				OPA171AIDBVR	Tape and Reel, 3000
	SO-8	D	O171A	OPA171AID	Rail, 75
				OPA171AIDR	Tape and Reel, 2500
OPA2171	MSOP-8	DGK	OPMI	OPA2171AIDGK	Rail, 80
				OPA2171AIDGKR	Tape and Reel, 2500
	VSSOP-8	DCU	OPOC	OPA2171AIDCUT	Tape and Reel, 250
				OPA2171AIDCUR	Tape and Reel, 3000
	SO-8	D	2171A	OPA2171AID	Rail, 75
				OPA2171AIDR	Tape and Reel, 2500
OPA4171	SO-14	D	OPA4171	OPA4171AID	Rail, 50
				OPA4171AIDR	Tape and Reel, 2500
	TSSOP-14	PW	OPA4171	OPA4171AIPW	Rail, 90
				OPA4171AIPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		OPAx171	UNIT
Supply voltage		±20	V
Signal input terminals	Voltage	(V ₋) – 0.5 to (V ₊) + 0.5	V
	Current	±10	mA
Output short circuit ⁽²⁾		Continuous	
Operating temperature		–55 to +150	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
ESD ratings:	Human body model (HBM)	4	kV
	Charged device model (CDM)	750	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $V_S = +2.7\text{V}$ to $+36\text{V}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA171, OPA2171, OPA4171			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input offset voltage	V_{OS}		0.25	± 1.8	mV
Over temperature			0.3	± 2	mV
Drift	dV_{OS}/dT		0.3	± 2	$\mu V/^{\circ}C$
vs power supply	PSRR	$V_S = +4V$ to $+36V$	1	± 3	$\mu V/V$
Channel separation, dc	dc		5		$\mu V/V$
INPUT BIAS CURRENT					
Input bias current	I_B		± 8	± 15	pA
Over temperature				± 3.5	nA
Input offset current	I_{OS}		± 4		pA
Over temperature				± 3.5	nA
NOISE					
Input voltage noise		$f = 0.1\text{Hz}$ to 10Hz	3		μV_{PP}
Input voltage noise density	e_n	$f = 100\text{Hz}$	25		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$	14		$\text{nV}/\sqrt{\text{Hz}}$
INPUT VOLTAGE					
Common-mode voltage range ⁽¹⁾	V_{CM}		$(V-) - 0.1V$	$(V+) - 2V$	V
Common-mode rejection ratio	CMRR	$V_S = \pm 2V, (V-) - 0.1V < V_{CM} < (V+) - 2V$	90	104	dB
		$V_S = \pm 18V, (V-) - 0.1V < V_{CM} < (V+) - 2V$	104	120	dB
INPUT IMPEDANCE					
Differential			$100 \parallel 3$		$\text{M}\Omega \parallel \text{pF}$
Common-mode			$6 \parallel 3$		$10^{12}\Omega \parallel \text{pF}$
OPEN-LOOP GAIN					
Open-loop voltage gain	A_{OL}	$V_S = +4V$ to $+36V, (V-) + 0.35V < V_O < (V+) - 0.35V$	110	130	dB
FREQUENCY RESPONSE					
Gain bandwidth product	GBP		3.0		MHz
Slew rate	SR	$G = +1$	1.5		V/ μs
Settling time	t_S	To 0.1%, $V_S = \pm 18V, G = +1, 10V$ step	6		μs
		To 0.01% (12 bit), $V_S = \pm 18V, G = +1, 10V$ step	10		μs
Overload recovery time		$V_{IN} \times \text{Gain} > V_S$	2		μs
Total harmonic distortion + noise	THD+N	$G = +1, f = 1\text{kHz}, V_O = 3V_{RMS}$	0.0002		%
OUTPUT					
Voltage output swing from rail	V_O	$V_S = 5V, R_L = 10\text{k}\Omega$	30		mV
Over temperature		$R_L = 10\text{k}\Omega, A_{OL} \geq 110\text{dB}$	$(V-) + 0.35$	$(V+) - 0.35$	V
Short-circuit current	I_{SC}		+25/-35		mA
Capacitive load drive	C_{LOAD}		See Typical Characteristics		pF
Open-loop output resistance	R_O	$f = 1\text{MHz}, I_O = 0A$	150		Ω
POWER SUPPLY					
Specified voltage range	V_S		+2.7	+36	V
Quiescent current per amplifier	I_Q	$I_O = 0A$	475	595	μA
Over temperature		$I_O = 0A$		650	μA
TEMPERATURE					
Specified range			-40	+125	$^{\circ}C$
Operating range			-55	+150	$^{\circ}C$

(1) The input range can be extended beyond $(V+) - 2\text{V}$ up to $V+$. See the [Typical Characteristics](#) and [Application Information](#) sections for additional information.

THERMAL INFORMATION: OPA171

THERMAL METRIC ⁽¹⁾		OPA171			UNITS
		D (SO)	DBV (SOT23)	DRL (SOT553)	
		8 PINS	5 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	97.9	133.9	0.1	
θ_{JB}	Junction-to-board thermal resistance	87.7	83.6	42.4	
Ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	0.5	
Ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	42.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

THERMAL INFORMATION: OPA2171

THERMAL METRIC ⁽¹⁾		OPA2171			UNITS
		D (SO)	DCU (VSSOP)	DGK (MSOP)	
		8 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	134.3	175.2	195.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	72.1	74.9	59.4	
θ_{JB}	Junction-to-board thermal resistance	60.6	22.2	115.1	
Ψ_{JT}	Junction-to-top characterization parameter	18.2	1.6	4.7	
Ψ_{JB}	Junction-to-board characterization parameter	53.8	22.8	114.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

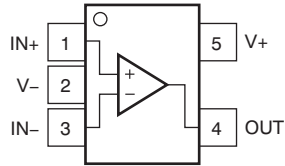
THERMAL INFORMATION: OPA4171

THERMAL METRIC ⁽¹⁾		OPA4171		UNITS
		D (SO)	PW (TSSOP)	
		14 PINS	14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	51.8	24.4	
θ_{JB}	Junction-to-board thermal resistance	49.4	59.3	
Ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	
Ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	

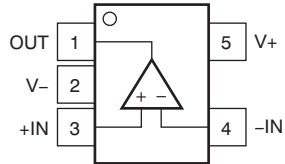
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PIN CONFIGURATIONS

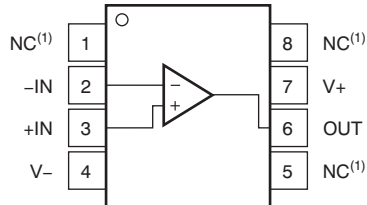
**DRL PACKAGE: OPA171
SOT-553
(TOP VIEW)**



**DBV PACKAGE: OPA171
SOT23-5
(TOP VIEW)**

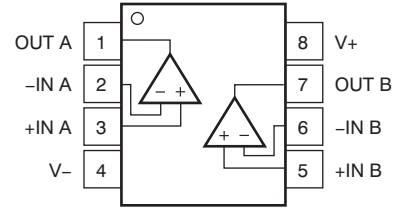


**D PACKAGE: OPA171
SO-8
(TOP VIEW)**

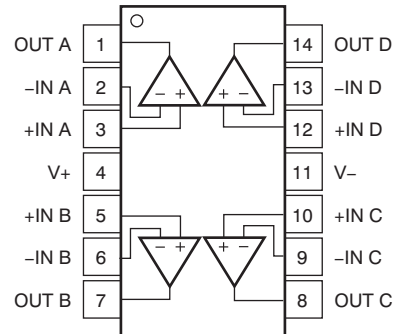


(1) No internal connection.

**D, DCU, AND DGK PACKAGES: OPA2171
SO-8, VSSOP-8, AND MSOP-8
(TOP VIEW)**



**D AND PW PACKAGES: OPA4171
SO-14 AND TSSOP-14
(TOP VIEW)**



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B and I_{OS} vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 10
CMRR vs Temperature	Figure 11
PSRR vs Temperature	Figure 12
0.1Hz to 10Hz Noise	Figure 13
Input Voltage Noise Spectral Density vs Frequency	Figure 14
THD+N Ratio vs Frequency	Figure 15
THD+N vs Output Amplitude	Figure 16
Quiescent Current vs Temperature	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Open-Loop Gain and Phase vs Frequency	Figure 19
Closed-Loop Gain vs Frequency	Figure 20
Open-Loop Gain vs Temperature	Figure 21
Open-Loop Output Impedance vs Frequency	Figure 22
Small-Signal Overshoot vs Capacitive Load (100mV Output Step)	Figure 23, Figure 24
No Phase Reversal	Figure 25
Positive Overload Recovery	Figure 26
Negative Overload Recovery	Figure 27
Small-Signal Step Response (100mV)	Figure 28, Figure 29
Large-Signal Step Response	Figure 30, Figure 31
Large-Signal Settling Time (10V Positive Step)	Figure 32
Large-Signal Settling Time (10V Negative Step)	Figure 33
Short-Circuit Current vs Temperature	Figure 34
Maximum Output Voltage vs Frequency	Figure 35
Channel Separation vs Frequency	Figure 36

TYPICAL CHARACTERISTICS

$V_S = \pm 18V$, $V_{CM} = V_S/2$, $R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

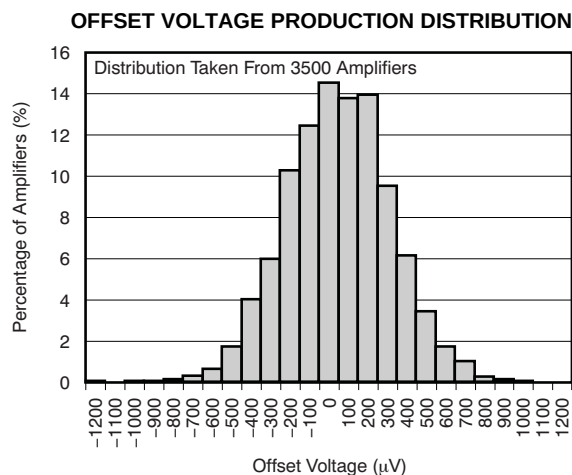


Figure 1.

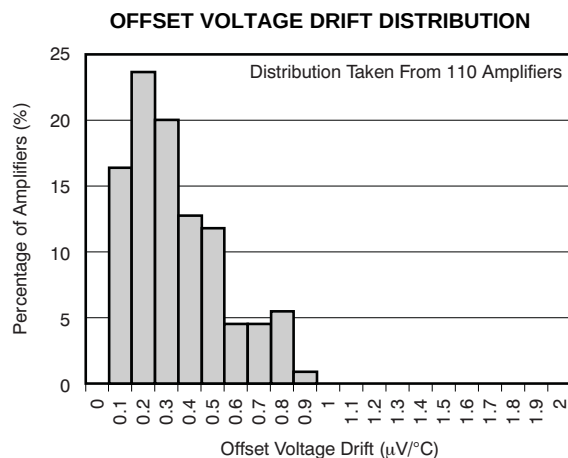


Figure 2.

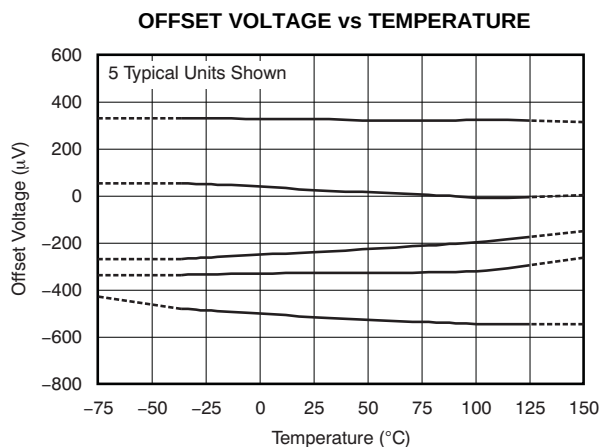


Figure 3.

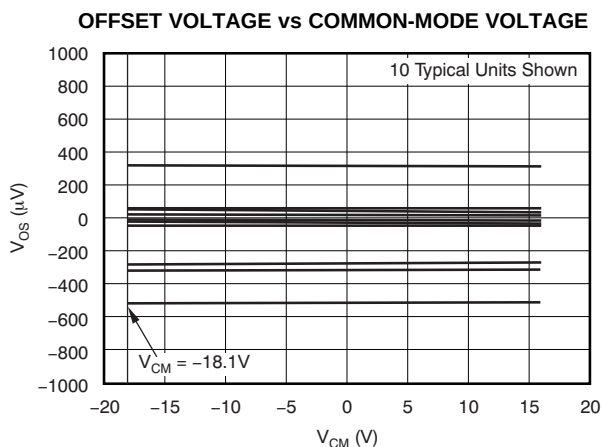


Figure 4.

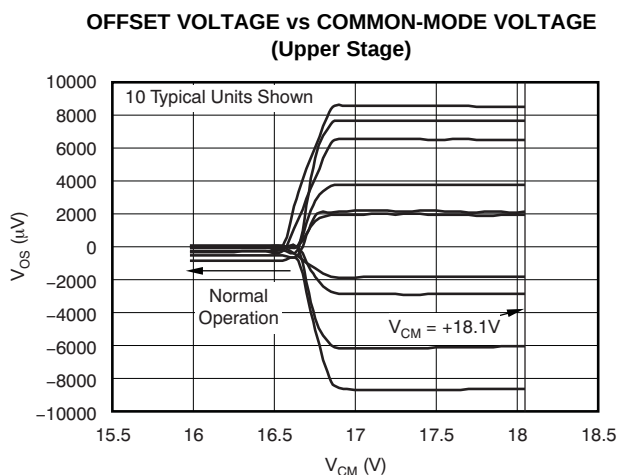


Figure 5.

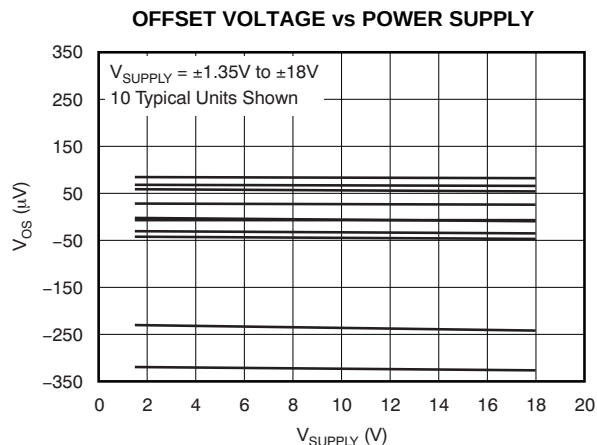


Figure 6.

TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 18V$, $V_{CM} = V_S/2$, $R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

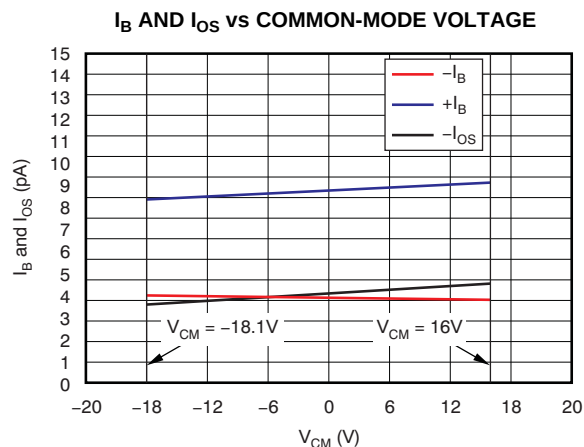


Figure 7.

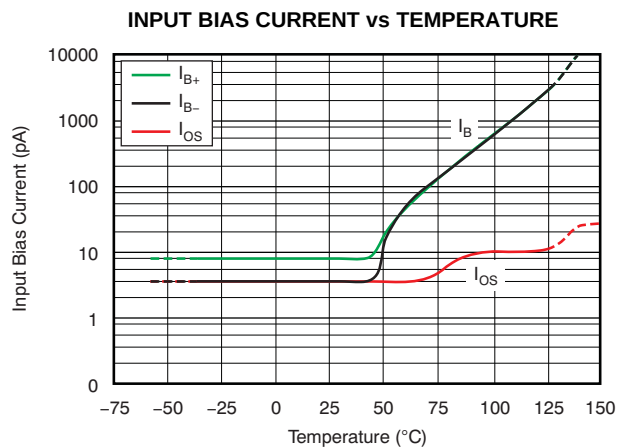


Figure 8.

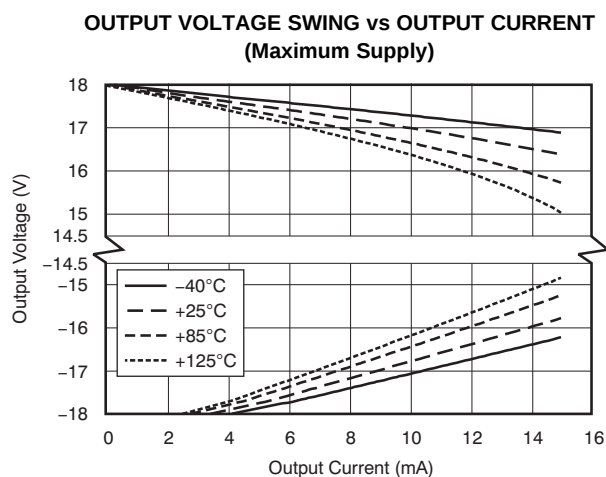


Figure 9.

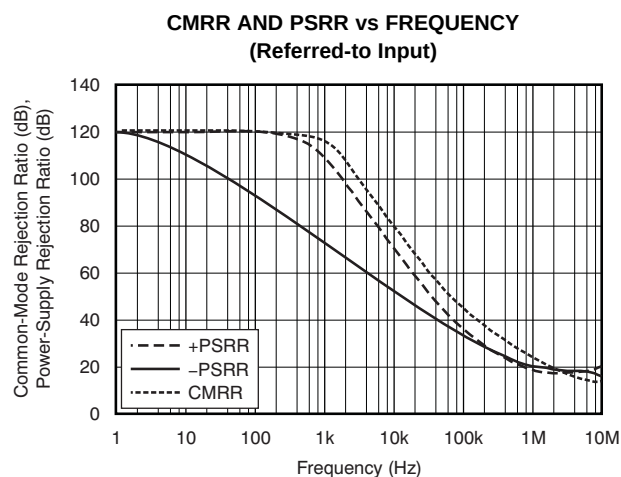


Figure 10.

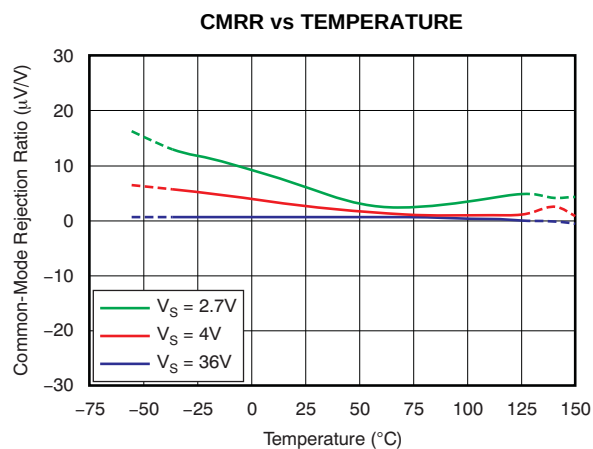


Figure 11.

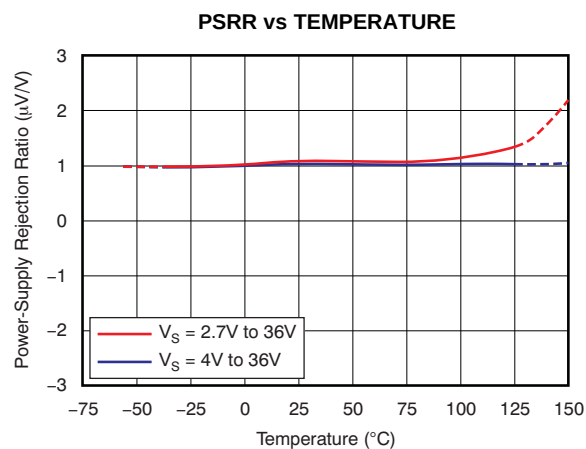


Figure 12.

TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 18V$, $V_{CM} = V_S/2$, $R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

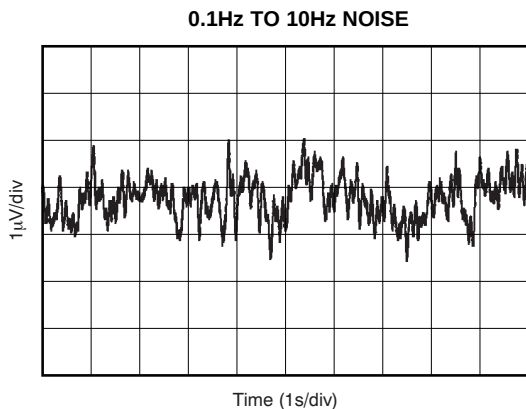


Figure 13.

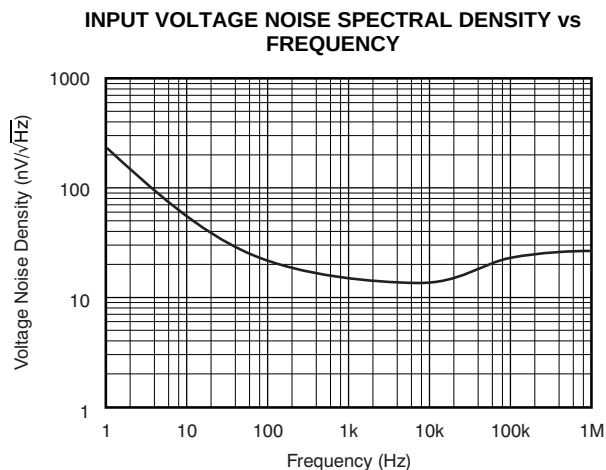


Figure 14.

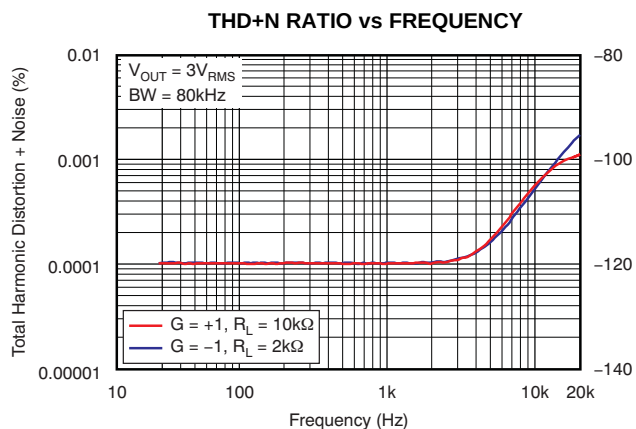


Figure 15.

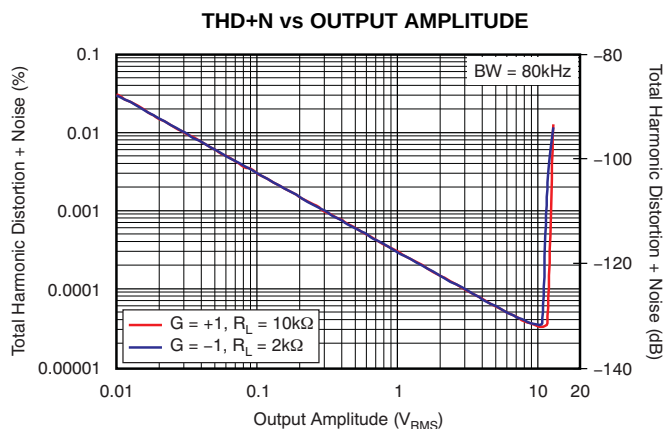


Figure 16.

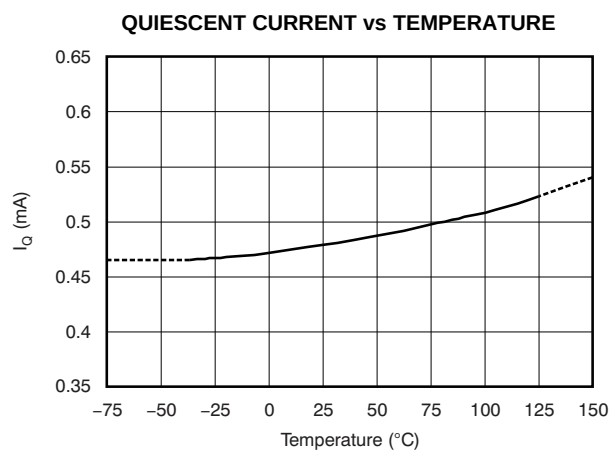


Figure 17.

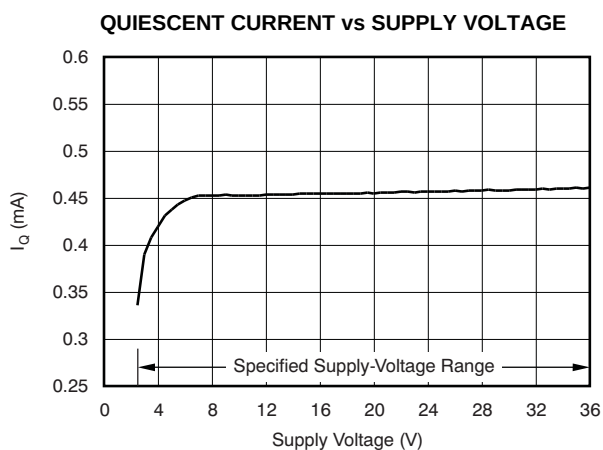


Figure 18.

TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 18V$, $V_{CM} = V_S/2$, $R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

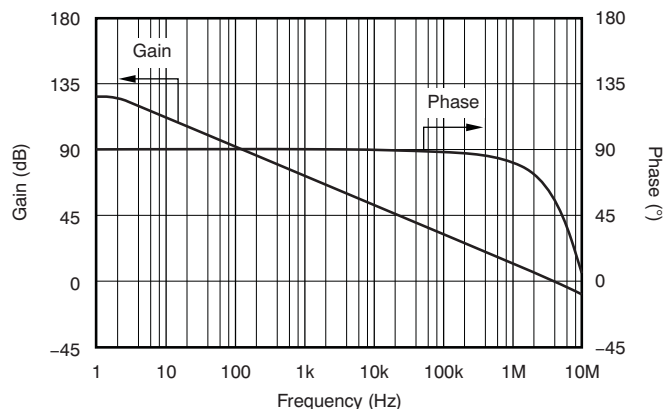


Figure 19.

CLOSED-LOOP GAIN vs FREQUENCY

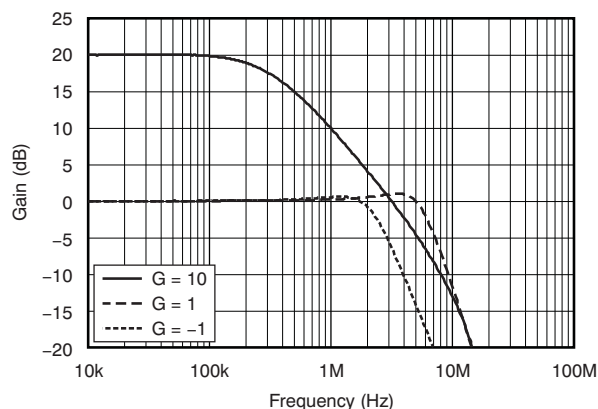


Figure 20.

OPEN-LOOP GAIN vs TEMPERATURE

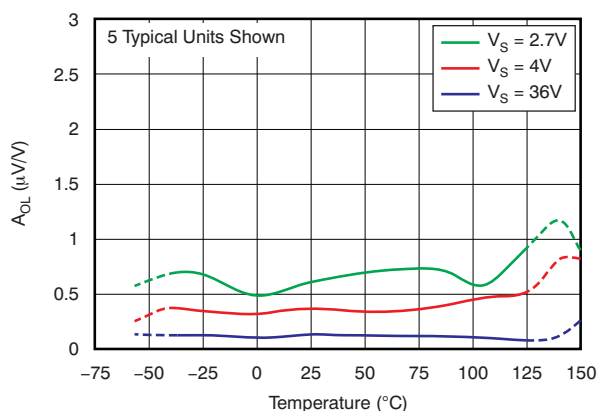


Figure 21.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

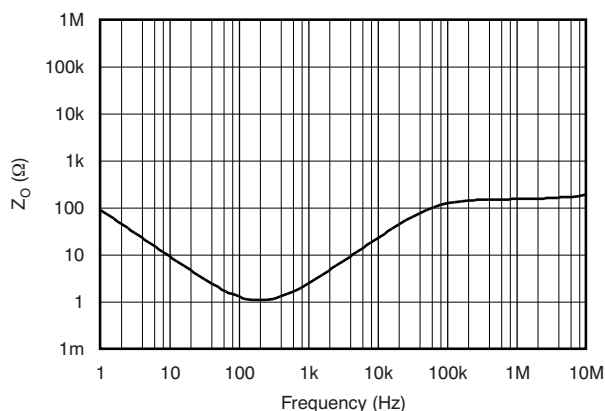


Figure 22.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD
(100mV Output Step)

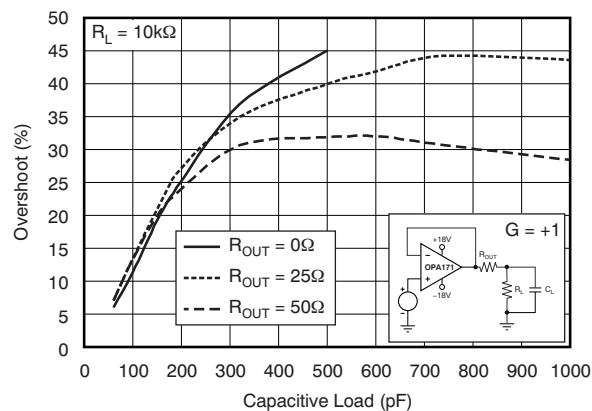


Figure 23.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD
(100mV Output Step)

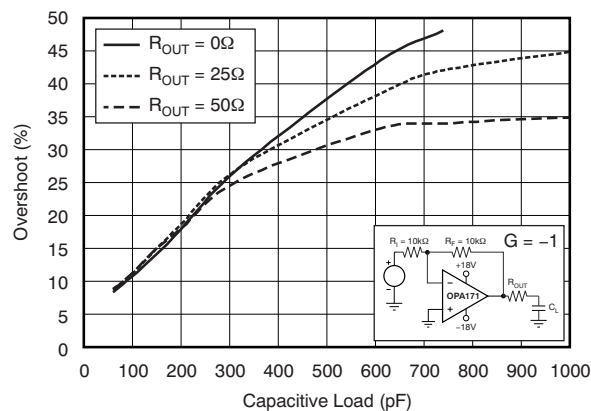
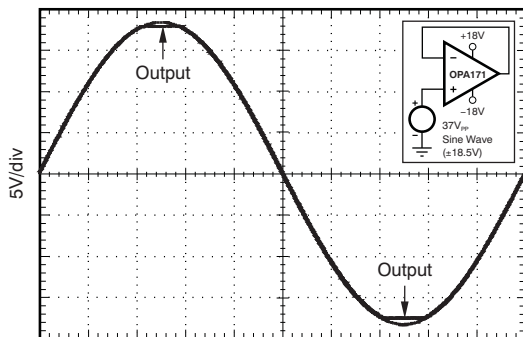


Figure 24.

TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 18V$, $V_{CM} = V_S/2$, $R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

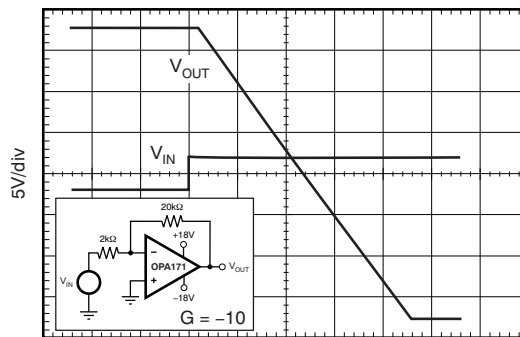
NO PHASE REVERSAL



Time (100 μ s/div)

Figure 25.

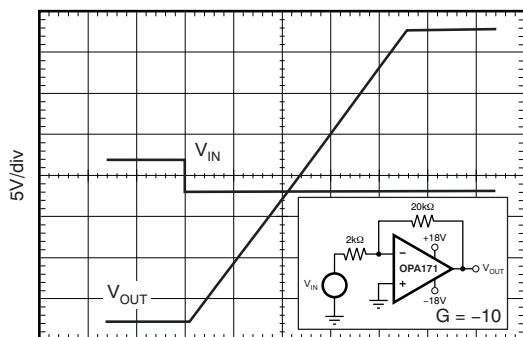
POSITIVE OVERLOAD RECOVERY



Time (5 μ s/div)

Figure 26.

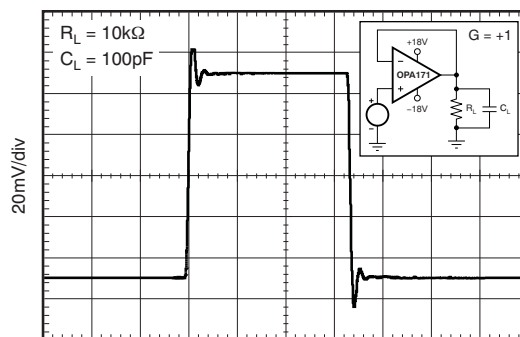
NEGATIVE OVERLOAD RECOVERY



Time (5 μ s/div)

Figure 27.

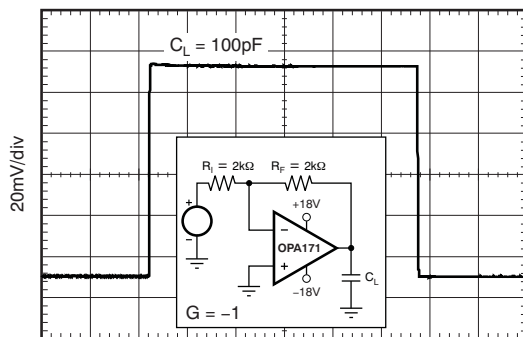
**SMALL-SIGNAL STEP RESPONSE
(100mV)**



Time (1 μ s/div)

Figure 28.

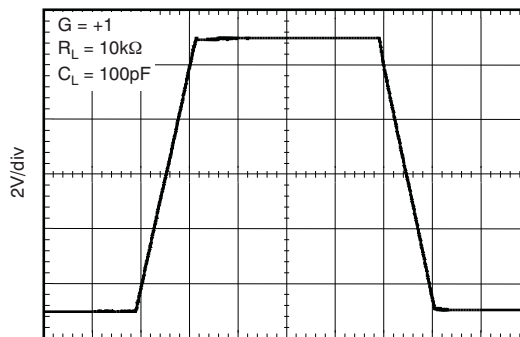
**SMALL-SIGNAL STEP RESPONSE
(100mV)**



Time (20 μ s/div)

Figure 29.

LARGE-SIGNAL STEP RESPONSE



Time (5 μ s/div)

Figure 30.

TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 18V$, $V_{CM} = V_S/2$, $R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

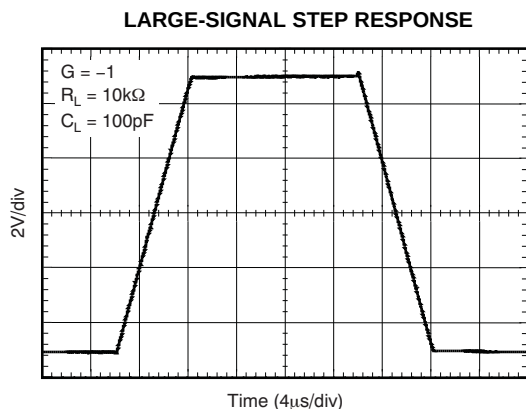


Figure 31.

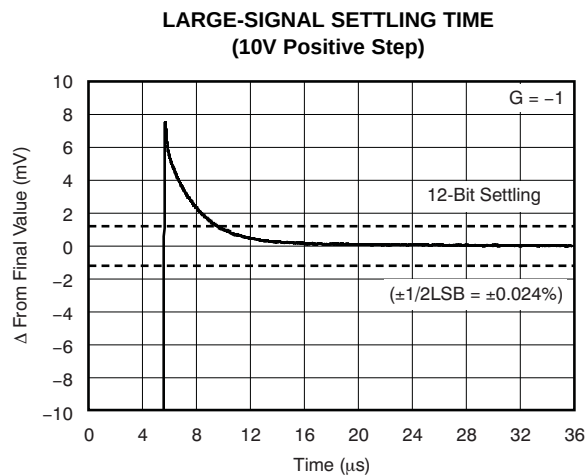


Figure 32.

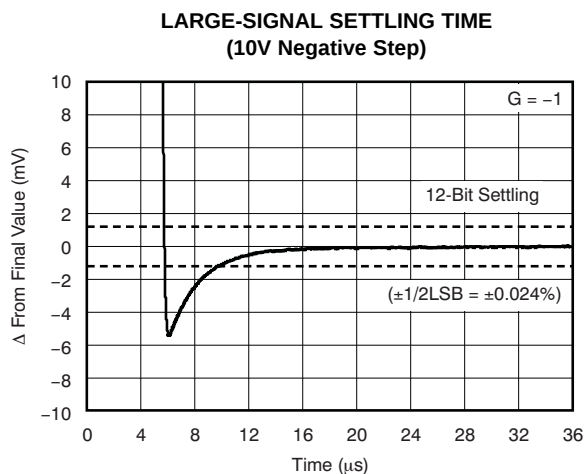


Figure 33.

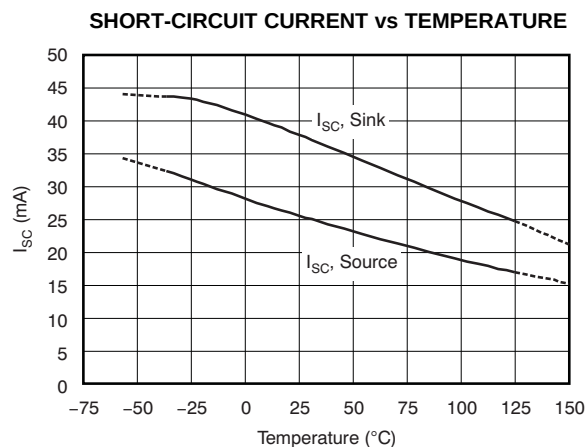


Figure 34.

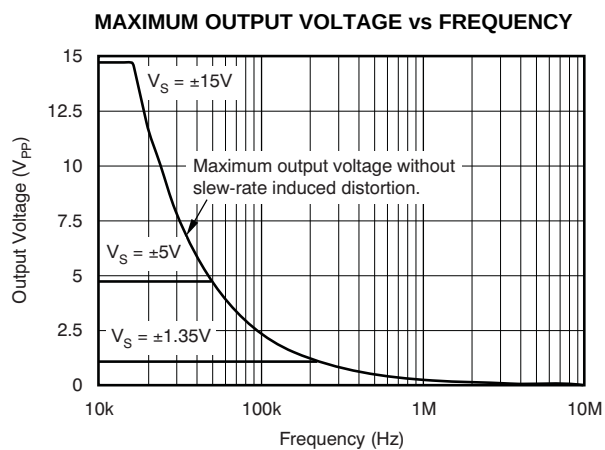


Figure 35.

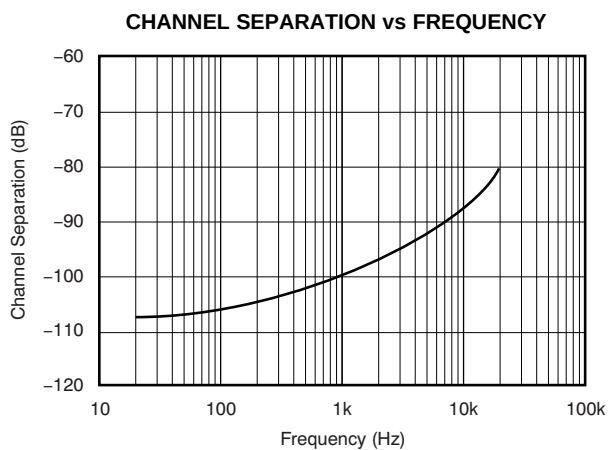


Figure 36.

APPLICATION INFORMATION

The OPAx171 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only $2\mu\text{V}/^\circ\text{C}$ provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL} . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, $0.1\mu\text{F}$ capacitors are adequate.

OPERATING CHARACTERISTICS

The OPAx171 family of amplifiers is specified for operation from 2.7V to 36V ($\pm 1.35\text{V}$ to $\pm 18\text{V}$). Many of the specifications apply from -40°C to $+125^\circ\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Low-loss, $0.1\mu\text{F}$ bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable to single-supply applications.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPAx171 series extends 100mV below the negative rail and within 2V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail. The typical performance in this range is summarized in [Table 2](#).

PHASE-REVERSAL PROTECTION

The OPAx171 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in [Figure 37](#).

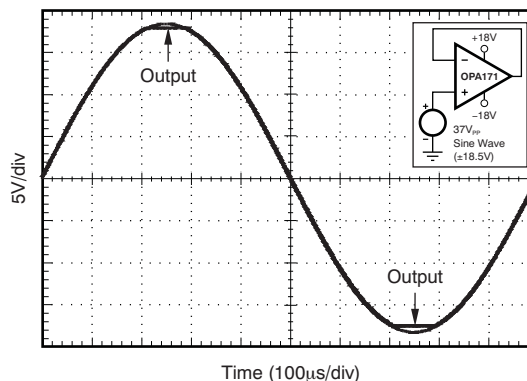


Figure 37. No Phase Reversal

Table 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
vs Temperature		12		$\mu\text{V}/^\circ\text{C}$
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/ μs
Noise at $f = 1\text{kHz}$		30		$\text{nV}/\sqrt{\text{Hz}}$

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx171 have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50Ω) in series with the output. Figure 38 and Figure 39 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT} . Also, refer to [Applications Bulletin AB-028 \(SBOA015\)](#), available for download from the TI website for details of analysis techniques and application circuits.

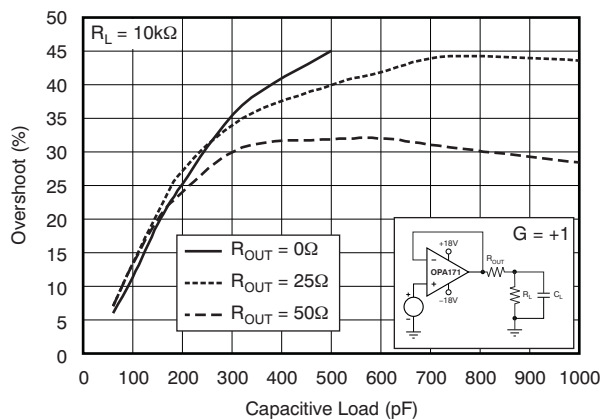


Figure 38. Small-Signal Overshoot versus Capacitive Load (100mV Output Step)

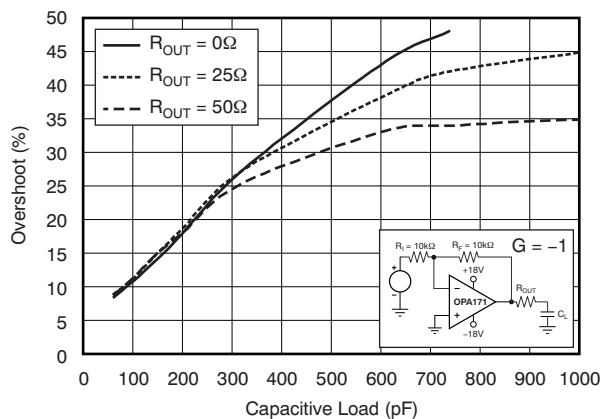


Figure 39. Small-Signal Overshoot versus Capacitive Load (100mV Output Step)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins

or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the [Absolute Maximum Ratings](#). Figure 40 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

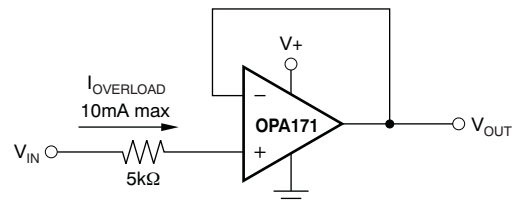


Figure 40. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2010) to Revision C	Page
• Added MSOP-8 package to device graphic	1
• Added MSOP-8 package to Features bullets	1
• Added MSOP-8 package to Product Family table	1
• Added MSOP-8 package to Package/Ordering Information table	2
• Deleted "A" suffix from OPA4171 package markings in Package/Ordering Information table.	2
• Added new row for Voltage Output Swing from Rail parameter to <i>Output</i> subsection of Electrical Characteristics	3
• Changed Voltage Output Swing from Rail parameter to over temperature in <i>Output</i> subsection of Electrical Characteristics	3
• Updated format of thermal information tables	4
• Added MSOP-8 package to OPA2171 Thermal Information table	4
• Updated pinout configurations for OPA2171 and OPA4171	5
• Changed Figure 9	8
Changes from Revision A (November, 2010) to Revision B	Page
• Changed input offset voltage specification	3
• Changed input offset voltage, over temperature specification	3
• Changed quiescent current per amplifier, over temperature specification	3

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
OPA171AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA171AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA171AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA171AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA171AIDRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA171AIDRLT	ACTIVE	SOT	DRL	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA2171AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2171AIDCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA2171AIDCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA2171AIDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2171AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2171AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4171AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
OPA4171AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
OPA4171AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4171AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

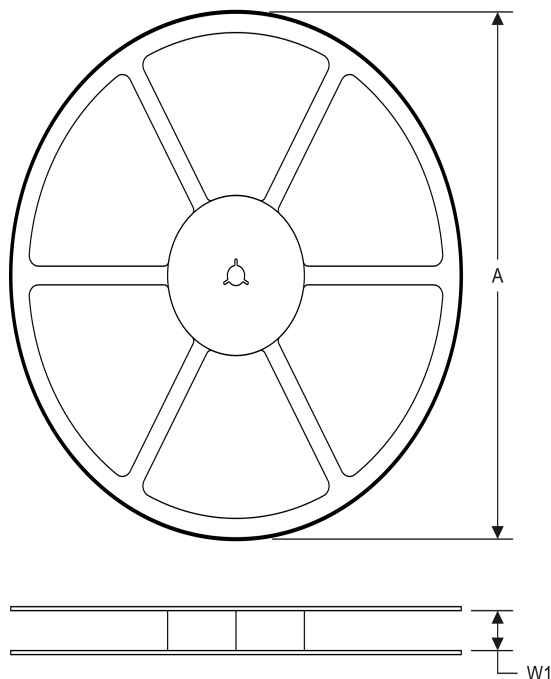
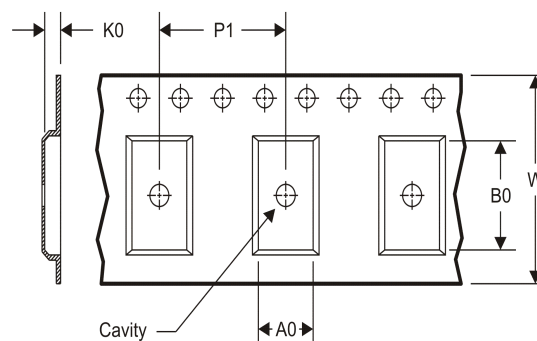
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA171 :

- Automotive: [OPA171-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA171AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA171AIDRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA171AIDRLT	SOT	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA2171AIDCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDCUT	US8	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4171AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4171AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

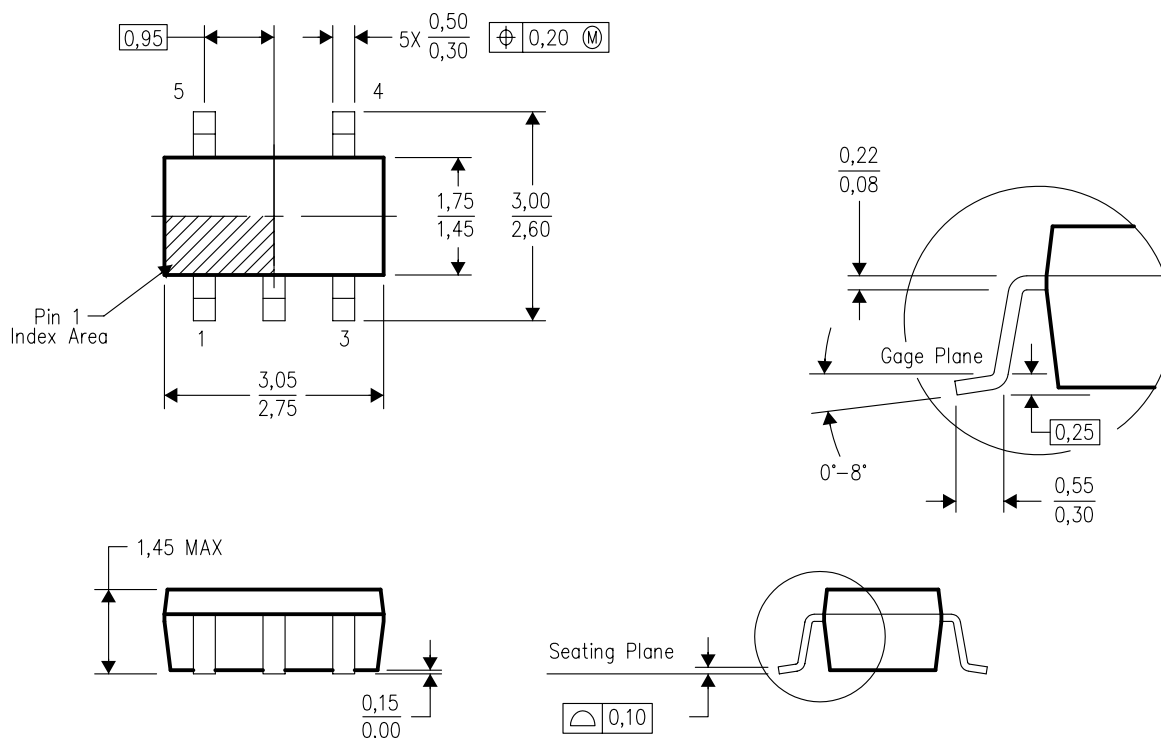


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA171AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA171AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA171AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA171AIDRLR	SOT	DRL	5	4000	202.0	201.0	28.0
OPA171AIDRLT	SOT	DRL	5	250	202.0	201.0	28.0
OPA2171AIDCUR	US8	DCU	8	3000	202.0	201.0	28.0
OPA2171AIDCUT	US8	DCU	8	250	202.0	201.0	28.0
OPA2171AIDGKR	MSOP	DGK	8	2500	366.0	364.0	50.0
OPA2171AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA4171AIDR	SOIC	D	14	2500	346.0	346.0	33.0
OPA4171AIPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

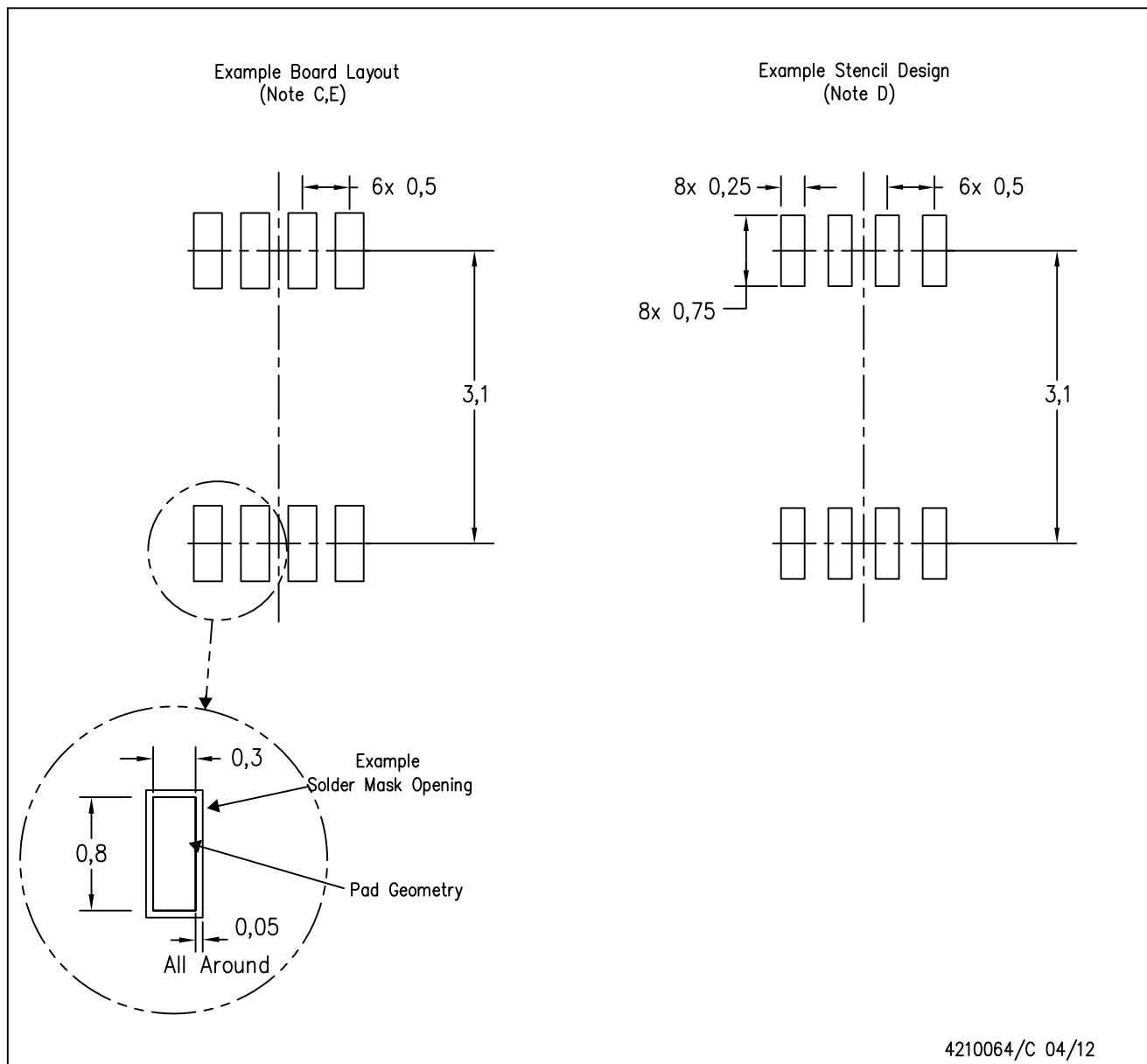


NOTES:

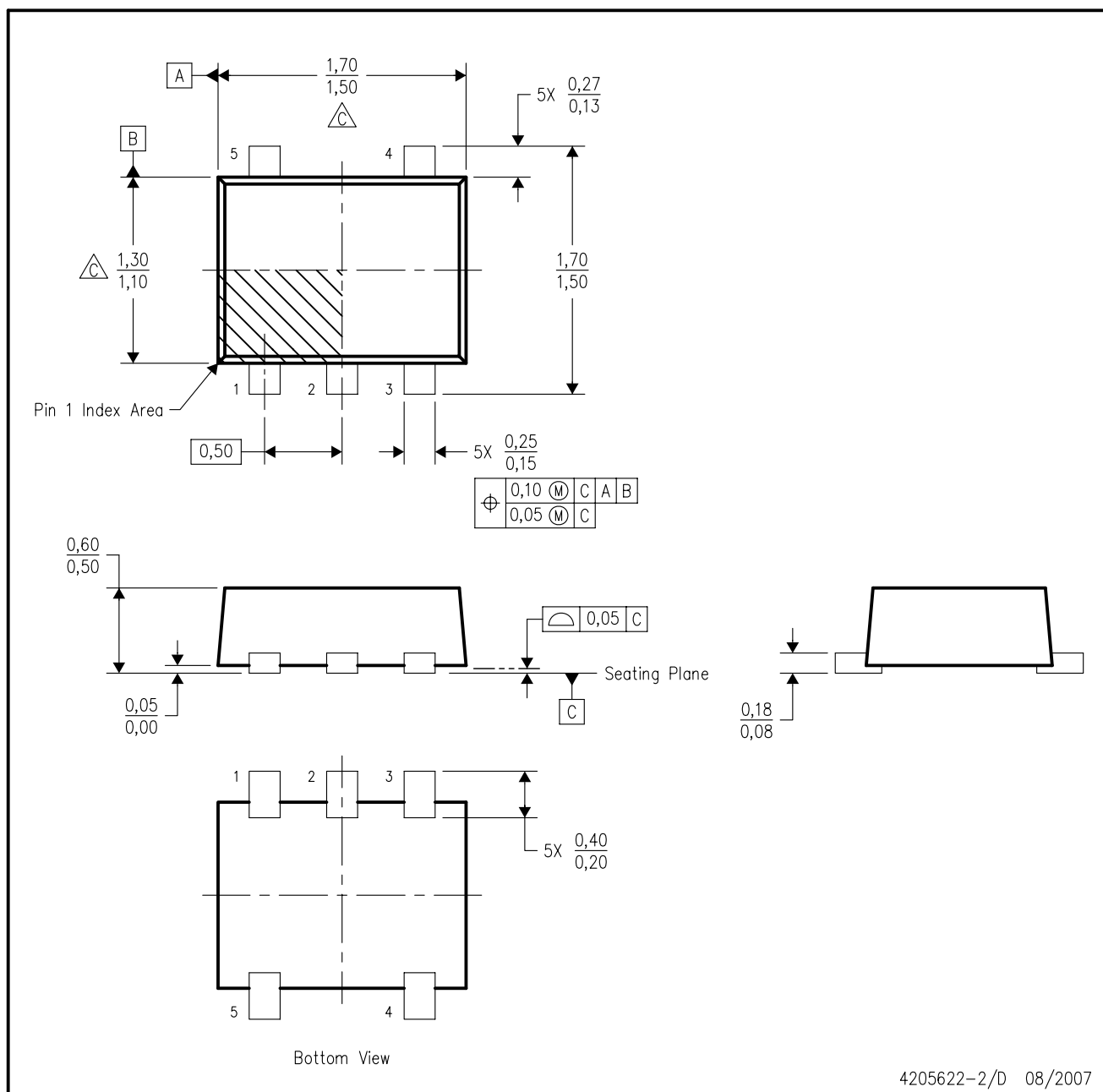
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

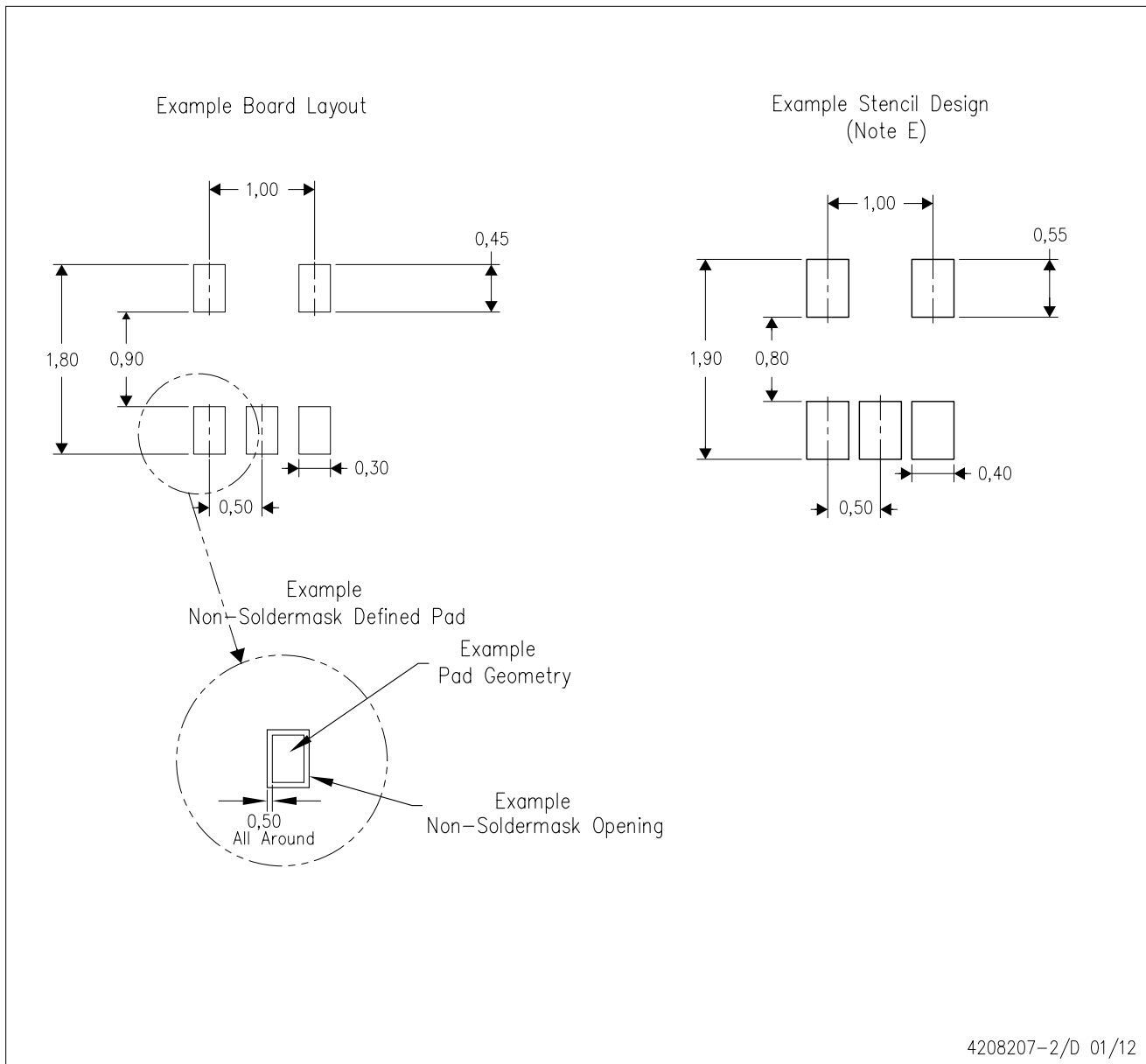


4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



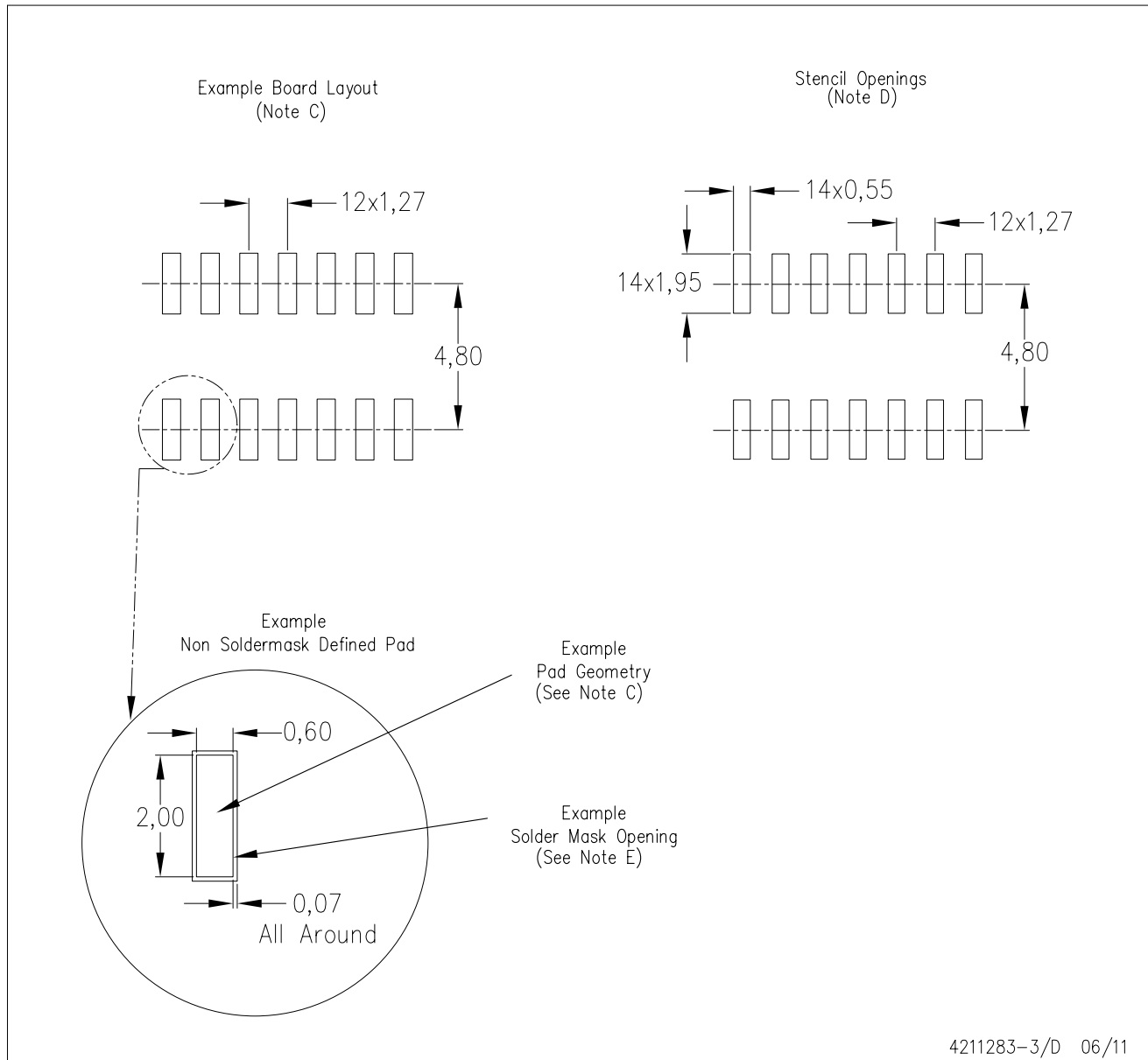
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

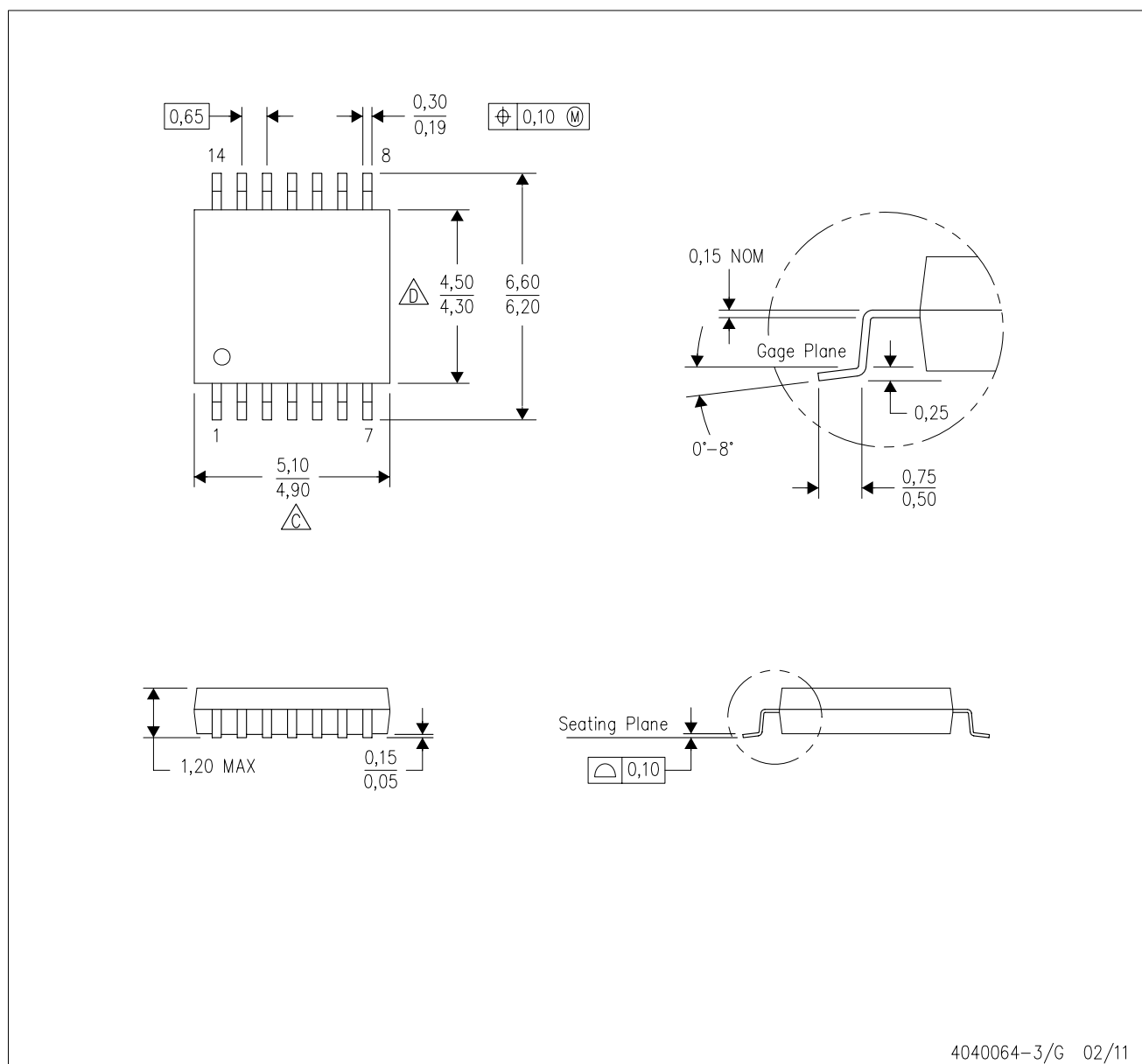


4211283-3/D 06/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

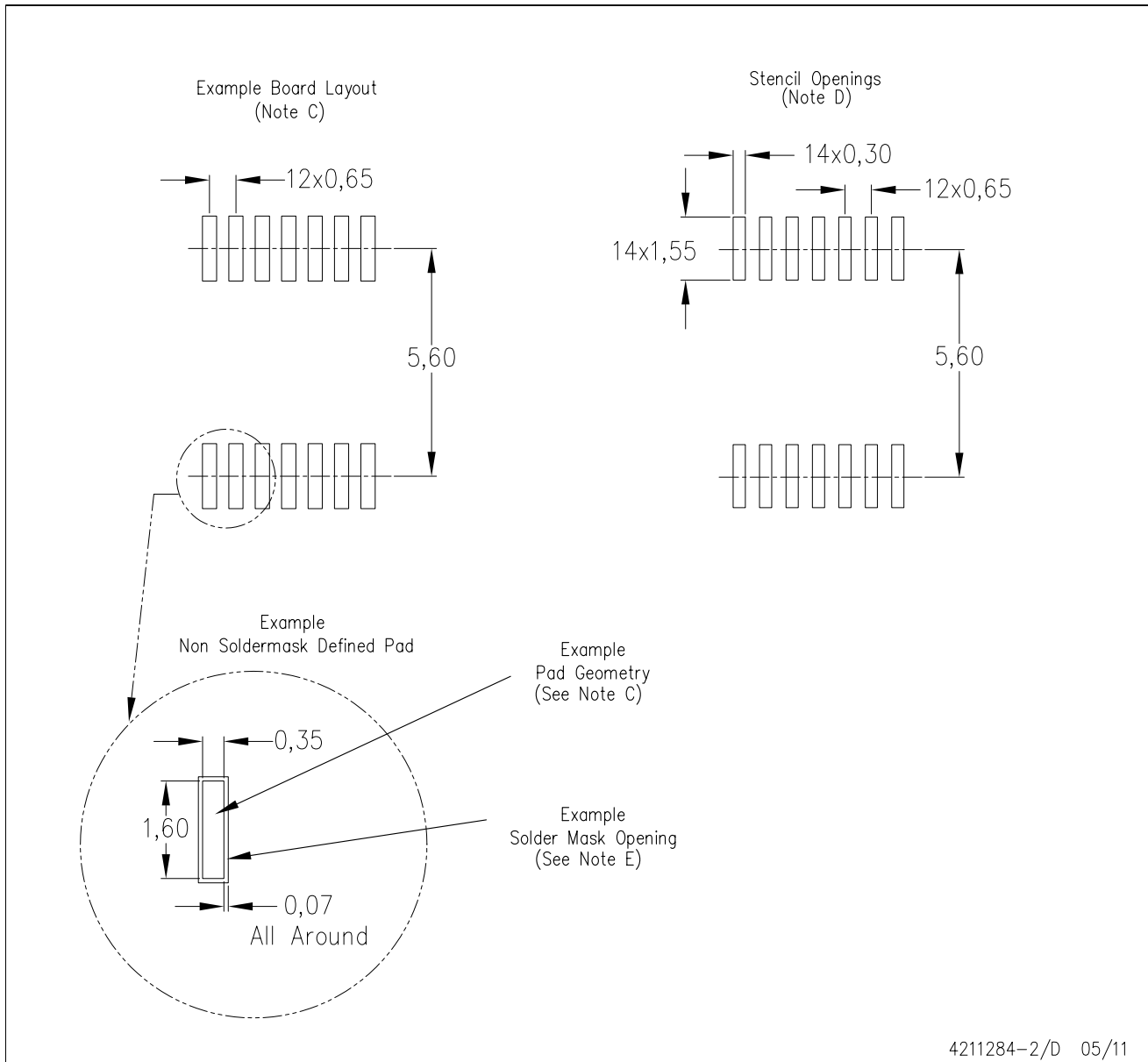
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

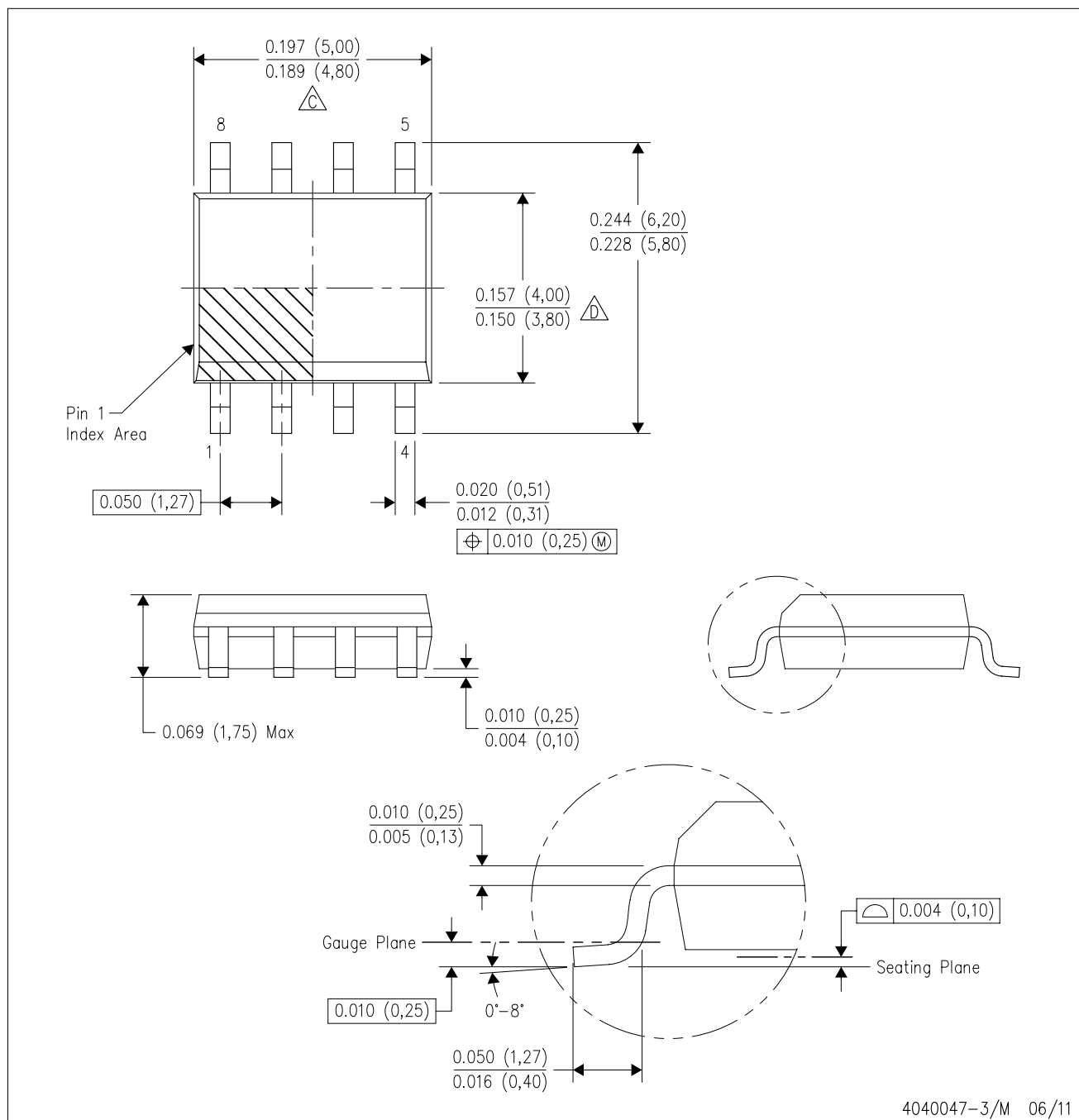
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

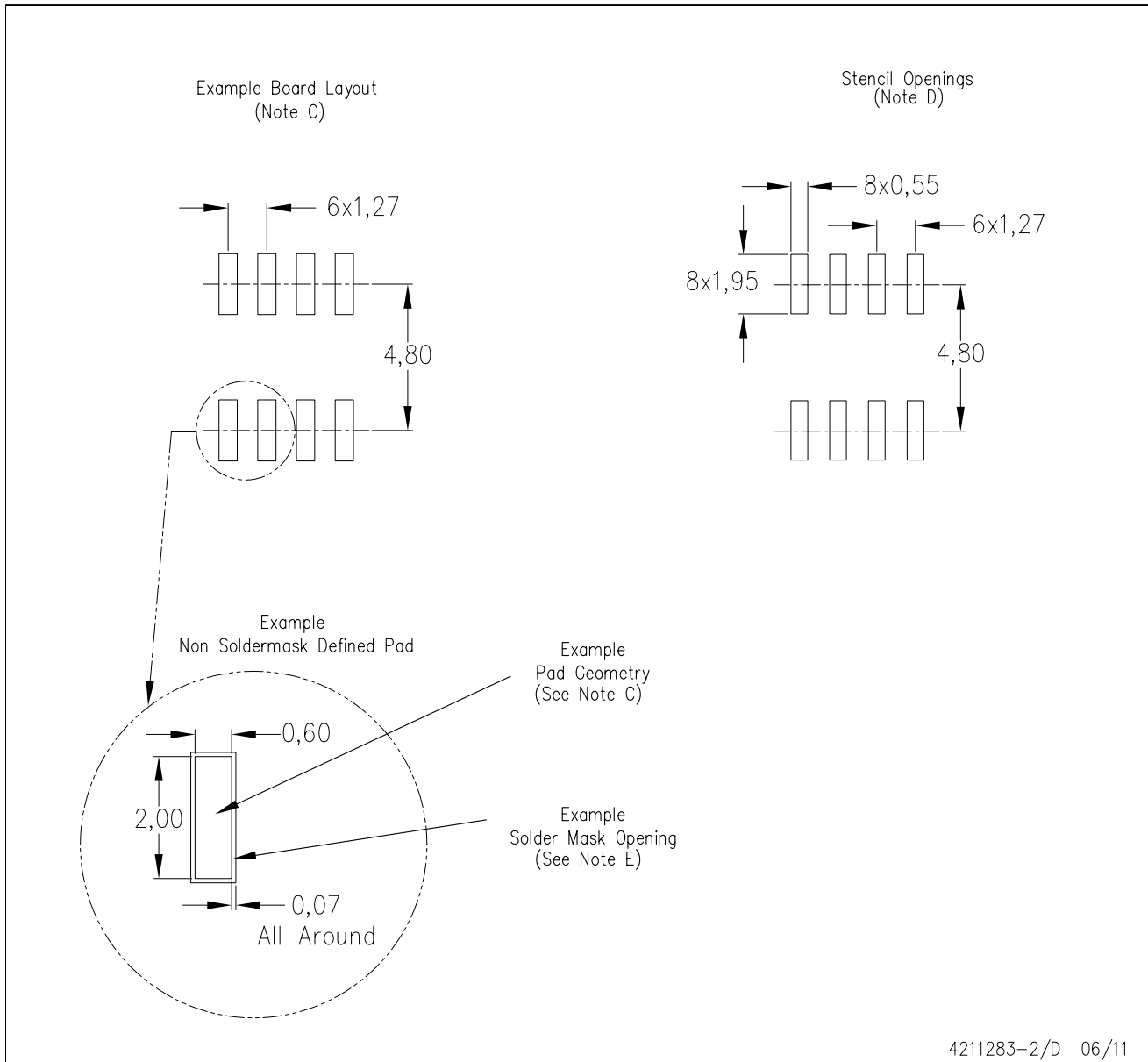
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/D 06/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated