National Semiconductor

August 2007

LP3970
Power Management Unit for Advanced Application Processor

General Description

The LP3970 is a multi-function, programmable Power Management Unit, designed especially for advanced application processors. The LP3970 is optimized for low power handheld PMU applications and provides 11 low dropout, low noise linear regulators, two DC/DC magnetic buck regulators, a back-up battery charger and 4 GPO's. A high speed serial interface is included to program individual regulator output voltages as well as on/off control.

Key Specifications

Buck Regulators

- Programmable V_{OUT} from 0.8 to 3.3V
- Up to 95% efficiency
- 650 mA output current
- ±3% output voltage accuracy

LDO's

- Programmable V_{OUT} of 1.5-3.3V
- ±3% output voltage accuracy
- 50 mA to 300 mA output current
- 100 mV dropout

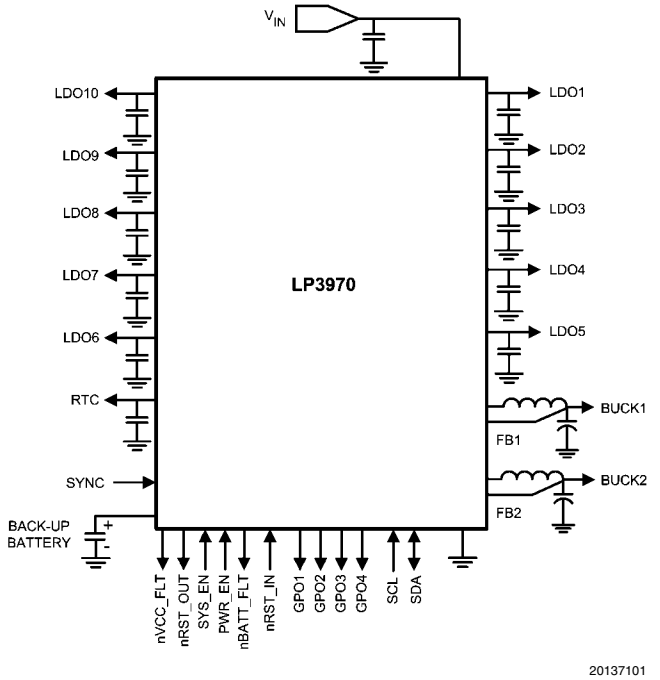
Features

- Compatible with advanced applications processors requiring dynamic voltage management (DVM)
- Two buck regulator for powering high current processor functions or peripheral devices
- Eleven LDO's for powering internal processor functions and I/O's
- Backup battery charger with automatic switching for lithium and lithium-manganese coin cell batteries
- I²C compatible high speed serial interface
- Software control of regulator functions and settings
- Thermal overload protection
- Current overload protection
- Tiny 48-Pin LLP package

Applications

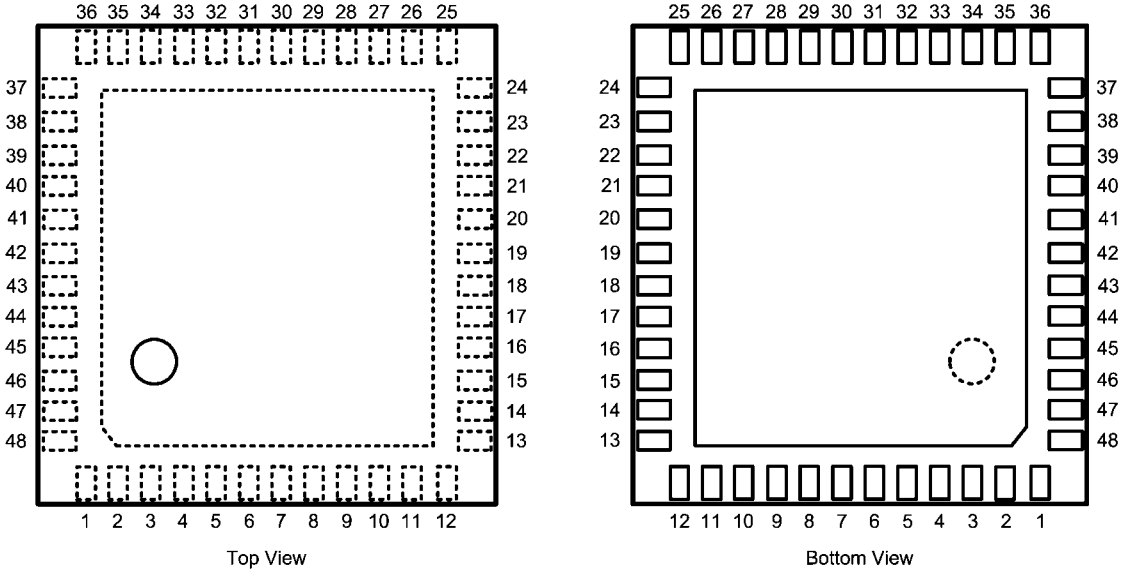
- PDA phones
- Smart phones
- Personal media players
- Digital cameras

Simplified Application Circuit



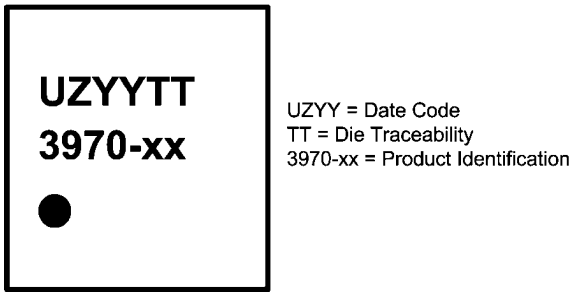
Connection Diagrams and Package Mark Information

48-Pin LLP



20137102

Package Mark



UZYY = Date Code
TT = Die Traceability
3970-xx = Product Identification

20137104

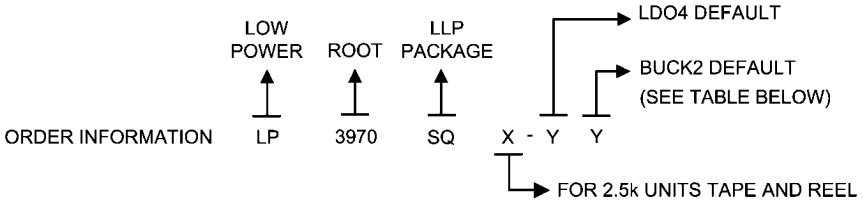
Top View

Note: Circle marks pin 1 position

Ordering Information

LDO 4 Default (V_{CC}_IO)	Buck 2 Default (V_{CC}_MEM)	Part Number	Package Marking	Transport Media	NSC Drawing
2.8	1.8	LP3970SQ-31	3970-31	250 Units Tape and Reel	SQA48A
		LP3970SQX-31		2.5k Units Tape and Reel	
2.8	3.3	LP3970SQ-35	3970-35	250 Units Tape and Reel	
		LP3970SQX-35		2.5k Units Tape and Reel	
3.0	3.0	LP3970SQ-44	3970-44	250 Units Tape and Reel	
		LP3970SQX-44		2.5k Units Tape and Reel	
3.0	3.3	LP3970SQ-45	3970-45	250 Units Tape and Reel	
		LP3970SQX-45		2.5k Units Tape and Reel	

***Contact National Semiconductor for availability**



Default V_{OUT} Coding

Y	Default V_{OUT}
1	1.8
2	2.5
3	2.8
4	3.0
5	3.3

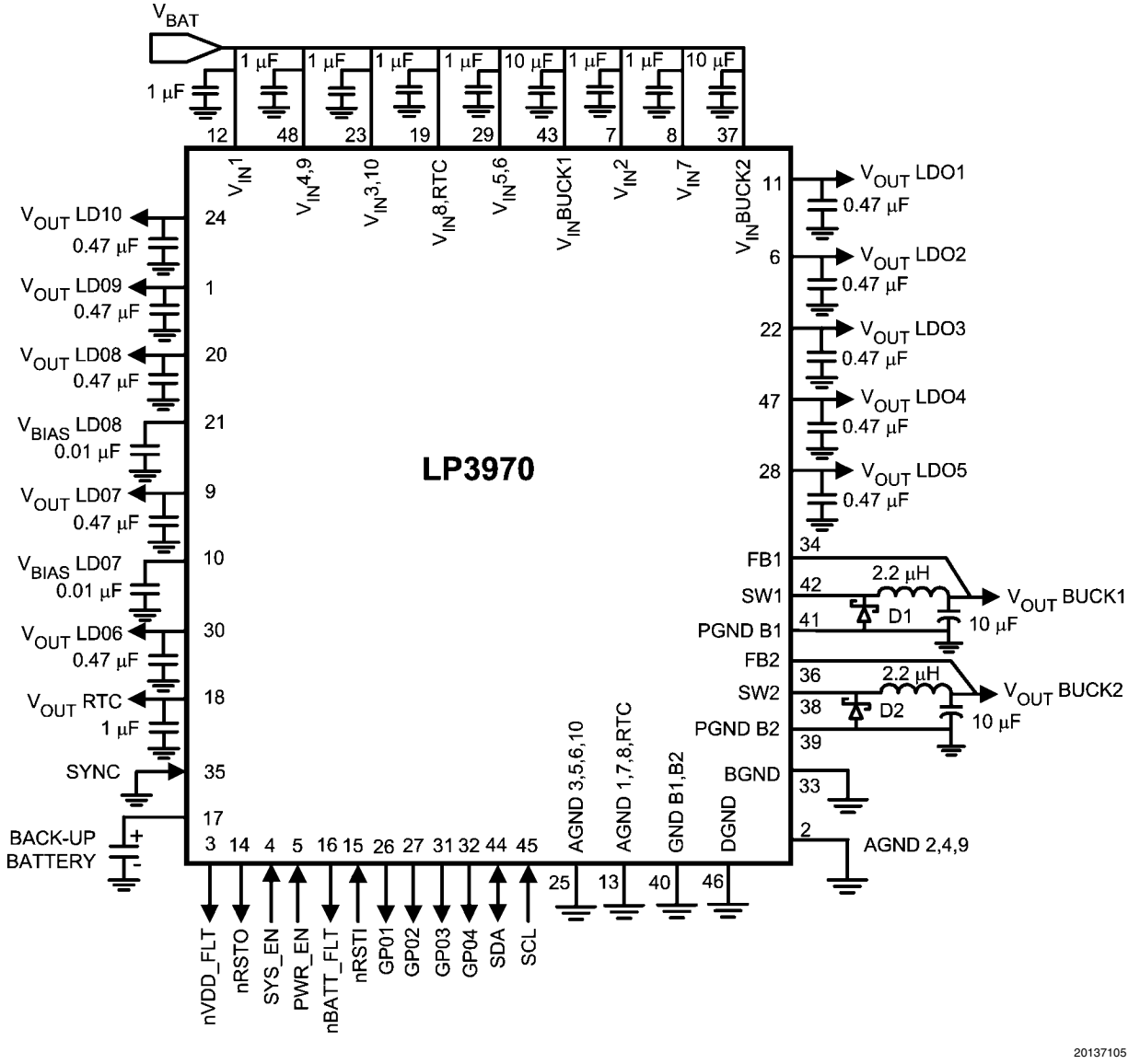
Pin Descriptions

Pin #	Name	I/O	Type	Description
1	V_{OUT} 9	O	P	LDO 9 output
2	AGND 2,4,9	G	G	Ground pin LDO's 2,4,9
3	nVDD_FLT	O	D	Regulator fault output
4	SYS_EN	I	D	High voltage domain power enable
5	PWR_EN	I	D	Low voltage domain power enable
6	V_{OUT} 2	O	A	LDO 2 output
7	V_{IN} 2	I	P	Input power terminal to LDO 2
8	V_{IN} 7	I	P	Input power terminal to LDO 7
9	V_{OUT} 7	O	P	LDO 7 Output
10	V_{BIAS} Cap LDO 7	I	A	Voltage reference bypass output. Only connect a 0.01 µF ceramic capacitor from V_{REF} to GND within 0.2 in. (5 mm) of the V_{REF} pin
11	V_{OUT} 1	O	P	LDO 1 output
12	V_{IN} 1	I	P	Input power terminal to LDO 1
13	AGND (LDO 1,7,8,RTC)	G	G	Ground pin LDO's 1, 7, 8, RTC
14	nRSTO	O	D	Output to applications processor from PMU
15	nRSTI	I	D	Input to PMU
16	nBAT_FLT	O	D	Battery fault output
17	V_{IN} BU_Batt	I	P	Back-up battery positive connection
18	V_{OUT} RTC	O	P	RTC LDO output
19	V_{IN} 8, RTC, VBAT_MON	I	P	Input power terminal to LDO's 8, RTC, battery monitor
20	V_{OUT} 8	O	P	LDO 8 output
21	V_{BIAS} Cap LDO8	I	A	Voltage reference bypass output. Only connect a 0.01 µF ceramic capacitor from V_{REF} to AGND within 0.2 in. (5 mm) of the V_{REF} pin
22	V_{OUT} 3	O	P	LDO 3 output
23	V_{IN} 3,10	I	P	Input power terminal to LDO's 3 & 10
24	V_{OUT} 10	O	P	LDO 10 output
25	AGND 3,5,6,10	G	G	Ground pin LDO's 3, 5, 6, 10
26	GPO1	O	D	General purpose CMOS output
27	GPO2	O	D	General purpose CMOS output
28	V_{OUT} 5	O	P	LDO 5 Output
29	V_{IN} 5, 6	I	P	Input power terminal to LDO's. 5 & 6
30	V_{OUT} 6	O	P	LDO 6 output
31	GPO3	O	D	General purpose CMOS Output
32	GPO4	O	D	General purpose CMOS Output
33	BGND	G	G	Ground for buck isolation
34	FB1	I	A	Feedback/V_{OUT} Buck 1
35	SYNC	I	D	System clock input for buck converters synchronization in PWM mode
36	FB2	I	A	Feedback/V_{OUT} Buck 2
37	V_{IN} B2	I	P	Input power terminal to buck 2
38	SW2	O	P	Output switch pin buck 2
39	PGND B2	G	G	NMOS power ground pin buck 2
40	GND B1 ,B2	G	G	Circuit ground SW1 and SW2
41	PGND B1	G	G	NMOS power ground pin buck 1
42	SW1	O	P	Output switch pin buck 1
43	V_{IN} B1	I	P	Input power terminal to buck 1

Pin #	Name	I/O	Type	Description
44	SDA	I/O	D	Serial interface data input/output
45	SCL	I	D	Serial interface clock input
46	DGND	G	G	Digital ground pin.
47	V_{OUT} 4	O	P	LDO 4 Output
48	V_{IN} 4, 9	I	P	Input power terminal to LDO's 4 & 9

A: Analog Pin
I: Input Pin
D: Digital Pin
I/O: Input/Output Pin
G: Ground Pin
O: Output Pin
P: Power Pin

Applications Schematic Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

All Input	−0.3 to +6V
GND to GND Slug	±0.3V
Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to 150°C
Power Dissipation (T_A = 70°C) (Note 4)	3.2W
θ_{JA}	25°C/W
Maximum Lead Temp (Soldering)	260°C
ESD Rating (Note 5)	
Human Body Model	1.0 kV
Machine Model	200V

Operating Ratings (Note 1)

V_{IN}	2.7 to 5.5V
V_{EN}	0 to (V_{IN} + 0.3V)
Junction Temperature (T_J)	−40°C to 125°C
Operating Temperature (T_A)	−40°C to 85°C
Maximum Power Dissipation (T_A = 70°C)	2.2W

General Electrical Characteristics

Unless otherwise noted, V_{IN} = 3.6, C_{IN} = 1.0 µF, C_{OUT} = 0.47 µF, C_{OUT} (V_{RTC}) = 1.0 µF ceramic, C_{BYP} = 0.1µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the entire junction temperature range for operation, −40 ≤ T_J ≤ 125°C. (Note 1), (Note 6)

Supply Specification LP3970

Supply	Supply Type	Power Domain	V_{OUT} (Volts)			I_{MAX} Maximum Output Current (mA)
			Default (V)	Range (V)	Resolution (mV)	
LDO_RTC	Digital	VBATT	**2.8**	Fixed	N/A	**5**
LDO1	Analog	V_{CC}_PLL	**1.3**	Fixed	N/A	**100**
LDO2	Digital	V_{CC}_SRAM	**1.1**	Fixed	N/A	**100**
LDO3	Digital	V_{CC}_USB	**2.8**	1.5 to 3.4	100	**150**
LDO4	Digital	V_{CC}_IO	**See Table Below**	1.5 to 3.4	100	**150**
LDO5	Digital	V_{CC}_USIM	**3.0**	1.5 to 3.4	100	**150**
LDO6	Digital	V_{CC}_BB/LCD	**2.8**	1.5 to 3.4	100	**50**
LDO7	Analog	GP Analog	**1.8**	Fixed	N/A	**100**
LDO8	Analog	GP Analog	**2.8**	1.5 to 3.4	100	**150**
LDO9	Digital	GP Digital	**2.8**	1.5 to 3.4	100	**300**
LDO10	Digital	GP Digital	**2.8**	1.5 to 3.4	100	**300**
Buck 1	Digital	V_{CC}_CORE	**1.45**	0.8 to 2.0	50	**650**
Buck 2	Digital	V_{CC}_MEM	**See Table Below**	1.8 to 3.3	100	**650**

Part Number	LDO4 Default (V)	Buck 2 Default (V)
LP3970SQ-31	2.8	1.8
LP3970SQ-35	2.8	3.3
LP3970SQ-44	3.0	3.0
LP3970SQ-45	3.0	3.3

RTC LDO

Unless otherwise noted, V_{IN} = VBATT = 3.6V C_{IN} = 1.0 µF, C_{OUT} (V_{RTC}) = 0.47 µF ceramic. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 ≤ T_J ≤ 125°C. (Note 1), (Note 6)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage, Fixed (Note1)	V_{IN} Connected, I_{LOAD} = 1 mA	**2.632**	**2.8**	**2.968**	
ΔV_{OUT}	Line Regulation	V_{IN} = (V_{OUT} + 0.3V) to 5.5V Load Current = I_{MAX}			**0.15**	%/V
	Load Regulation	V_{IN} = 3.6V, Load Current = 1 mA to I_{MAX}			**0.05**	%/mA
I_{MAX}	Load Current	V_{IN} = V_{OUT} +0.3 to 5.5V			**5**	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0V		35		mA
V_{IN} - V_{OUT}	Dropout Voltage	Load Current = I_{MAX} (Note 7)		220	**375**	mV
I_{Q}_Max	Maximum Quiescent Current	I_{OUT} = 0 mA		40		µA
C_O	Output Capacitor	Capacitance for Stability	**0.7**	1		µF
		ESR	**5**		**500**	mΩ

Common Performance Specifications LDO 1 to 10

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 1.0 µF, C_{OUT} = 0.47 µF, C_{BYP} = 0.1 µF. Typical values and limits appearing in normal type apply for T_J= 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 ≤ T_J ≤ 125°C. (Note 1), (Note 6)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	LDO 1 Output Voltage Accuracy (Default V_{OUT})	I_{LOAD} = 1 mA	**1.2285**	1.3	**1.3715**	V
	LDO 2 Output Voltage Accuracy (Default V_{OUT})	I_{LOAD} = 1 mA	**1.056**	1.1	**1.144**	
	LDO 3-10 Output Voltage Accuracy (Default V_{OUT})	I_{LOAD} = 1 mA	**−3**		**+3**	%
ΔV_{OUT}	Line Regulation	V_{IN} = (V_{OUT} +0.3) to 5.5V, Load Current = I_{MAX} (Note 2)			**0.15**	%/V
	Load Regulation LDO 1,2,7	V_{IN} = 3.6V, Load Current = 1 mA to I_{MAX}			**0.015**	%/mA
	Load Regulation LDO 3,4,5,8				**0.011**	
	Load Regulation LDO 6				**0.075**	
	Load Regulation LDO 9,10				**0.006**	
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0V		400		mA
V_{IN} - V_{OUT}	Dropout Voltage	Load Current = 50 mA (Note 7)			**150**	mV
PSRR	Digital Supply Ripple Rejection	f = 10 kHz, Load Current = I_{MAX}		45		dB
PSRR	Analog Supply Ripple Rejection	f = 10 kHz, Load Current = I_{MAX}		60		dB
θn	Analog Supply Output Noise Voltage	10 Hz < F < 100 kHz		80		uVrms
Analog I_Q	Quiescent Current “On”	I_{OUT} = 0 mA		40	**80**	µA
		I_{OUT} = I_{MAX}		60	**130**	
	Quiescent Current “Off”	EN is de-asserted		0.03		
Digital I_Q	Quiescent Current “On”	I_{OUT} = 0 mA		40	**95**	µA
		I_{OUT} = I_{MAX}		60	**180**	
	Quiescent Current “Off”	EN is de-asserted		0.03		
T_{ON}	Turn On Time	Start up from Shut-down (Note 10)			**300**	µsec
T_{SD}	Thermal Shutdown	Temperature		160		°C
		Hysteresis		20		

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{OUT}	Output Capacitance LDO 1	Capacitance for Stability	**0.33**	0.47		µF
	Output Capacitance LDO 2 - 10	Capacitance for Stability °C ≤ T_J ≤ 125°C	**0.33**	0.47		
		–40 ≤ T_J ≤ 125°C	**0.68**	1		
	Output Capacitor LDO 1 - 10	ESR	**5**		**500**	

Buck Converters SW1, SW2

Unless otherwise noted, V_{IN} = VBATT = 3.6V C_{IN} = 10 µF, C_{OUT} = 10 µF, L_{OUT} = 2.2 µH Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, –40 ≤ T_J ≤ 125°C. (Note 1), (Note 6)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Accuracy	Default V_{OUT}	**3**		**3**	%
Eff	Efficiency	Load Current = 200 mA		90		%
I_{SHDN}	Shutdown Supply Current	EN is de-asserted		0.1		µA
	Sync Mode Clock Frequency	Synchronized from 13 MHz System Clock		1.6		MHz
f_{OSC}	Internal Oscillator Frequency		**1.1**	1.6	**2.0**	MHz
I_{PEAK}	Peak Switching Current Limit	(Open Loop)		850		mA
I_Q	Quiescent Current “On”	No Load PFM Mode		33	**55**	µA
		No Load PWM Mode		200		
R_{DSON} (P)	Pin-Pin Resistance PFET			400	**675**	mΩ
R_{DSON} (N)	Pin-Pin Resistance NFET			250	**500**	mΩ
T_{ON}	Turn On Time	Start up from Shut-down		500		µsec
T_{SD}	Thermal Shutdown	Temperature		150		°C
		Hysteresis		20		
C_{IN}	Input Capacitor	Capacitance for Stability	10			µF
C_O	Output Capacitor	Capacitance for Stability	10			µF

Back-Up Charger Electrical Characteristics

Unless otherwise noted, V_{IN} = VBATT = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, –40 ≤ T_J ≤ 125°C. (Note 1), (Note 6), (Note 8)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Operational Voltage Range	Voltage at V_{IN}	**3.3**		**5.5**	V
I_{OUT}	Backup Battery Charging Current (Default Setting)	V_{IN} = 3.6V, Backup_Bat = 2.5V, Backup Battery Charger Enabled		500		µA
V_{OUT}	Charger Termination Voltage	V_{IN} = 5.5V Backup Battery Charger Enabled	**2.8**	3.0	**3.2**	V
	Backup Battery Charger Short Circuit Current	Backup_Bat = 0V, Backup Battery Charger Enabled		9		mA
PSRR	Power Supply Ripple Rejection Ratio	I_{OUT} ≤ 50 µA, V_{OUT} = 3.15V V_{OUT} + 0.4 ≤ VBATT = V_{IN} ≤ 5.5V f < 10 kHz		15		dB
I_Q	Quiescent Current	I_{OUT} < 50 µA		25		µA

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 100 µA		0.1		µF
	Output Capacitor ESR		**5**		**500**	MΩ

Logic Inputs DC Operating Conditions

Logic input specifications applies to SYS_EN, PWR_EN and nRSTI.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage				**0.4**	V
V_{IH}	High Level Input Voltage		**1.6**			V
I_{LEAK}	Input Leakage Current			0.01		µA

Logic Output DC Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output Low Level				**0.4**	V
V_{OH}	Output High Level		**2.3**			V
I_{LEAK}	Output Leakage Current				**+5**	µA

GPO Logic Output DC Operating Conditions

The LP3970 contains four (4) general purpose CMOS outputs (GPO) connected to the V_{DD}_RTC. Each GPO can be set to high impendence (HiZ), logic high (V_{OH}), or logic low (V_{OL}) by using the serial interface. The default setting is HiZ

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output Low Level				**0.4**	V
V_{OH}	Output High Level		**2.1**			V
V_{HZ}	Logic Current in High Z Mode	$V_{IN} = V_{RTC}/2$			**5**	µA

nBATT_FLT DC Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
	nBATT_FLT Default Voltage			2.8		
	nBATT_FLT Threshold Voltage	Programmable via serial data port	2.5		3.5	V
V_{OL}	Output Low Level				**0.4**	V
V_{OH}	Output High Level		**2.3**			V
I_{LEAK}	Input Leakage Current				**+5**	µA

I²C Compatible Serial Interface Electrical Specifications

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the entire junction temperature range for operation, –40°C ≤ T_J ≤ 125°C. (Note 1), (Note 6), (Note 9)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage		–0.5		0.3 V_{RTC}	V
V_{IH}	High Level Input Voltage		0.7V_{RTC}		V_{RTC}	
V_{OL}	Low Level Output Voltage		0		0.2 V_{TRC}	
I_{OL}	Low Level Output Current	V_{OL} = 0.4V	3.0			mA
FCLK	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time Between Start and Stop		1.3			µs
t_{HOLD}	Hold Time Repeated Start Condition		0.6			µs
t_{CLKLP}	CLK Low Period		1.3			µs
t_{CLKHP}	CLK High Period		0.3			µs
t_{SU}	Set Up Time Repeated Start Condition		0.6			µs

Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_{DATAHLD}$	Data Hold Time		0			µs
t_{CLKSU}	Data Set Up Time		100			µs
T_{SU}	Set Up Time for Start Condition		0.6			µs
T_{TRANS}	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both DATA & CLK Signals			50		ns

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: LDO 1,2,7 Line Regulation Specified as V_{IN} = 2.5V to 5.5V I_{LOAD}= I_{MAX}. Specification does not apply to LDO 1.

Note 3: All voltages are with respect to the potential at the GND pin.

Note 4: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125°C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: TA-MAX = TJ-MAX-OP – (θ_{JA} x PD-MAX).

Note 5: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (JESD22-A114C) The machine model is a 200 pF capacitor discharged directly into each pin. (EAIJ)

Note 6: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are production tested, guaranteed through statistical analysis or guaranteed by design. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 7: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. Dropout specification does not apply to LDO 1,2,6,7.

Note 8: Back-up battery charging current is programmable via the I²C compatible interface. Refer to the Application Section for more information.

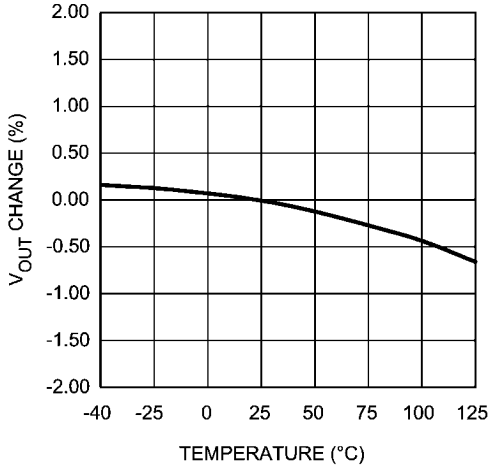
Note 9: Both I²C compatible signals from the applications processor have alternate functions as GPIO's. Following cold-start power-on or a hard reset both signals default to GPIO"s. An internal pull-down resistor on each signal prevents them from floating during reset or power-on events. The I²C signals behave like open-drain outputs and require an external pull-up resistor on the system module in the 2 kΩ to 20 kΩ range. The I²C signals from the processor are pulled low after power-up or reset.

Note 10: C_{BYP} not connected to LDO 7 & 8. Use of a C_{BYP} capacitor will increase the LDO's start-up time.

Note 11: Test Condition: for V_{out} less than 2.5V, V_{in} = 3.6V; for V_{out} greater than or equal to 2.5V, V_{IN} = V_{out} + 1V.

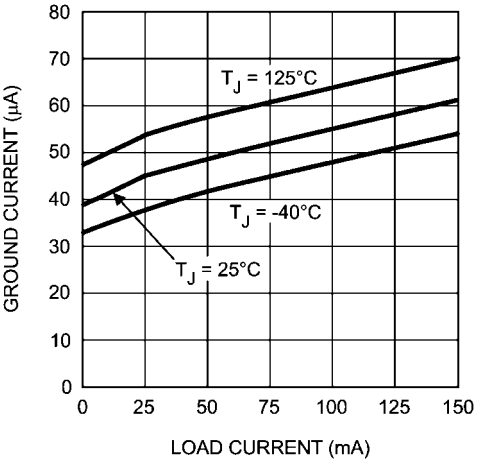
Typical Performance Characteristics — LDO Characteristics

Output Voltage Change vs. Temperature



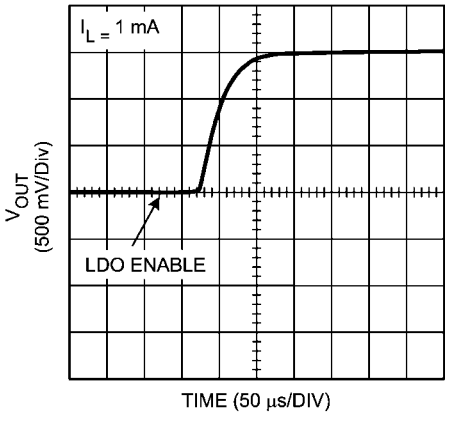
20137123

Ground Current vs. Load Current



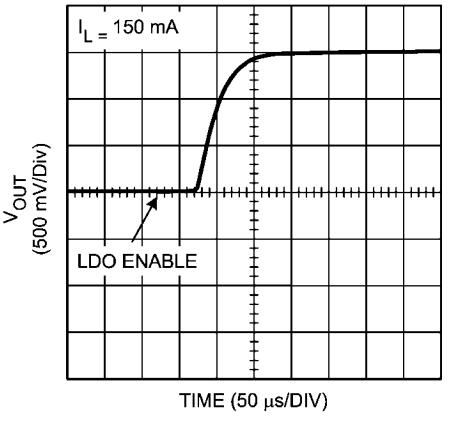
20137124

Enable Start-Up Time



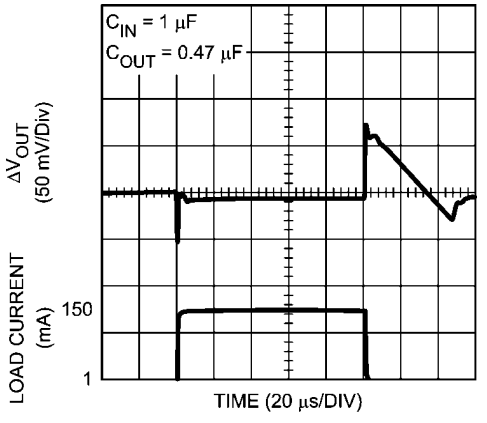
20137125

Enable Start-Up Time



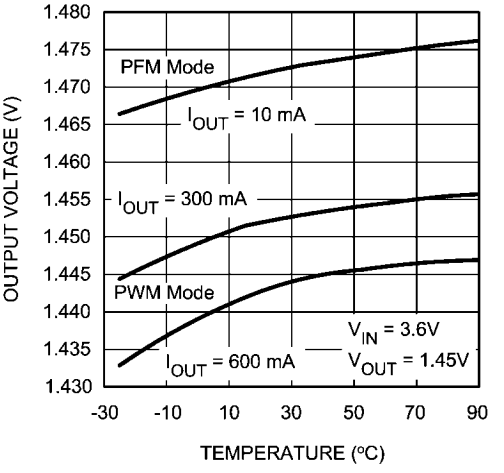
20137126

Load Transient



20137127

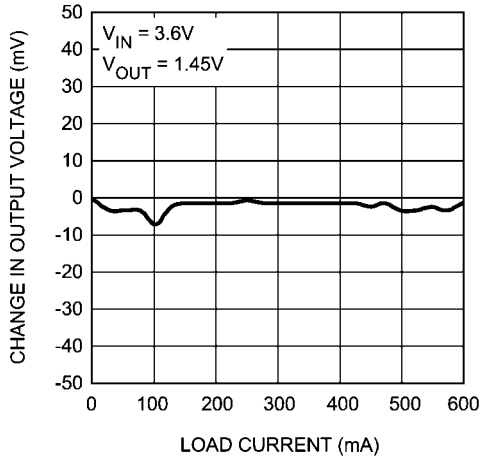
Output Voltage vs. Temperature, V_{OUT} = 1.45V)



20137128

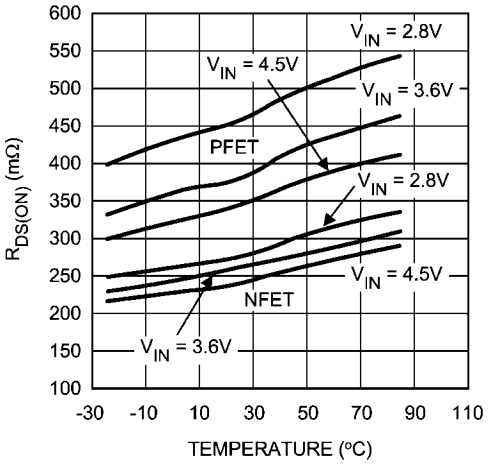
Typical Performance Characteristics — Buck Converter Characteristics

Buck1 Change in Output Voltage vs. Load Current



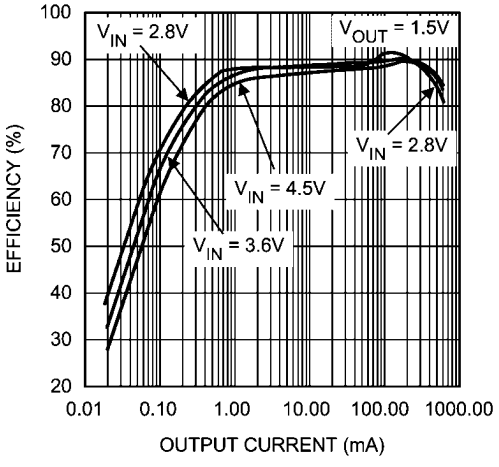
20137129

R_{DSON} vs. Temperature



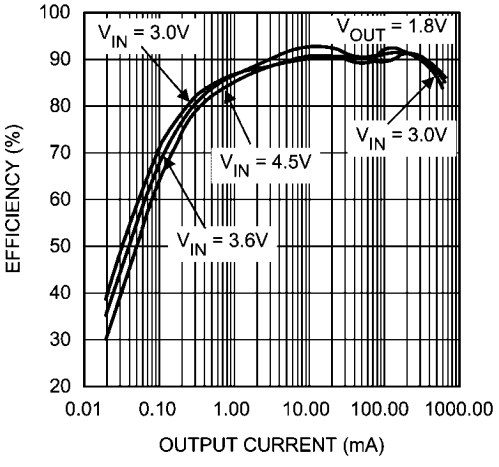
20137130

Efficiency vs. Output Current (V_{OUT} = 1.45V, L = 2.2 µH)



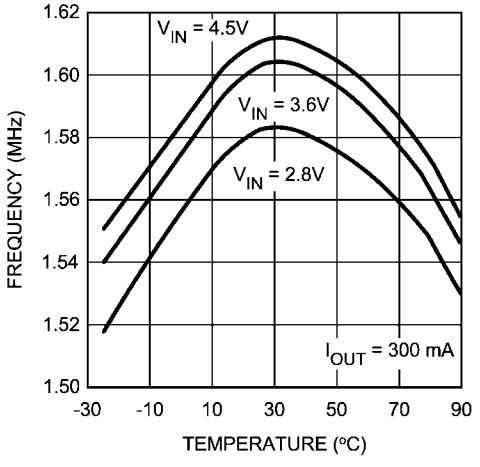
20137131

Efficiency vs. Output Current (V_{OUT} = 1.8V, L = 2.2 µH)



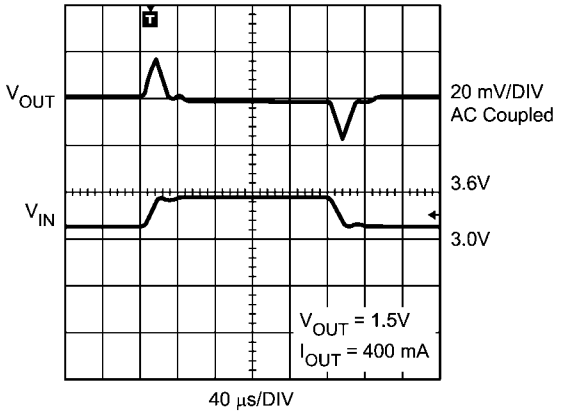
20137132

Switching Frequency vs. Temperature



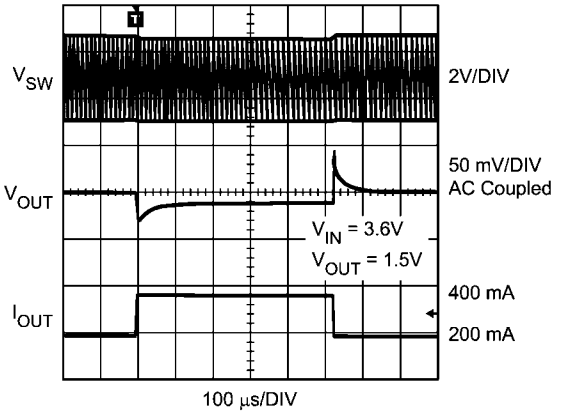
20137133

Line Transient Response (PWM Mode)



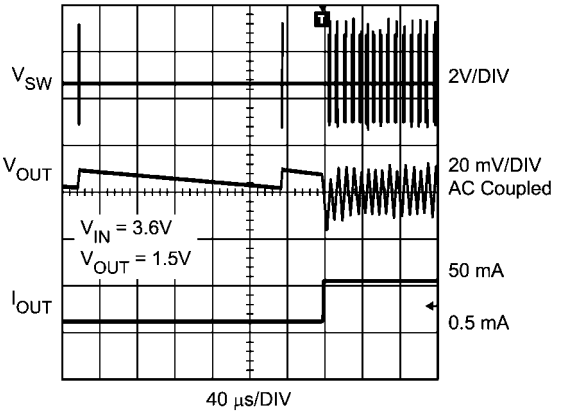
20137134

Load Transient Response (PWM Mode)



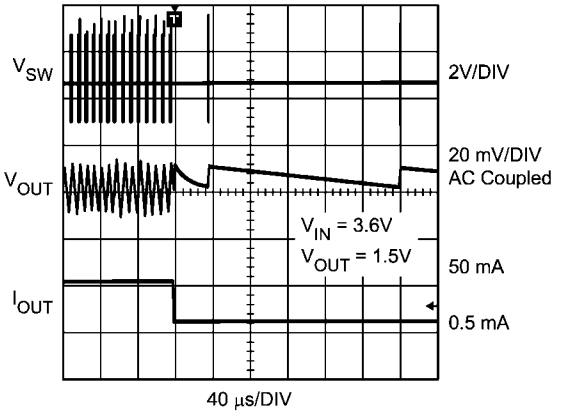
20137135

Load Transient Response (PFM Mode 0.5 mA to 50 mA)



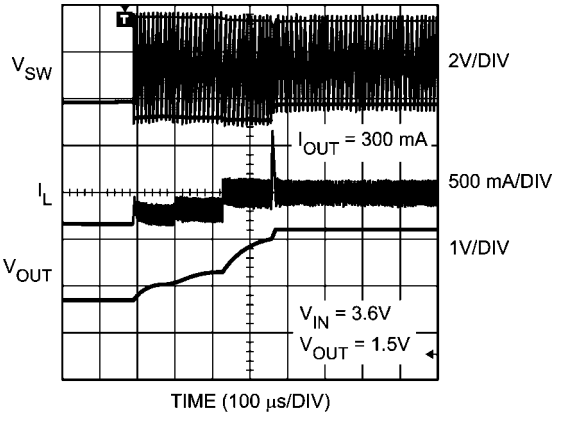
20137136

Load Transient Response (PFM Mode 50 mA to 0.5 mA)



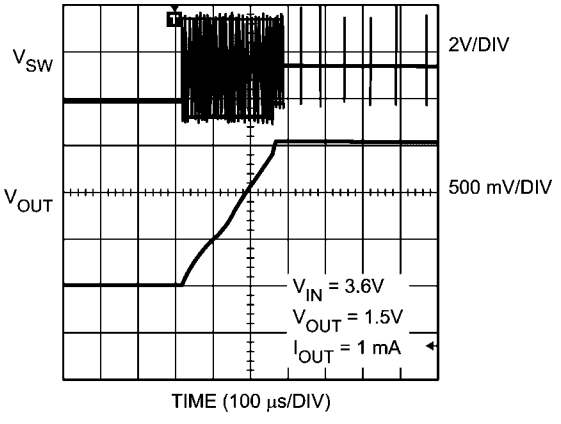
20137137

Start Up into PWM Mode (Output Current = 300 mA)



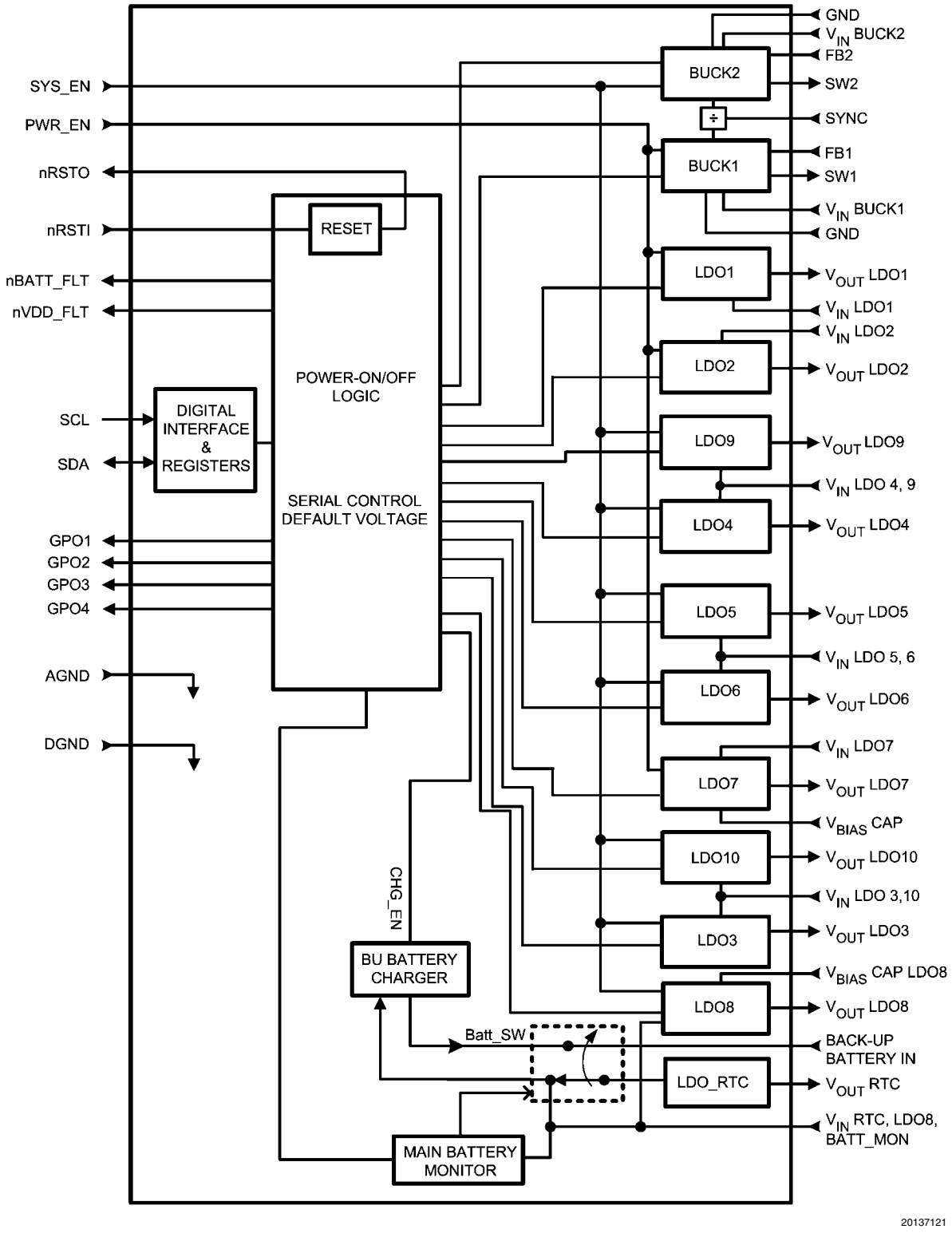
20137138

Start Up into PFM Mode (Output Current = 1 mA)



20137139

Functional Block Diagram



Buck Converter Operation

DEVICE INFORMATION

The LP3970 includes two high efficiency step down DC-DC switching buck converters. Using a voltage mode architecture with synchronous rectification, the buck converters have the ability to deliver up to 600 mA depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

There are three modes of operation depending on the current required - PWM, PFM, and shutdown. The device operates in PWM mode at load currents of approximately 80 mA or higher, having voltage tolerance of ±4% with 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM for reduced current consumption. Shutdown mode turns off the device, offering the lowest current consumption ($I_{Q,\ SHUTDOWN}$ = 0.01 µA typ).

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 2.8V or higher.

CIRCUIT OPERATION

The buck converters operates as follows. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN}–V_{OUT})/L, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of - V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

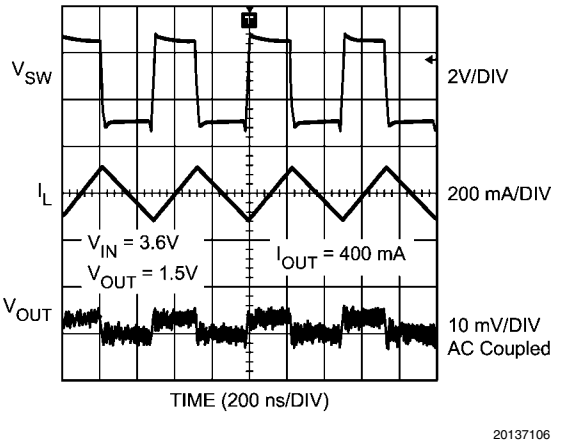


FIGURE 1. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the converters uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the converters to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 850 mA (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A: The inductor current becomes discontinuous.

B: The peak PMOS switch current drops below the I_{MODE} level, (Typically I_{MODE} < 30 mA + V_{IN}/42Ω).

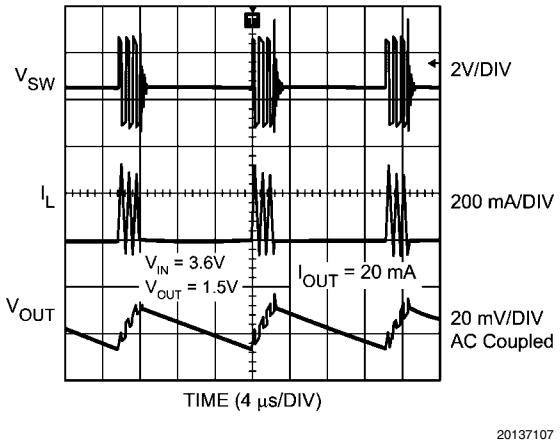


FIGURE 2. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.6% and ~1.7% above the nominal PWM output voltage. If the output voltage is below the "high" PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the IPFM level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112 mA + $V_{IN}/27\Omega$.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see *Figure 3*), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 16 µA (typ), which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage (average voltage in PFM mode) to ~1.15% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see *Figure 3*) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode. When V_{IN} = 2.8V the part transitions from PWM to PFM mode at ~35 mA output current and from PFM to PWM mode at ~85 mA , when V_{IN} = 3.6V, PWM to PFM transition happens at ~50 mA and PFM to PWM transition happens at ~100 mA, when V_{IN} = 4.5V, PWM to PFM transition happens at ~65 mA and PFM to PWM transition happens at ~115 mA.

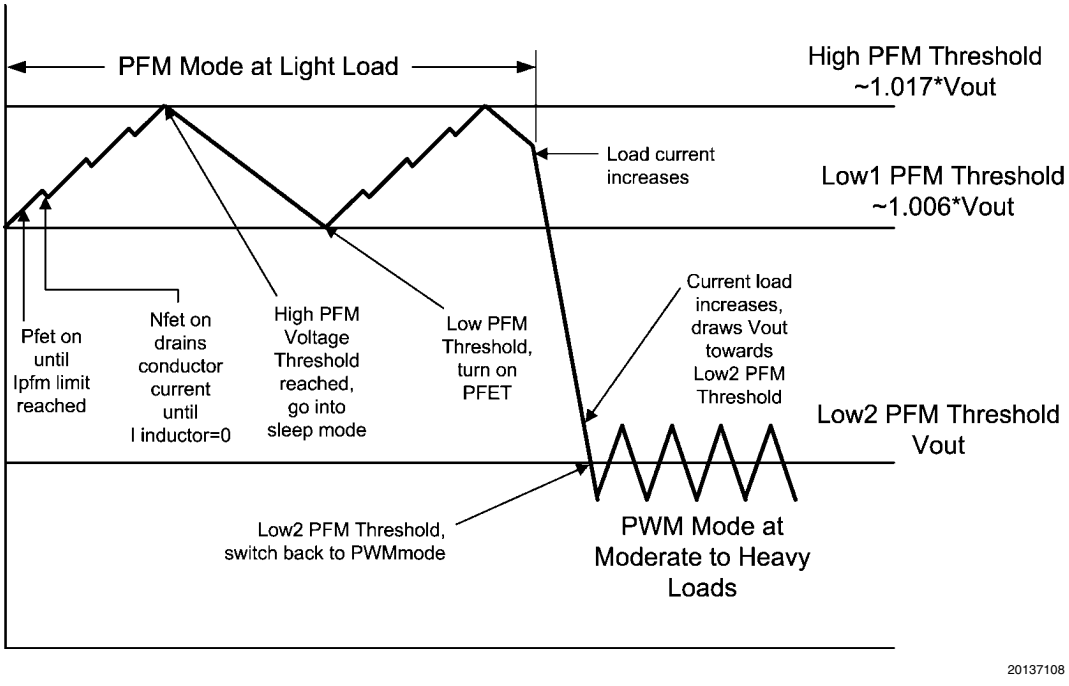


FIGURE 3. Operation in PFM Mode and Transfer to PWM Mode

SHUTDOWN MODE

During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the converters are turned off. When the converter is enabled, EN, soft start is activated. It is recommended to disable the converter during the system power up and undervoltage conditions when the supply is less than 2.8V.

SOFT START

The buck converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.8V. Soft start is implemented by increasing switch current limit in steps of 70 mA, 140 mA, 280 mA and 1020 mA (typ. switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with 22 µF output capacitor and 300 mA load current is 400 µs and with 1 mA load current its 275 µs.

LDO - LOW DROP OUT OPERATION

The buck converter can operate at 100% duty cycle (no switching, PMOS switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

The minimum input voltage needed to support the output voltage is

$$V_{IN,\,MIN} = I_{LOAD} * (R_{DSON,\,PFET} + R_{INDUCTOR}) + V_{OUT}$$

- I_{LOAD} Load Current
- $R_{DSON,\,PFET}$ Drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ Inductor resistance

Power Controller Interface Signals

Signal	Definition	Active State	Signal Direction (x)
PWR_EN	Low voltage power enable	High	Input
SYS_EN	High voltage power enable	High	Input
PWR_SCL	Serial bus clock	Clock	Input
PWR_SDA	Serial bus data		Bidirectional
nRSTI	Forces an unconditional hardware reset	Low	Input
nRSTO	Forces an unconditional hardware reset	Low	Output
nBATT_FLT	Indicates main battery removed or discharged	Low	Output
nVDD_FLT	Indicates one or more supplies are out of regulation	Low	Output

nRSTI Forces an unconditional reset when activated from a momentary contact push button switch.

nRSTO is an active-low signal from the PMU to the Applications processor that tells the processor to enter the hardware-reset state. nRSTO is asserted for a cold start power-on or if the reset button is pushed. The PMU must assert nRSTO for both events. nRSTO will remain asserted for a minimum of 50 ms.

PWR_EN is an active-high input to the PMU from the Applications processor that enables the low voltage power supplies (V_{CC}_CORE, V_{CC}_SRAM, and V_{CC}_PLL).

SYS_EN is an active-high input to the PMU from the Applications processor that enables the high voltage power supplies (V_{CC}_IO, V_{CC}_LCD, V_{CC}_MEM, V_{CC}_USIM, V_{CC}_BB, and V_{CC}_USB).

nVDD_FLT signals the Applications processor that one or more of it's enabled supplies are below the minimum regulation limit (supplies that are not enabled do not cause nVDD_FLT assertion).

Power Enables

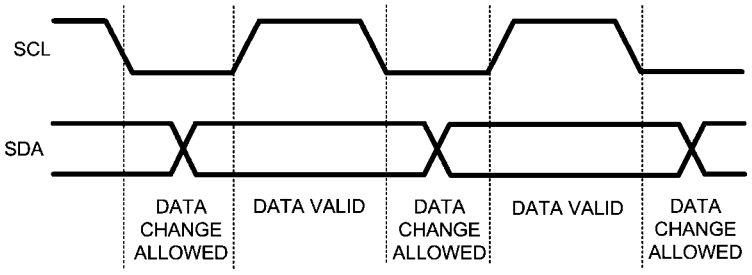
PMU Output	Enable	Applications Input	Supply Reference
LDO_RTC	None	V_{CC}_BAT	Sleep-control subsystem. oscillators, and real-time clock
LDO1	PWR_EN	V_{CC}_PLL	Phase locked loops
LDO2	PWR_EN	V_{CC}_SRAM	Internal SRAM
LDO3	SYS_EN	V_{CC}_USB	Differential USB interface
LDO4	SYS_EN	V_{CC}_IO	Peripheral input/output
LDO5	SYS_EN	V_{CC}_USIM	USIM interface
LDO6	SYS_EN	V_{CC}_BB/LCD	Baseband interface, LCD input/output
LDO7	PWR_EN	Peripheral	AUX1, GP Analog
LDO8	SYS_EN	Peripheral	AUX2, GP Analog
LDO9	SYS_EN	Peripheral	AUX3, GP Digital
LDO10	SYS_EN	Peripheral	AUX4, GP Digital

PMU Output	Enable	Applications Input	Supply Reference
SW1	PWR_EN	V_{CC}_CORE	CPU Core
SW2	SYS_EN	V_{CC}_MEM	Memory controller input/output

I²C Compatible Interface

I²C DATA VALIDITY

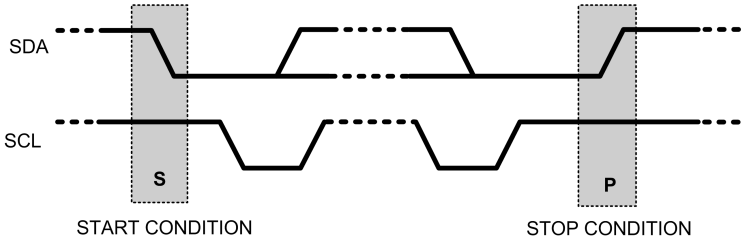
The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



20137109

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



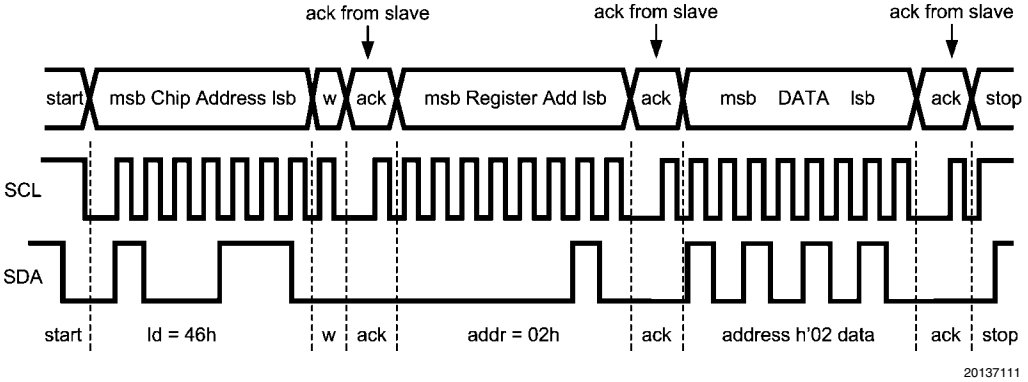
20137110

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, a chip address is sent by the I²C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3970 address is 46h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

I²C Write Cycle



20137111

w = write (SDA = “0”)

r = read (SDA = “1”)

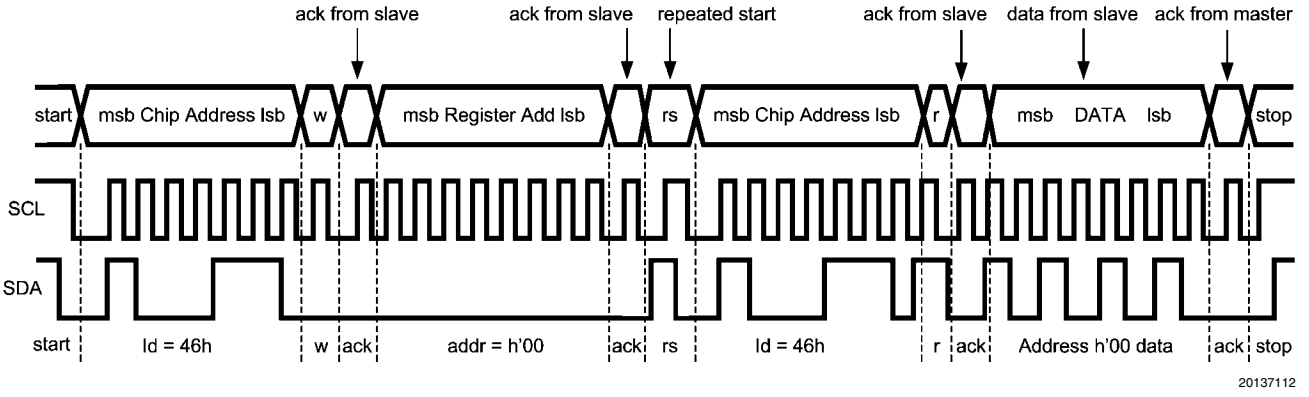
ack = acknowledge (SDA pulled down by either master or slave)

rs = repeated start

xx = 46h

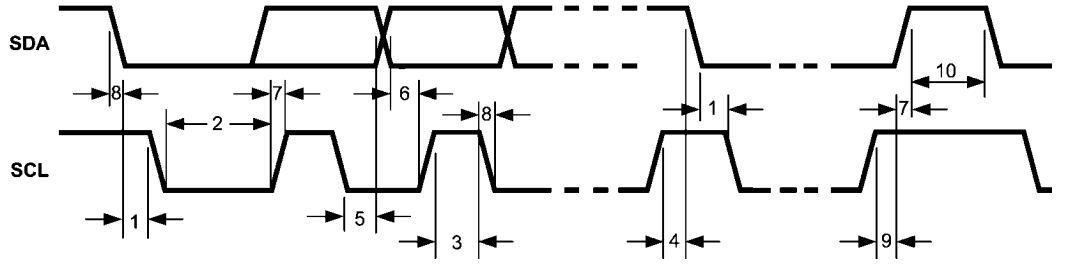
However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in Figure 5.

I_2C Read Cycle



20137112

I^2C Timing Diagram



20137113

LP3970 Serial Port Communication Address Code 7h'46

1	0	0	0	1	1	0	R/W

LP3970 Control and Data Codes

Numbers in parentheses indicate default setting. **(0)** bit is set to low state and**(1)** bit is set to high state. R/O –Read Only, All other bits are Read and Write.

Addrs	Register	7	6	5	4	3	2	1	0
8h'0	Enable 0	LDO8–EN (1)	LDO7–EN (1)	LDO6–EN (1)	LDO5–EN (1)	LDO4–EN (1)	LDO3–EN (1)	LDO2–EN (1)	LDO1_EN (1)
8h'01	Enable 1	Not used (0)	Not used (0)	Not used (0)	Not used (0)	Buck2_EN (1)	Buck1_EN (1)	LDO10_EN (1)	LDO9_EN (1)
8h'02	GPO Control	GPO4 nHZ EN (0)	GPO4 EN (0)	GPO3 nHZ EN (0)	GPO3 EN (0)	GPO2 nHZ EN (0)	GPO2 EN (0)	GPO1 nHZ EN (0)	GPO1 EN (0)
8h'03	LDO3 Data Code	Not used (0)	Not used (0)	Not used (0)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (0)	V_{OUT} (1)
8h'04	LDO4 Data Code	Not used (0)	Not used (0)	Not used (0)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (0)	V_{OUT} (1)
8h'05	LDO5 Data Code	Not used (0)	Not used (0)	Not used (0)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (1)
8h'06	LDO6 Data Code	Not used (0)	Not used (0)	Not used (0)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (0)	V_{OUT} (1)
8h'08	LDO8 Data Code	Not used (0)	Not used (0)	Not used (0)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (0)	V_{OUT} (1)
8h'09	LDO9 Data Code	Not used (0)	Not used (0)	Not used (0)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (0)	V_{OUT} (1)
8h'0A	LDO10 Data Code	Not used (0)	Not used (0)	Not used (0)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (0)	V_{OUT} (1)
8h'0B	Buck1 Data Code	Not used (0)	Ext_clk EN (0)	nStep_EN (1)	V_{OUT} (0)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (1)	V_{OUT} (0)
8h'0C	Buck2 Data Code	Not used (0)	Ext_clk EN (0)	nStep_EN (1)	V_{OUT} (0)	V_{OUT} (0)	V_{OUT} (0)	V_{OUT} (0)	V_{OUT} (1)
8h'0D	Back Up Battery Charger	nBU_Bat EN (0)	nBat_FLT EN (0)	BAT_FLT Voltage (0)	BAT_FLT Voltage (1)	BAT_FLT Voltage (0)	nBU_Bat Charger Enable (0)	BU_Bat Charger Current (0)	BU_Bat Charger Current (1)

Output Voltage Selection Codes			
Data Code	LDO's	Buck_1 (V)	Buck _2 (V)
5h'00	1.5	N/A	N/A
5h'01	1.6	0.80	1.8
5h'02	1.7	0.85	1.9
5h'03	1.8	0.90	2.0
5h'04	1.9	0.95	2.1
5h'05	2.0	1.00	2.2
5h'06	2.1	1.05	2.3
5h'07	2.2	1.10	2.4
5h'08	2.3	1.15	2.5
5h'09	2.4	1.20	2.6
5h'0A	2.5	1.25	2.7
5h'0B	2.6	1.30	2.8
5h'0C	2.7	1.35	2.9
5h'0D	2.8	1.40	3.0
5h'0E	2.9	1.45	3.1
5h'0F	3.0	1.50	3.2
5h'10		1.55	3.3
5h'11		1.60	
5h'12		1.65	
5h'13		1.70	
5h'14		1.75	
5h'15		1.80	
5h'16		1.85	
5h'17		1.90	
5h'18		1.95	
5h'19		2.00	
5h'1A			
5h'1B			
5h'1C	3.1		
5h'1D	3.2		
5h'1E	3.3		
5h'1F	3.4		

nBATT_FLT Threshold Voltage Voltage Selection Codes		
Bold face voltages are default values		
Data Code	**De-asserted**	**Asserted**
3h'00	2.4	2.6
3h'01	2.6	2.8
3h'02	**2.8**	**3.0**
3h'03	3.0	3.2
3h'04	3.2	3.4
3h'05	3.4	3.6

Battery Monitoring

When Back-Up battery is connected but Main battery removed or voltage too low, LP3970 uses Back-Up Battery for generating LDO_RTC voltage. When Main Battery is available the battery switch changes main battery for LDO_RTC voltage and Back-Up Battery charger starts charging. User can set the battery fault determination voltage and battery charging current via I²C compatible interface.

BU Charger Current Selection Code	
Data Code	**I_{SET} (µA)**
2h'00	375
2h'01	**500**
2h'02	625

Power On Sequence

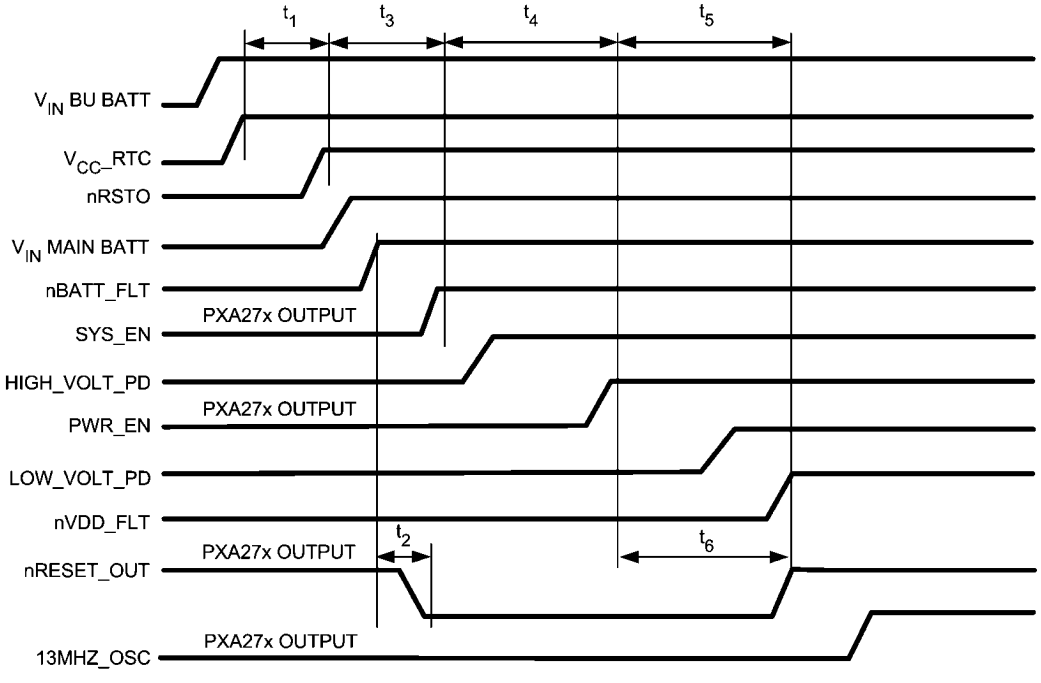
The Power Management Unit (PMU) supplies both high-voltage (I/O) and low-voltage power to the Applications processor. There are two power control signal inputs to the LM3970 PMU. SYS_EN controls the high-voltage supplies and PWR_EN controls the low-voltage supplies. When the back-up battery is installed, the processor begins the initial cold-start, power-up sequence enabling its internal power management unit and one oscillator.

The LP3970 will monitor voltages and generate the nBATT_FLT and nVDD_FLT signals. The LP3970 will assert both nBATT_FLT and nVDD_FLT until V_{IN} is above the default threshold voltage.

INITIAL COLD START POWER ON SEQUENCE

1. The Back up battery is connected to the PMU, power is applied to the back-up battery pin, the RTC_LDO turns on and supplies a stable output voltage to the V_{CC}_BATT pin of the Applications processor (initiating the power-on reset event) with nRSTO asserted from the LP3970 to the processor.
2. nRSTO de-asserts after a minimum of 50 mS.
3. The Applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is applied, the LP3970 de-asserts nBATT_FLT.
5. The Applications processor asserts SYS_EN, the LP3970 enables the system high-voltage power supplies. The Applications processor starts its countdown timer set to 125 mS
6. The LP3970 enables the high-voltage power supplies.
7. Countdown timer expires; the Applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer set to 125 mS period.
8. The Applications processor asserts PWR_EN, the LP3970 enables the low-voltage regulators.
9. Countdown timer expires; If nVDD_FLT is de-asserted the power up sequence continues by enabling the processors 13 MHz oscillator and PLL's.
10. The Applications processor begins the execution of code.

Cold Start Power on Timing



20137114

Power-On Timing Specifications

Symbol	Description	Min	Typ	Max	Units
t_1	Delay from V_{CC}_RTC assertion to nRSTO de-assertion	50			ms
t_2	Delay from nBATT_FLT de-assertion to nRESET assertion		100		µs
t_3	Delay from nRST de-assertion to SYS_EN assertion		10		ms
t_4	Delay from SYS_EN assertion to PWT_EN assertion		125		ms
t_5	Delay from PWR_EN assertion to nVDD_FLT de-assertion			120	ms
t_6	Delay from PWR_EN assertion to nRST_OUT de-assertion		125		ms

Hardware Reset Sequence

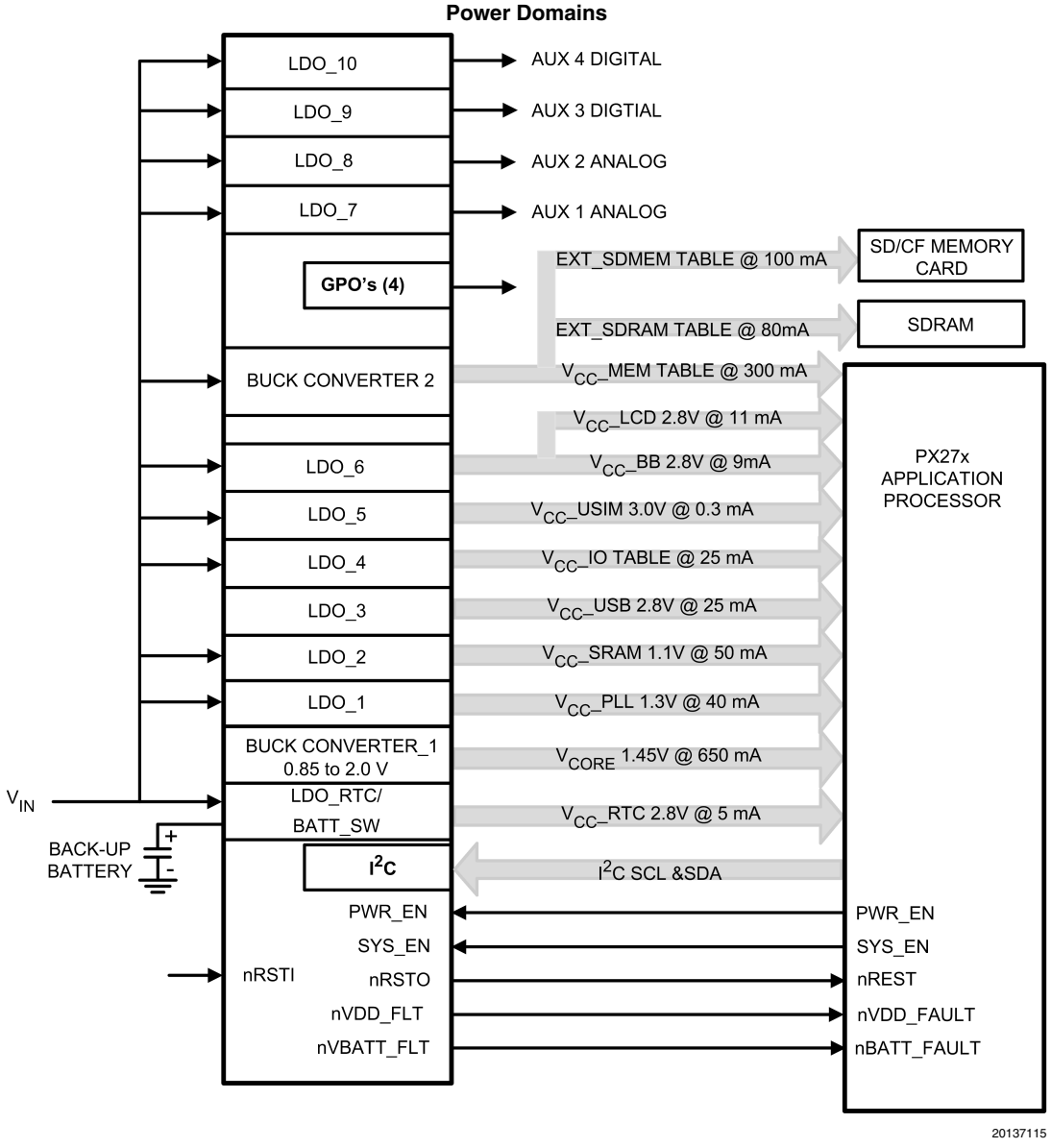
Hardware reset initiates when the nRSTI signal is asserted (low). Upon assertion of nRST the processor enters hardware reset state. The LP3970 must hold the nRST low long enough to allow the processor time to initiate the reset state, which is a minimum of 50 ms

RESET SEQUENCE

1. nRSTI is asserted
2. nRSTO is asserted and will de-asserts after a minimum of 50 ms.
3. The Applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is turned on, the LP3970 de-asserts nBATT_FLT.
5. The Applications processor asserts SYS_EN, the LP3970 enables the system high-voltage power supplies. The Applications processor starts its countdown timer set to 125 ms.
6. The LP3970 enables the high-voltage power supplies.
7. Countdown timer expires; the Applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer set to 125 mS period.
8. The Applications processor asserts PWR_EN, the LP3970 enables the low-voltage regulators.
9. Countdown timer expires; If nVDD_FLT is de-asserted the power up sequence continues by enabling the processors 13 MHz oscillator and PLL's.
10. The Applications processor begins the execution of code.

Typical Application Circuit

CONNECTION DIAGRAM FOR PXA27X AND LP3970



Application Hints

LDO CONSIDERATIONS

External Capacitors

The LP3970's regulators requires external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitor is required for stability. It is recommended that a 1.0 µF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0 µF over the entire operating temperature range.

Output Capacitor

The LDO's are designed specifically to work with very small ceramic output capacitors. A 1.0 µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500 mΩ, are suitable in the application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

No-Load Stability

The LDO's will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

Capacitor Characteristics

The LDO's are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDO's.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, *Figure 4* shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

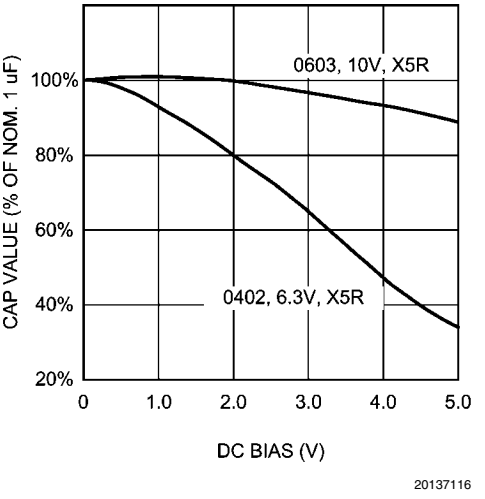


FIGURE 4. Graph Showing a Typical Variation in Capacitance vs. DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

BUCK CONSIDERATIONS

Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specs are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings at max ambient temperature of application should be requested from manufacturer.

There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{WHERE } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: Average to peak inductor current
- I_{OUTMAX}: Maximum load current (600 mA)
- V_{IN}: Maximum input voltage in application
- L: Min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f: Minimum switching frequency (1.6 MHz)
- V_{OUT}: Output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the max current limit of 1150 mA.

A 2.2 µH inductor with a saturation current rating of at least 1150 mA is recommended for most applications. The inductor's resistance should be less than 0.3Ω for good efficiency. Table 1 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 10 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{1 - \frac{V_{OUT}}{V_{IN}} * \left(\frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$

TABLE 1. Suggested Inductors and their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (Max)
DO3314-222MX	Coilcraft	3.3 x 3.3 x 1.4	200 mΩ
LPO3310-222MX	Coilcraft	3.3 x 3.3 x 1.0	150 mΩ
ELL5GM2R2N	Panasonic	5.2 x 5.2 x 1.5	53 mΩ
CDRH2D14-2R2	Sumida	3.2 x 3.2 x 1.55	94 mΩ

OUTPUT CAPACITOR SELECTION

Use a 10 µF, 6.3V ceramic capacitor. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process. The LP3970 has been evaluated with 10 µF, 6.3V, 0805 capacitor.

The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follows

$$V_{PP-C} = \frac{I_{RIPPLE}}{4 * f * C}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows

$$V_{PP-ESR} = (2 * I_{RIPPLE}) * R_{ESR}$$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared can be expressed as follows

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (RESR).

The RESR is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

TABLE 2. Suggested Capacitor and their Suppliers

Model	Type	Vendor	Voltage	Case Size Inch (mm)
22 µF for C_{OUT}				
GRM21BR60J226K	Ceramic, X5R	Murata	6.3V	0805 (2012)
C2012X5R0J226K	Ceramic, X5R	TDK	6.3V	0805 (2012)
JMK212BJ226K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
10 µF for C_{IN} or C_{OUT}				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3V	0805 (2012)

Board Layout Considerations

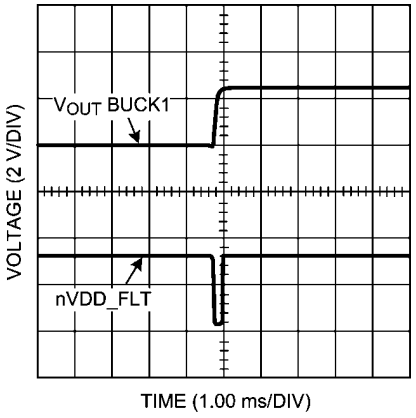
PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Good layout for the converters can be implemented by following a few simple design rules.

1. Place the converters, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the converter and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the converter by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the converter and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the converter by giving it a low-impedance ground connection.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the converter circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. Place noise sensitive circuitry, such as radio RF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

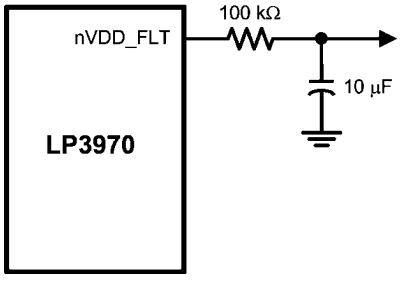
Application Note 1 nVDD FLT

When I²C commands are used to enable LDO 1 to 6 or Buck1, 2 the nVDD_FLT output momentarily glitches, see plot below.



20137140

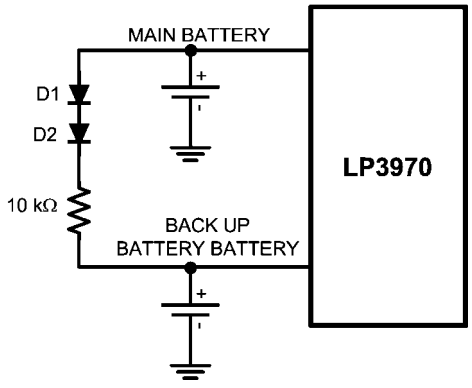
The nVDD_FLT signal can be deglitched using the following circuit. This will deglitch nVDD_FLT and allow the system designer to use I²C commands to turn the supplies on or off.



20137141

Application Note 2 Back-Up Battery Switch

When operating from a backup battery the battery selection switch may latch up if the backup battery voltage has discharged below 2.0V. The circuit shown below will prevent back up battery from latching up under these conditions. D1 and D2 are silicon SMT diodes and the 10 kΩ resistor can be adjusted for different capacity BU batteries however care should be taken not to exceed manufactures specification.

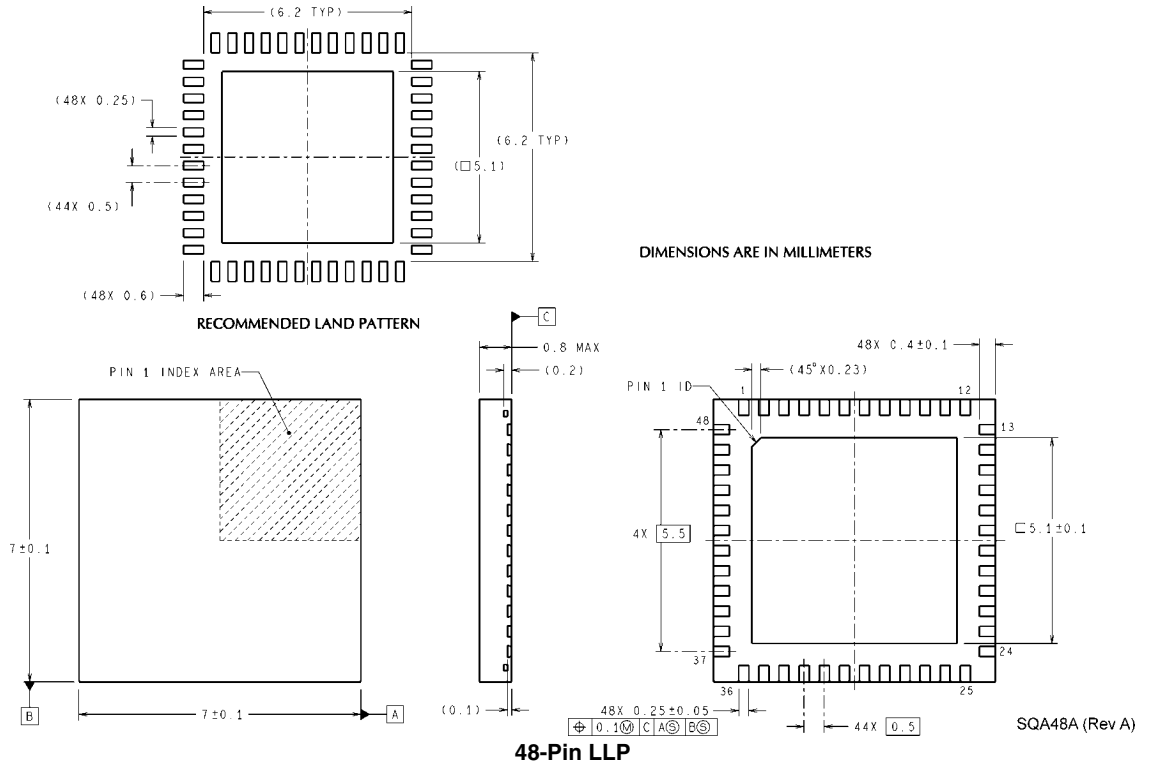


20137142

Application Note 3 V_{CC} IO

The PXA27x power requirements document states V_{CC}_IO shall be ±200 mV of V_{CC}_RTC when V_{CC}_IO is active. The current LP3970 datasheet specification has V_{CC}_RTC = 2.8V and V_{CC}_IO = to 2.8V. The LP3970 does not incorporate circuitry for the RTC_LDO to tract V_{CC}_IO. The LP3970 can accommodate V_{CC}_IO voltages of no more then 3.0V. If a higher IO voltage is required an external low dropout regulator such as the LP3871 can be used to power V_{CC}_RTC with the output voltage set to V_{CC}_IO.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Pin LLP
NS Drawing SQA48A

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560