LMH6629

LMH6629 Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown

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Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown

General Description

The LMH6629 is a high-speed, ultra low-noise amplifier designed for applications requiring wide bandwidth with high gain and low noise such as in communication, test and measurement, optical and ultrasound systems.

The LMH6629 operates on 2.7 to 5.5V supply with an input common mode range that extends below ground and outputs that swing to within 0.8V of the rails for ease of use in single supply applications. Heavy loads up to ±250 mA can be driven by high-frequency large signals with the LMH6629's –3dB bandwidth of 900 MHz and 1600 V/μs slew rate. The LMH6629 (LLP-8 package only) has user-selectable internal compensation for minimum gains of 4 or 10 controlled by pulling the COMP pin low or high, thereby avoiding the need for external compensation capacitors required in competitive devices. Compensation for the SOT23-5 package is internally set for a minimum stable gain of 10 V/V. The LLP-8 package also provides the power-down enable/ disable feature.

The low-input noise (0.69nV/√Hz and 2.6 pA/√Hz), low distortion (HD2/ HD3 = –90 dBc/–94 dBc) and ultra-low DC errors (800 μV V_{OS} maximum over temperature, ±0.45 μV/°C drift) allow precision operation in both AC- and DC-coupled applications.

The LMH6629 is fabricated in National Semiconductor's proprietary SiGe process and is available in a 3mm x 3mm 8-pin LLP, as well as the SOT23-5, package.

Features

Specified for V_S = 5V, R_L = 100Ω, A_V = 10V/V LLP-8 package, unless specified

–3dB bandwidth	900 MHz
Input voltage noise	0.69 nV/√Hz
Input offset voltage max. over temperature	±0.8 mV
Slew rate	1600 V/ μs
HD2 @ f = 1MHz, $2V_{PP}$	–90 dBc
HD3 @ f = 1MHz, $2V_{PP}$	–94 dBc
Supply voltage range	2.7V to 5.5V
Typical supply current	15.5 mA
Selectable min. gain	≥4 or ≥10 V/V
Enable Time	75 ns
Output Current	±250 mA
LLP-8 and SOT23-5 Packages	

Applications

- Instrumentation Amplifiers
- Ultrasound Pre-amps
- Wide-band Active Filters
- Opto-electronics
- Medical imaging systems
- Base-station Amplifiers
- Low-Noise Single Ended to Differential Conversion
- Trans-impedance amplifier

Typical Application Circuit

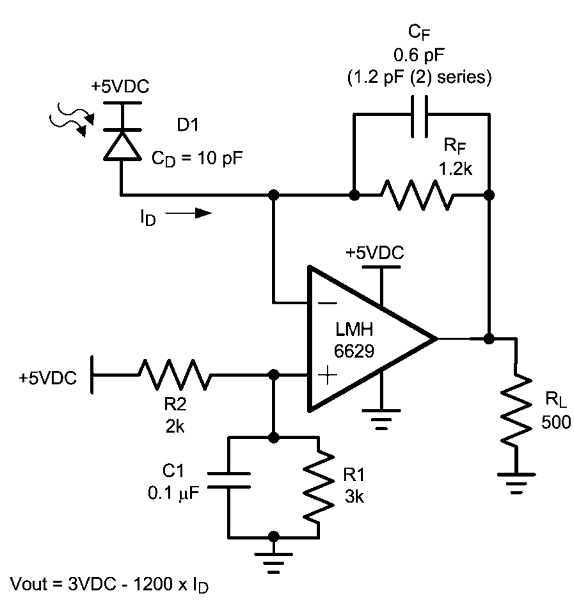
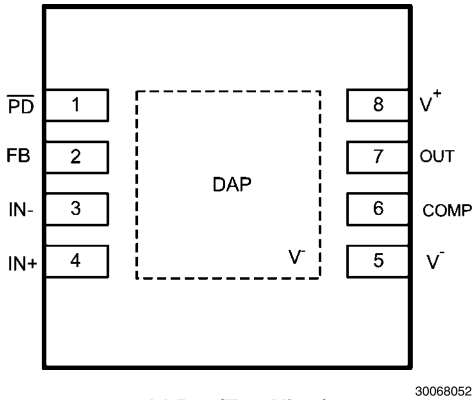


FIGURE 1. Transimpedance Amplifier

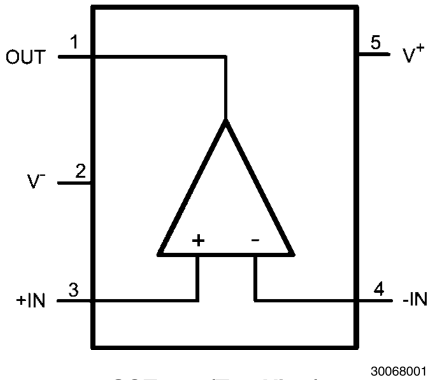
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
LLP-8	LMH6629SD	L6629	1k Units Tape and Reel	SDA08A
	LMH6629SDE		250 Units Tape and Reel	
	LMH6629SDX		4.5k Units Tape and Reel	
SOT23-5	LMH6629MF	AE7A	1k Units Tape and Reel	MF05A
	LMH6629MFE		250 Units Tape and Reel	
	LM6629MFX		3k Units Tape and Reel	

Connection Diagrams



LLP-8 (Top View)



SOT23-5 (Top View)

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 4)	
Human Body Model	2kV
Machine Model	200V
Charge-Device Model	750V
Positive Supply Voltage	−0.5 to 6.0V
Differential Input Voltage	3V
Analog Input Voltage Range	−0.5 to V_S
Digital Input Voltage	−0.5 to V_S
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	

See Product Folder at www.national.com and http://www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (Note 1)

Supply Voltage (V^+ - V^-)	2.7V to 5.5V
Operating Temperature Range	−40°C to +125°C
Package	(θ_{JA})
LLP-8	71°C/W
SOT23-5	179°C/W

5V Electrical Characteristics

The following specifications apply for single supply with V_S = 5V, R_L = 100Ω terminated to 2.5V, gain = 10V/V, V_O = 2V_{PP}, V_{CM} = V_S/2, COMP Pin = HI (LLP-8 package), unless otherwise noted. **Boldface** limits apply at the temperature extremes. (Note 2).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
DYNAMIC PERFORMANCE						
SSBW	Small signal −3dB bandwidth	V_O = 200 mV_{PP}, LLP-8 package		900		MHz
		V_O = 200 mV_{PP}, SOT23-5 package		1000		
		A_V= 4, V_O = 200 mV_{PP}, COMP Pin = LO		800		
LSBW	Large signal −3dB bandwidth	V_O = 2V_{PP}		380		MHz
		COMP Pin = LO, A_V= 4, V_O = 2V_{PP}		190		
	0.1 dB bandwidth	A_V= 10, V_O = 200 mV_{PP}, LLP-8 package		330		MHz
		A_V= 10, V_O = 200 mV_{PP}, SOT23-5 package		190		
		A_V= 4, V_O = 200 mV_{PP}, COMP Pin = LO		95		
	Peaking	V_O = 200 mV_{PP}, LLP-8 package		0		dB
		V_O = 200 mV_{PP}, SOT23-5 package		2		
SR	Slew rate	A_V= 10, 2V step		1600		V/µs
		A_V= 4, 2V step, COMP Pin = LO		530		
t_r/ t_f	Rise/fall time	A_V= 10, 2V step, 10% to 90%, LLP-8 package		0.90		ns
		A_V= 10, 2V step, 10% to 90%, SOT23-5 package		0.95		
		A_V= 4, 2V step, 10% to 90%, COMP Pin = LO, (Slew Rate Limited)		2.8		
T_s	Settling time	A_V= 10, 1V step, ±0.1%		42		
	Overload Recovery	V_{IN} = 1V_{PP}		2		

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
NOISE AND DISTORTION						
HD2	2^{nd} order distortion	fc = 1MHz, V_O = $2V_{PP}$		−90		dBc
		COMP Pin = LO, A_V= 4, fc = 1 MHz, V_O = $2V_{PP}$		−88		
		fc = 10 MHz, V_O = $2V_{PP}$		−70		
		COMP Pin = LO, fc = 10 MHz, A_V= 4V, V_O = $2V_{PP}$		−65		
HD3	3^{rd} order distortion	fc = 1MHz, V_O = $2V_{PP}$		−94		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = $2V_{PP}$		−87		
		fc = 10 MHz, V_O = $2V_{PP}$		−82		
		COMP Pin = LO, fc = 10 MHz, V_O = $2V_{PP}$		−75		
OIP3	Two-tone 3^{rd} order intercept point	fc = 25 MHz, V_O = 2 V_{PP} composite		31		dBm
		fc = 75 MHz, V_O = $2V_{PP}$ composite		27		
e_n	Noise Voltage	Input referred f > 1MHz		0.69		nV/√Hz
i_n	Noise current			2.6		pA/√Hz
NF	Noise Figure	R_S = R_T = 50Ω		8.0		dB
ANALOG I/O						
CMVR	Input voltage range	CMRR > 70 dB, LLP-8 package	−0.30		3.8	V
		CMRR > 70 dB, SOT23-5 package		−0.30 to 3.8		
V_O	Output voltage range	R_L = 100Ω to V_S/2	0.89 **0.95**	0.82 to 4.19	4.0 **3.9**	V
		No Load	0.76 **0.85**	0.72 to 4.28	4.1 **4.0**	
I_{OUT}	Linear output current	V_O = 2.5V (Note 3)		250		mA
V_{OS}	Input offset voltage			±150	±780 **±800**	μV
TcV_{OS}	Input offset voltage temperature drift	(Note 7)		±0.45		μV/°C
I_{BI}	Input bias current	(Note 6)		−15	−23 **−37**	μA
I_{OS}	Input offset current			±0.1	±1.8 **±3.0**	μA
T_CI_{OS}	Input offset voltage temperature drift	(Note 7)		±2.8		nA/°C
C_{CM}	Input capacitance	Common Mode		1.7		pF
R_{CM}	Input resistance	Common Mode		450		kΩ
MISCELLANEOUS PARAMETERS						
CMRR	Common mode rejection ratio	V_{CM} from 0V to 3.7V, LLP-8 package	82 **70**	87		dB
		V_{CM} from 0V to 3.7V, SOT23-5 package		87		
PSRR	Power supply rejection ratio		81 **78**	83		
A_{VOL}	Open loop gain	LLP-8 package	74 **72**	78		
		SOT23-5 package		78		

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
DIGITAL INPUTS/TIMING						
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins, , LLP-8 package			0.8	V
V_{IH}	Logic high-voltage threshold	$\overline{PD}$ and COMP pins, LLP-8 package	2.5			V
I_{IL}	Logic low-bias current	$\overline{PD}$ and COMP pins = 0.8V, , LLP-8 package(Note 6)	−23 **−19**	−28	−34 **−38**	μA
I_{IH}	Logic high-bias current	$\overline{PD}$ and COMP pins = 2.5V, LLP-8 package(Note 6)	−16 **−14**	−22	−27 **−29**	μA
T_{en}	Enable time	LLP-8 package		75		ns
T_{dis}	Disable time	LLP-8 package		80		ns
POWER REQUIREMENTS						
I_S	Supply Current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open for LLP-8 package)		15.5	16.7 **18.2**	mA
I_S	Supply Current	No Load, Shutdown ($\overline{PD}$ Pin =LO for LLP-8 package)		1.1	1.85 **2.0**	mA

3.3V Electrical Characteristics

The following specifications apply for single supply with V_S = 3.3V, R_L = 100Ω terminated to 1.65V, gain = 10V/V, V_O = 1V_{PP}, V_{CM} = V_S/2, COMP Pin = HI (LLP-8 package), unless otherwise noted. **Boldface** limits apply at the temperature extremes. (Note 2)

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 5)	Max (Note 5)	Units
DYNAMIC PERFORMANCE						
SSBW	Small signal –3dB bandwidth	V_O = 200 mV_{PP}, LLP-8 package		820		MHz
		V_O = 200 mV_{PP}, SOT23-5 package		950		
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		730		
LSBW	Large signal –3dB bandwidth	V_O = 1V_{PP}		540		MHz
		COMP Pin = LO, A_V= 4, V_O = 1V_{PP}		320		
	0.1 dB bandwidth	A_V= 10, V_O = 200 mV_{PP}, LLP-8 package		330		MHz
		A_V= 10, V_O = 200 mV_{PP}, SOT23-5 package		190		
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		85		
	Peaking	V_O = 200 mV_{PP}, LLP-8 package		0		dB
		V_O = 200 mV_{PP}, SOT23-5 package		1.8		
SR	Slew rate	A_V= 10, 1.3V step		1100		V/µs
		COMP Pin = LO, A_V= 4, 1.3V step		500		
t_r/ t_f	Rise/fall time	A_V= 10, 1V step, 10% to 90%, LLP-8 package		0.7		ns
		A_V= 10, 1V step, 10% to 90%, SOT23-5 package		0.55		
		A_V= 4, COMP Pin = LO, 1V step, 10% to 90% (Slew Rate Limited)		1.3		
T_s	Settling time	A_V= 10, 1V step, ±0.1%		70		
	Overload Recovery	V_{IN} = 1V_{PP}		2		
NOISE AND DISTORTION						
HD2	2nd order distortion	fc = 1MHz, V_O = 1V_{PP}		–82		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = 1V_{PP}		-88		
		fc = 10 MHz, V_O = 1V_{PP}		-67		
		COMP Pin = LO, fc = 10 MHz, A_V= 4V, V_O = 1V_{PP}		-74		
HD3	3rd order distortion	fc = 1MHz, V_O = 1V_{PP}		-94		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = 1V_{PP}		-112		
		fc = 10 MHz, V_O = 1V_{PP}		-79		
		COMP pin = LO, fc = 10 MHz, V_O = 1V_{PP}		–96		
OIP3	Two-tone 3rd Order Intercept Point	fc = 25 MHz, V_O = 1V_{PP} composite		30		dBm
		fc = 75 MHz, V_O = 1V_{PP} composite		26		
e_n	Noise voltage	Input referred, f > 1MHz		0.69		nV/√HZ
i_n	Noise current			2.6		pA/√HZ
NF	Noise figure	R_S = R_T = 50Ω		8.0		dB

Symbol	Parameter	Conditions	Min (*Note 5*)	Typ (*Note 5*)	Max (*Note 5*)	Units
ANALOG I/O						
CMVR	Input voltage range	CMRR > 70 dB, LLP-8 package	−0.30		2.1	V
		CMRR > 70 dB, SOT23-5 package		−0.30 to 2.1		
V_O	Output voltage range	R_L = 100Ω to $V_S/2$	0.90 **0.95**	0.79 to 2.50	2.4 **2.3**	V
		No load	0.76 **0.80**	0.70 to 2.60	2.5 **2.4**	
I_{OUT}	Linear output current	V_O = 1.65V (*Note 3*)		230		mA
V_{OS}	Input Offset Voltage			±150	±680 **±700**	μV
TcV_{OS}	Input offset voltage temperature drift	(*Note 7*)		±1		μV/°C
I_{BI}	Input Bias Current	(*Note 6*)		−15	−23 **−35**	μA
I_{OS}	Input Offset Current			±0.13	±1.8 **±3.0**	μA
T_CI_{OS}	Input offset voltage temperature drift	(*Note 7*)		±3.2		nA/°C
C_{CM}	Input Capacitance	Common Mode		1.7		pF
R_{CM}	Input Resistance	Common Mode		1		MΩ
MISCELLANEOUS PARAMETERS						
CMRR	Common Mode Rejection Ratio	V_{CM} from 0V to 2.0V, LLP-8 package	84 **81**	87		dB
		V_{CM} from 0V to 2.0V, SOT23-5 package		87		
PSRR	Power supply rejection ratio		82 **79**	84		
A_{VOL}	Open Loop Gain	LLP-8 package	78 **73**	79		
		SOT23-5 package		79		
DIGITAL INPUTS/TIMING						
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins, LLP-8 package			0.8	V
V_{IH}	Logic high-voltage threshold		2.0			
I_{IL}	Logic low-bias current	$\overline{PD}$ and COMP pins = 0.8V, LLP-8 package (*Note 6*)	-17 **−14**	−23	−28 **−32**	μA
I_{IH}	Logic high-bias current	$\overline{PD}$ and COMP pins = 2.0V, LLP-8 package (*Note 6*)	−16 **−13**	−22	−27 **−31**	
T_{en}	Enable time	LLP-8 package		75		ns
T_{dis}	Disable time	LLP-8 package		80		
POWER REQUIREMENTS						
I_S	Supply Current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open for LLP-8 package)		13.7	14.9 **16.0**	mA
		No Load, Shutdown ($\overline{PD}$ Pin = LO for LLP-8 package)		0.89	1.4 **1.5**	

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

Note 4: Human Body Model, applicable std. JESD22-A114C. Machine Model, applicable std. JESD22-A115-A. Field Induced Charge Device Model, applicable std. JESD22-C101-C.

Note 5: Typical numbers are the most likely parametric norm. Bold numbers refer to over-temperature limits.

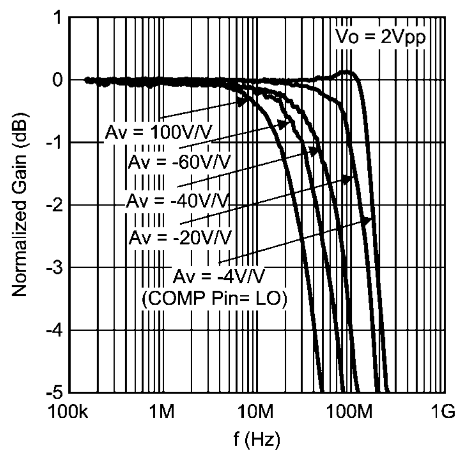
Note 6: Negative input current implies current flowing out of the device.

Note 7: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Typical Performance Characteristics

Unless otherwise specified, $V_S = \pm2.5V$, $R_f = 240\Omega$, $R_L = 100\Omega$, $V_O = 2V_{PP}$, COMP pin = HI, $A_V = +10$ V/V, LLP-8 and SOT23-5 packages (unless specifically noted).

Inverting Frequency Response



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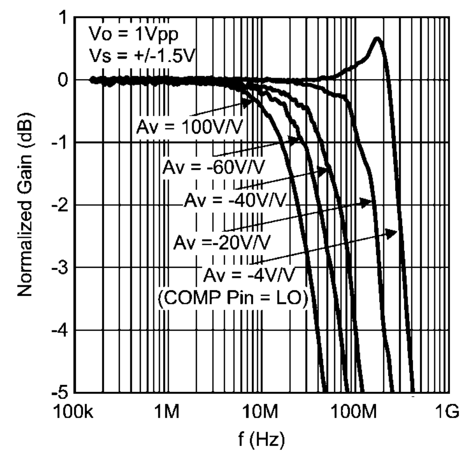
Inverting Frequency Response



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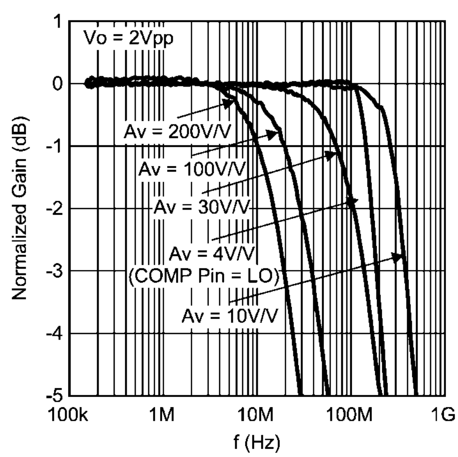
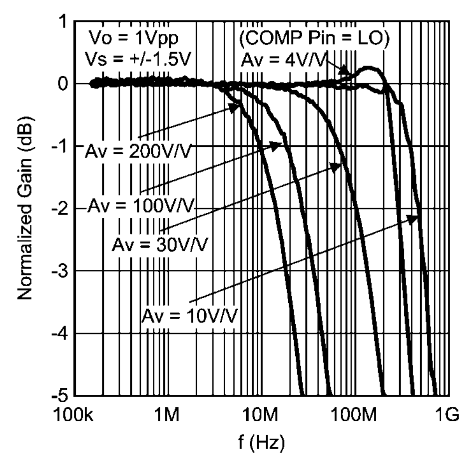
Non-Inverting Frequency Response



30068005

Non-Inverting Frequency Response



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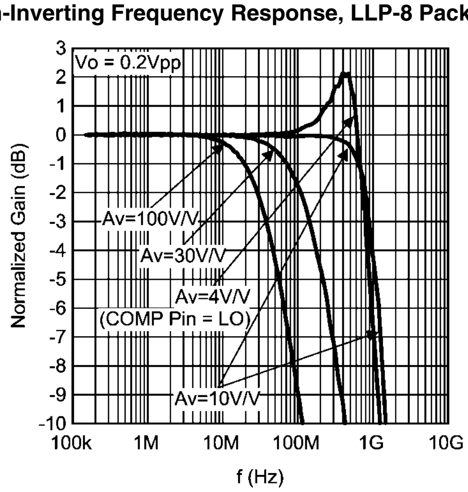
Non-Inverting Frequency Response, LLP-8 Package



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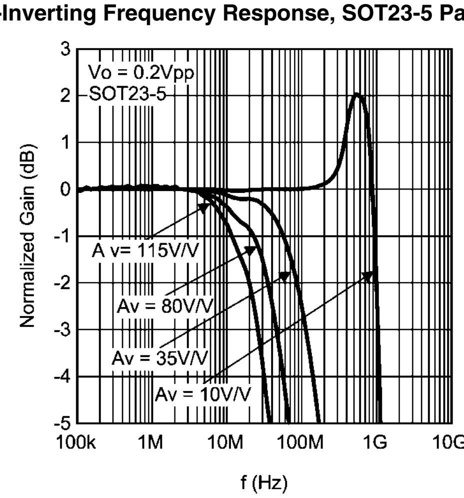
Non-Inverting Frequency Response, SOT23-5 Package



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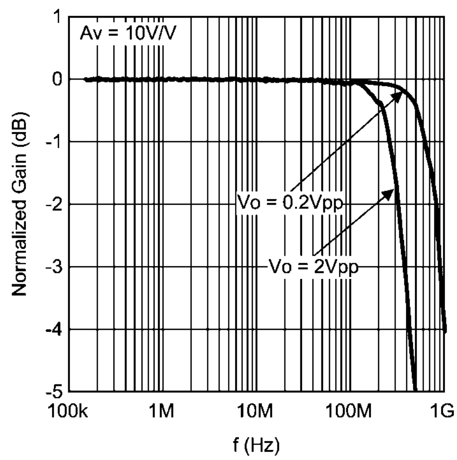
Non-Inverting Frequency Response with Varying V_O, LLP-8 Package



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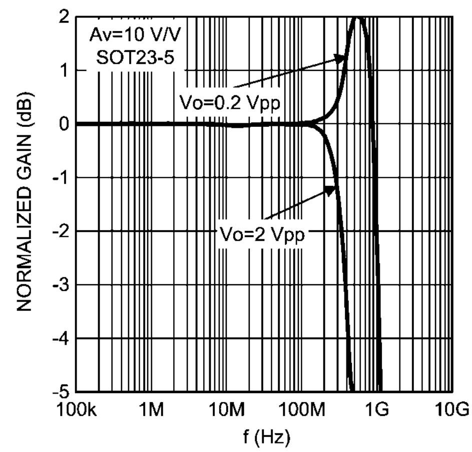
Non-Inverting Frequency Response with Varying V_O, SOT23-5 Package



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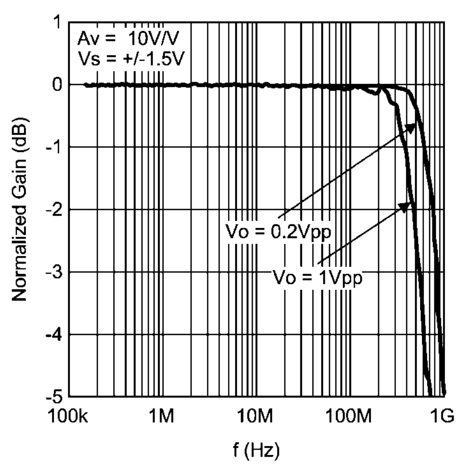
Non-Inverting Frequency Response with Varying V_O, LLP-8 Package



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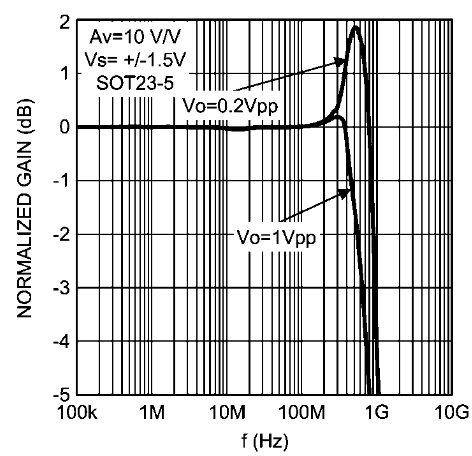
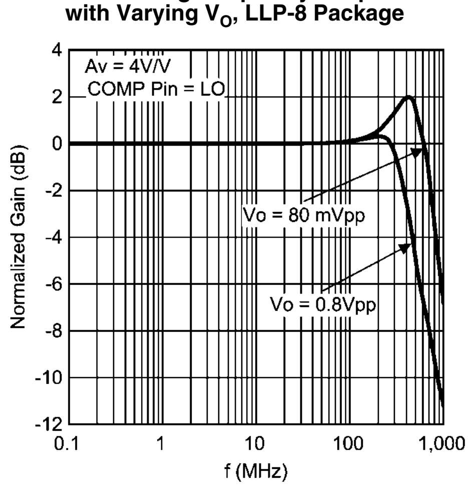
Non-Inverting Frequency Response with Varying V_O, SOT23-5 Package



30068027

Non-Inverting Frequency Response with Varying V_O, LLP-8 Package



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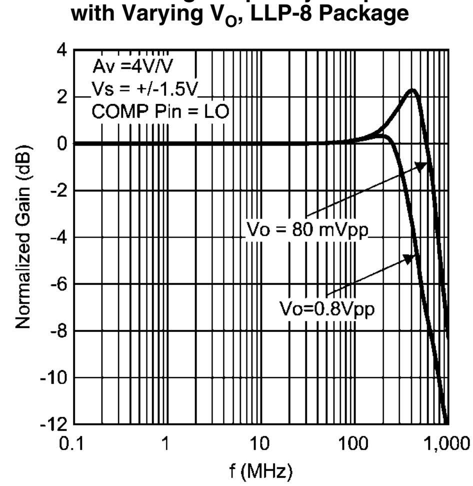
Non-Inverting Frequency Response with Varying V_O, LLP-8 Package



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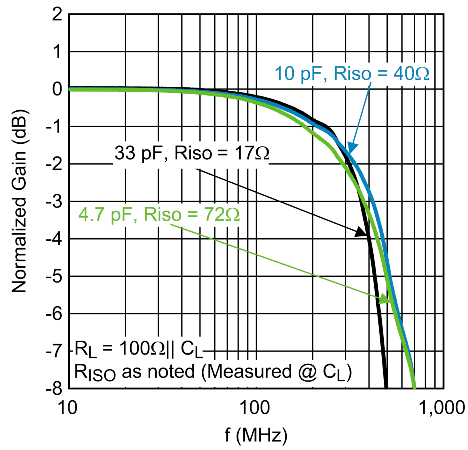
Frequency Response with Cap. Loading



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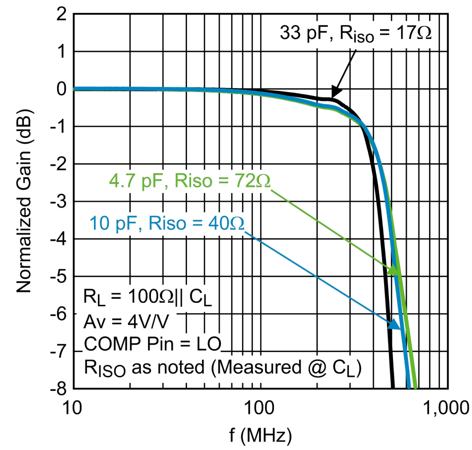
Frequency Response Cap. Loading, LLP-8 Package



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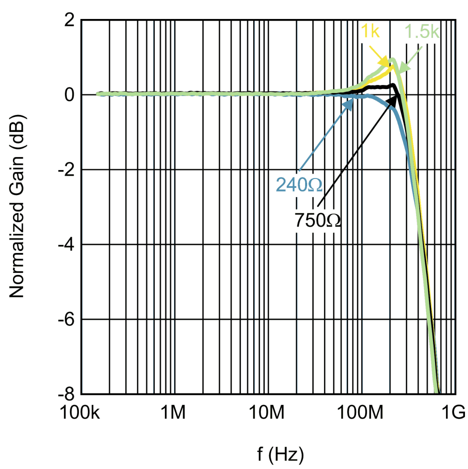
Frequency Response vs. R_f, LLP-8 Package



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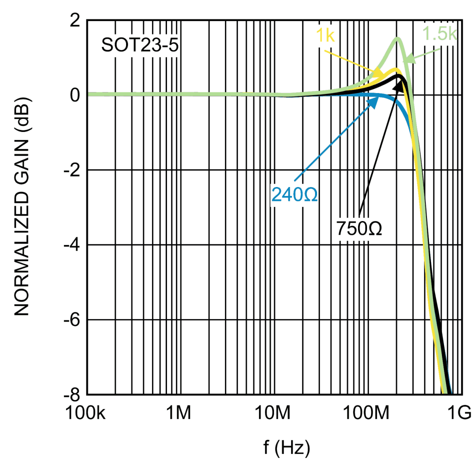
Frequency Response vs. R_f, SOT23-5 Package



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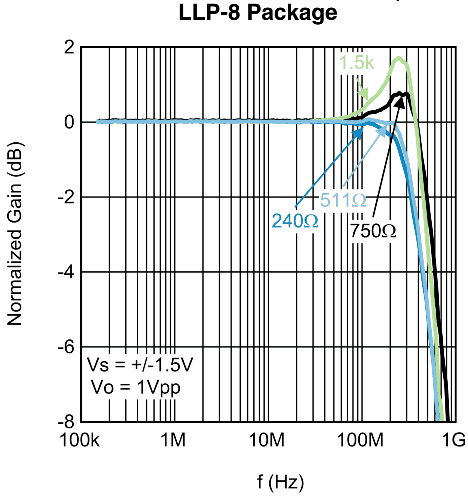
Frequency Response vs. R_f, LLP-8 Package



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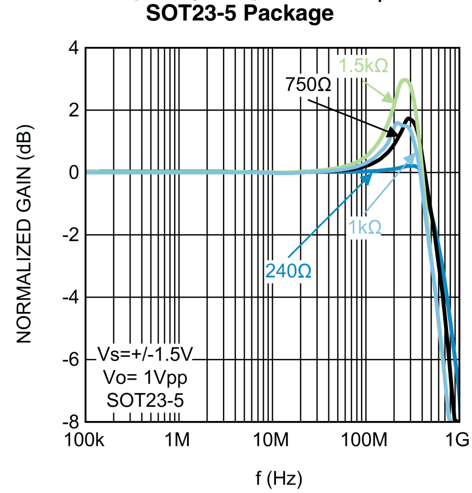
Frequency Response vs. R_f, SOT23-5 Package



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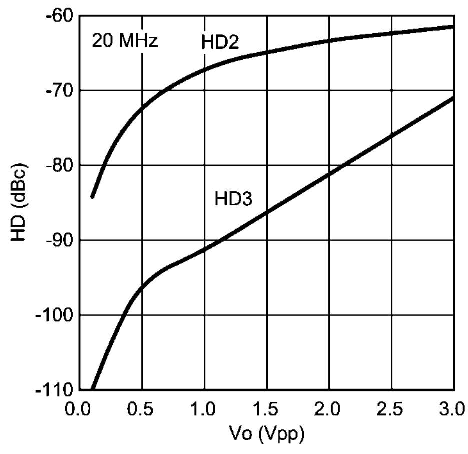
Distortion vs. Swing, LLP-8 Package



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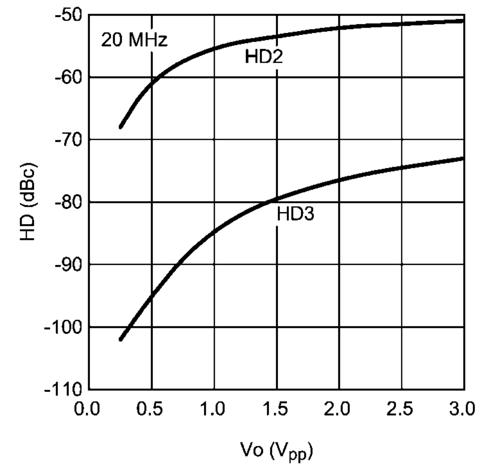
Distortion vs. Swing, SOT23-5 Package



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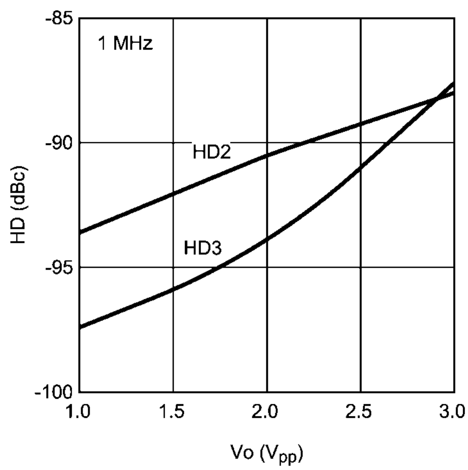
Distortion vs. Swing, LLP-8 Package



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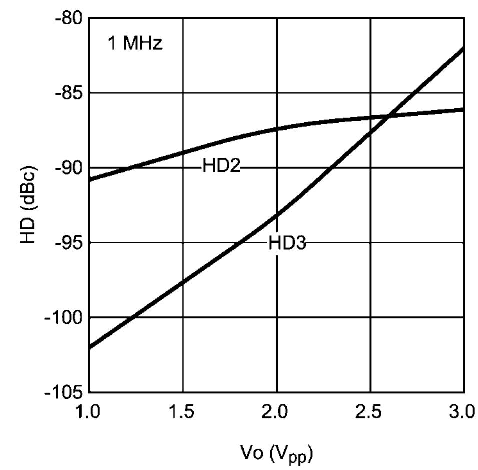
Distortion vs. Swing, SOT23-5 Package



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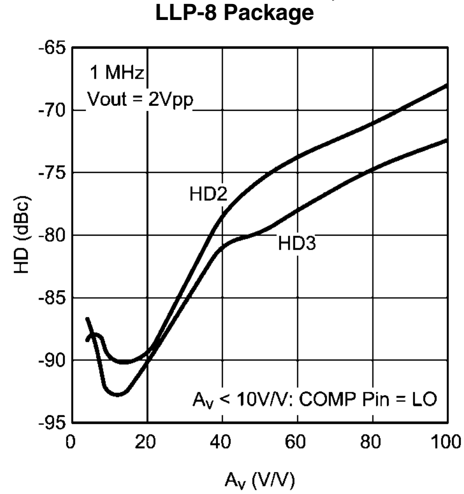
Distortion vs. Gain, LLP-8 Package



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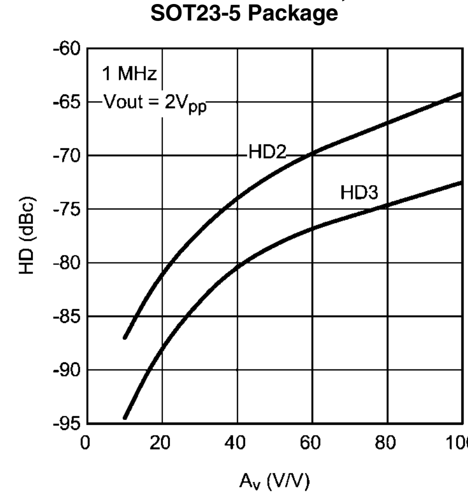
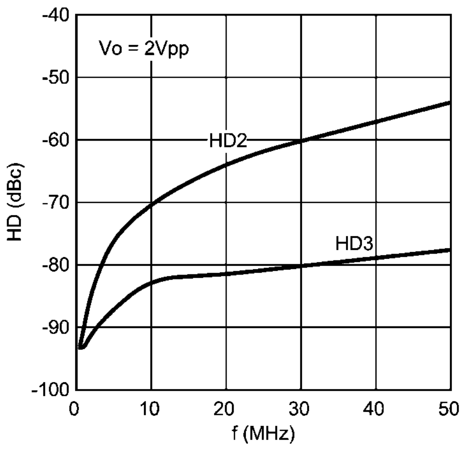
Distortion vs. Gain, SOT23-5 Package



30068048

Distortion vs. Frequency, LLP-8 Package



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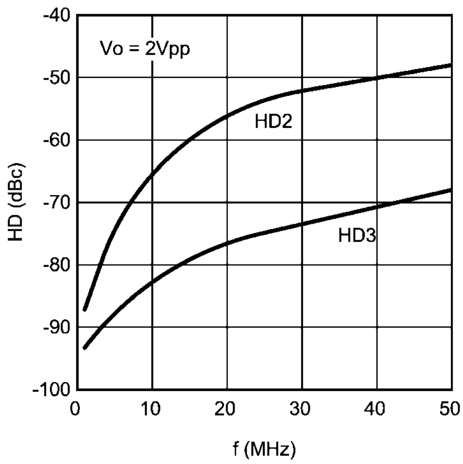
Distortion vs. Frequency, SOT23-5 Package



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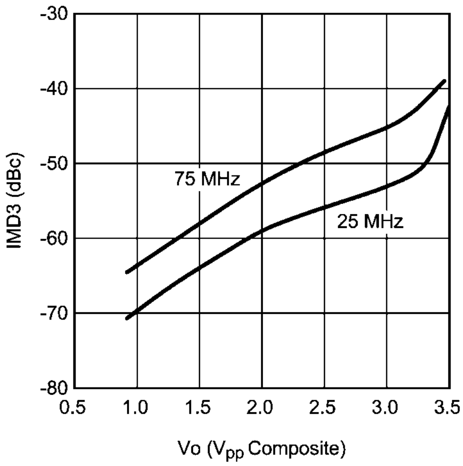
3rd Order Intermodulation Distortion vs. Output Voltage



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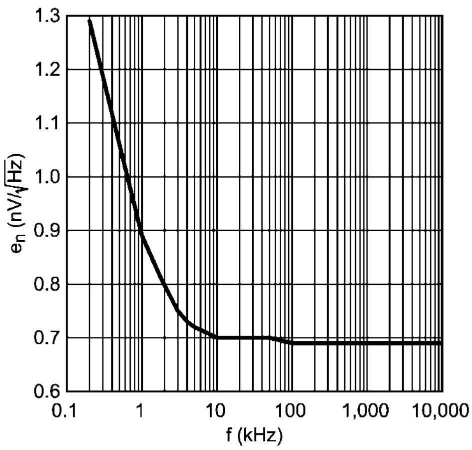
Input Noise Voltage vs. Frequency



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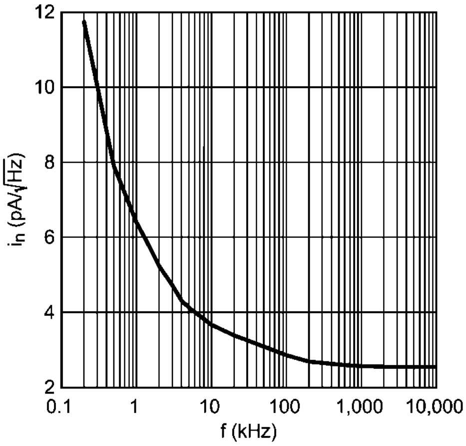
Input Noise Current vs. Frequency



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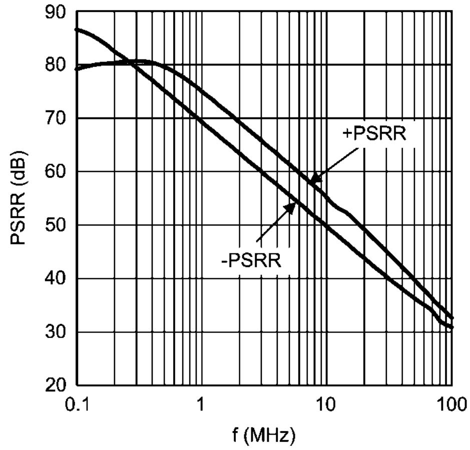
PSRR vs. Frequency



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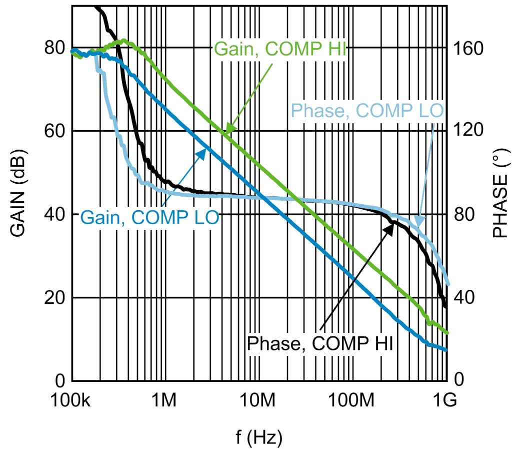
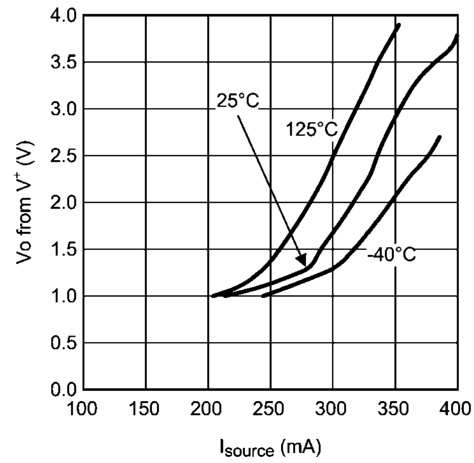
Open Loop Gain/Phase Response



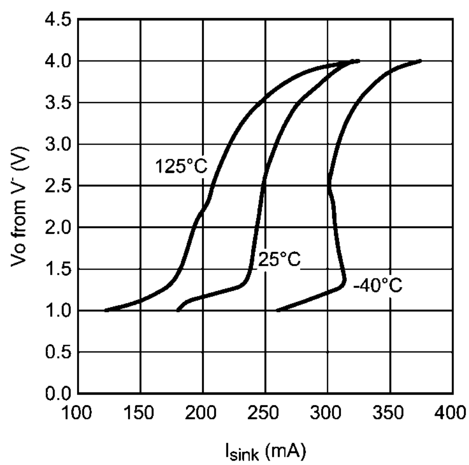
30068060

Output Source Current, LLP-8 Package



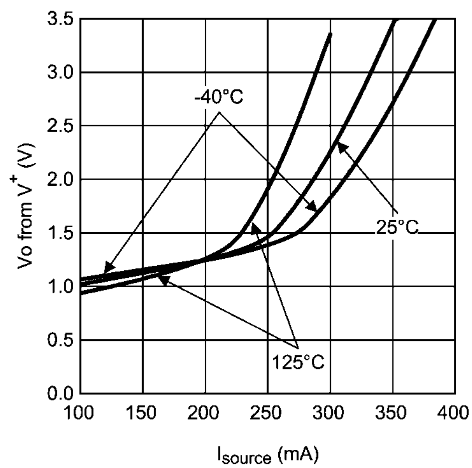
30068057

Output Sink Current LLP-8 Package



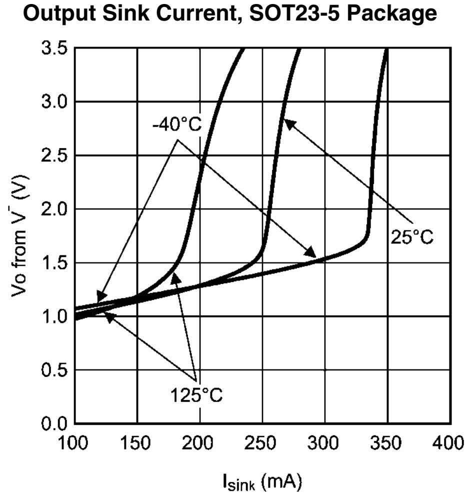
30068058

Output Source Current, SOT23-5 Package



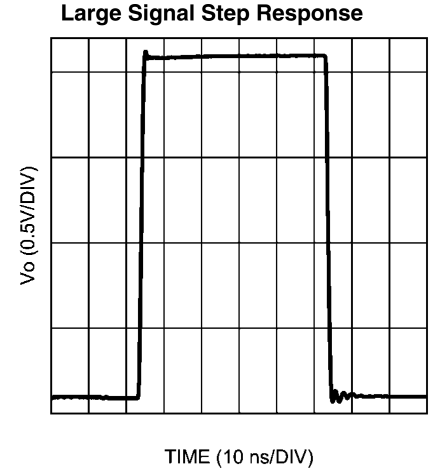
30068065

Output Sink Current, SOT23-5 Package



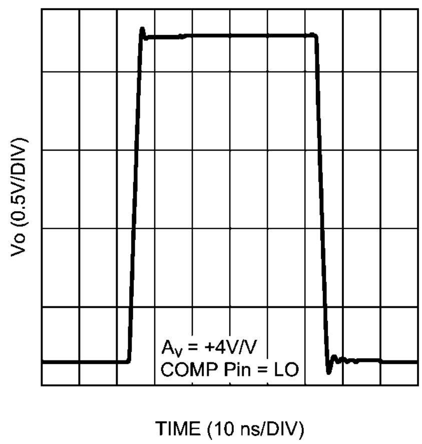
30068066

Large Signal Step Response



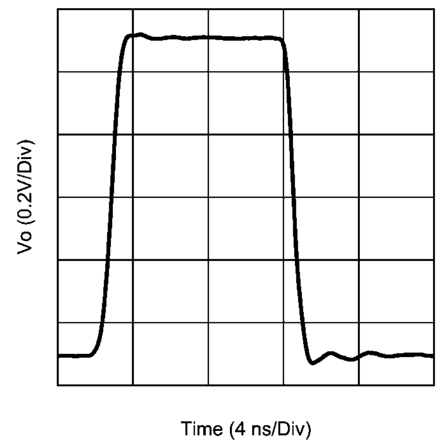
30068073

Large Signal Step Response



30068074

Large Signal Step Response



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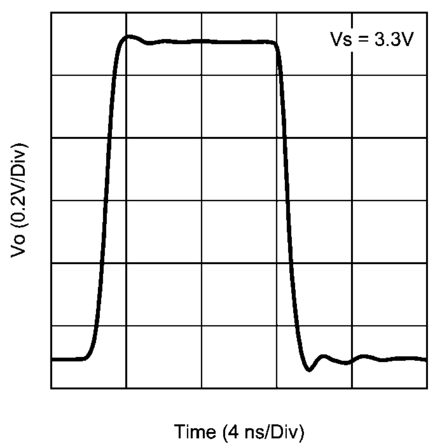
Large Signal Step Response



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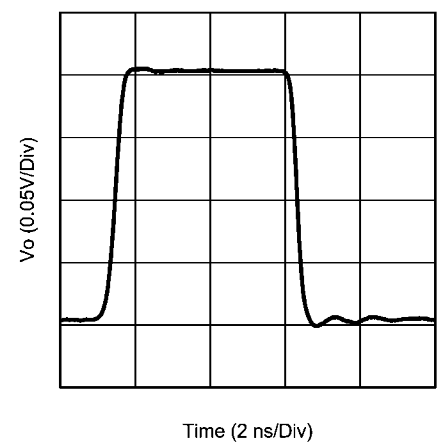
Small Signal Step Response, LLP-8 Package



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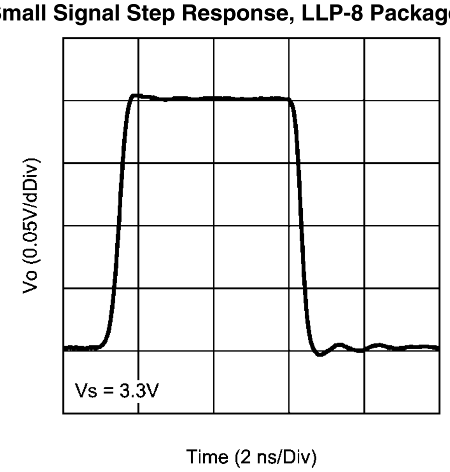
Small Signal Step Response, LLP-8 Package



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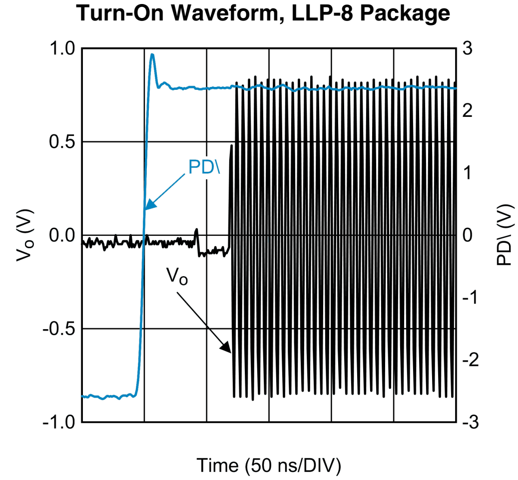
Turn-On Waveform, LLP-8 Package



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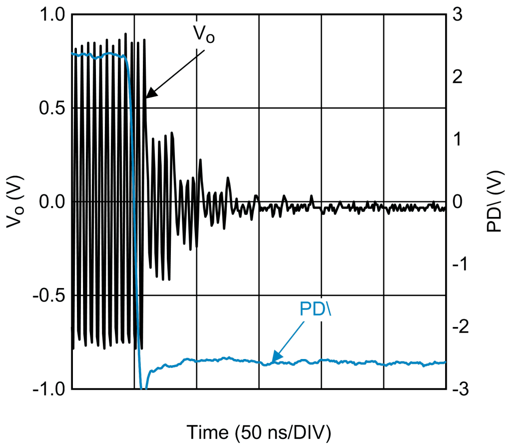
Turn-Off Waveform, LLP-8 Package



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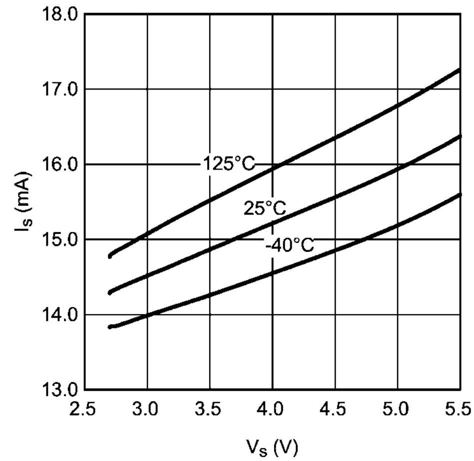
Supply Current vs. Supply Voltage



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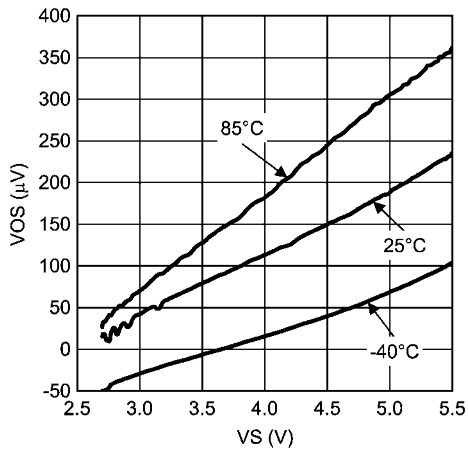
Offset Voltage vs. Supply Voltage (Typical Unit)



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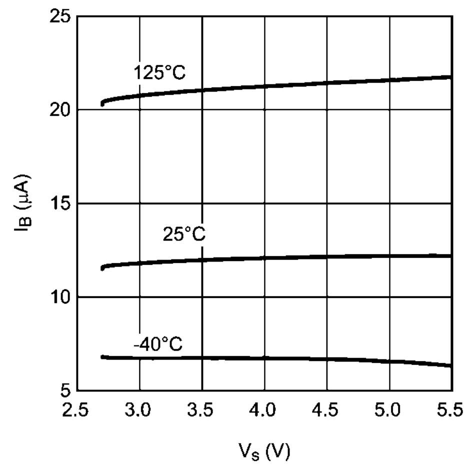
Input Bias Current vs. Supply Voltage (Typical Unit)



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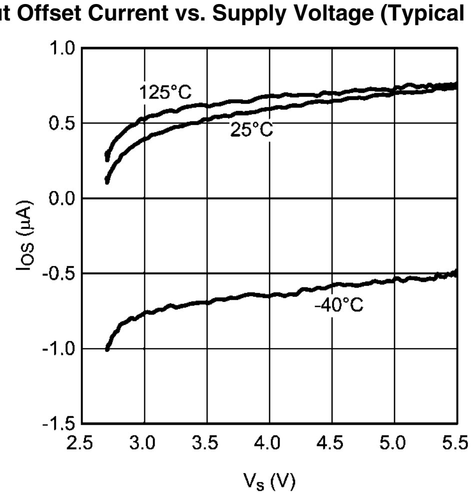
Input Offset Current vs. Supply Voltage (Typical Unit)



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Application Section

INTRODUCTION

The LMH6629 is a high gain bandwidth, ultra low-noise voltage feedback operational amplifier. The excellent noise and bandwidth enables applications such as medical diagnostic ultrasound, magnetic tape & disk storage and fiberoptics to achieve maximum high frequency signal-to-noise ratios. The following discussion will enable the proper selection of external components to achieve optimum system performance.

The LMH6629 (LLP-8 package only) has some additional features to allow maximum flexibility. As shown in *Figure 2* there are provisions for low-power shutdown and two internal compensation settings, which are further discussed below under the *COMPENSATION* heading. Also provided is a feedback (FB) pin which allows the placement of the feedback resistor directly adjacent to the inverting input (IN-) pin. This pin simplifies printed circuit board layout and minimizes the possibility of unwanted interaction between the feedback path and other circuit elements.

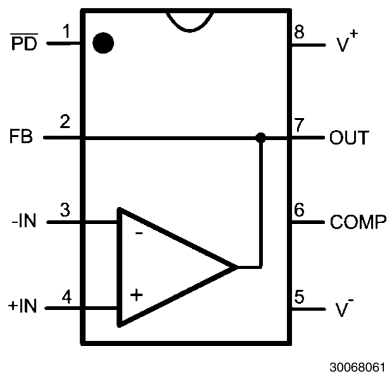


FIGURE 2. 8-Pin LLP Pinout Diagram

The LLP-8 package requires the bottom-side Die Attach Paddle (DAP) to be soldered to the circuit board for proper thermal dissipation and to get the thermal resistance number specified. The DAP is tied to the V^- potential within the LMH6629 package. Thus, the circuit board copper area devoted to DAP heatsinking connection should be at the V- potential as well. Please refer to the package drawing for the recommended land pattern and recommended DAP connection dimensions.

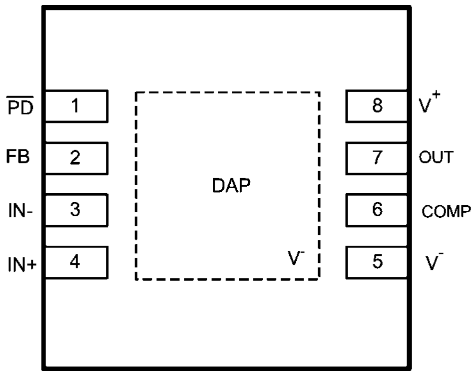


FIGURE 3. LLP–8 DAP(Top View)

LLP-8 CONTROL PINS & SOT23-5 COMPARISON

The LMH6629 LLP-8 package has two digital control pins; $\overline{PD}$ and COMP pins. The $\overline{PD}$ pin, used for powerdown, floats high (device on) when not driven. When the $\overline{PD}$ pin is pulled low, the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. The other control pin, the COMP pin, allows control of the internal compensation and defaults to the lower gain mode or logic 0.

The SOT23-5 package has the following differences relative to the LLP-8 package:

1. No power down (shutdown) capability.
2. No COMP pin to set the minimum stable gain. SOT23–5 package minimum stable gain is internally fixed to be 10V/V.
3. No feedback (FB) pin.

From a performance point of view, the LLP-8 and the SOT23-5 packages perform very similarly except in the following areas:

1. **SSBW, Peaking, and 0.1 dB Bandwidth:** These differences are highlighted in the *Typical Performance Characteristics* section and the Electrical Characteristics tables. Most notable differences are with small signal (0.2 Vpp) and close to the minimum stable gain of 10V/V.
2. **Distortion:** It is possible to get slightly different distortion performance. The board layout, decoupling capacitor return current routing strongly influences this
3. **Output Current:** In heavy current applications, there will be differences between these package types because of the difference in their respective Thermal Resistances (θ_{JA}).

COMPENSATION

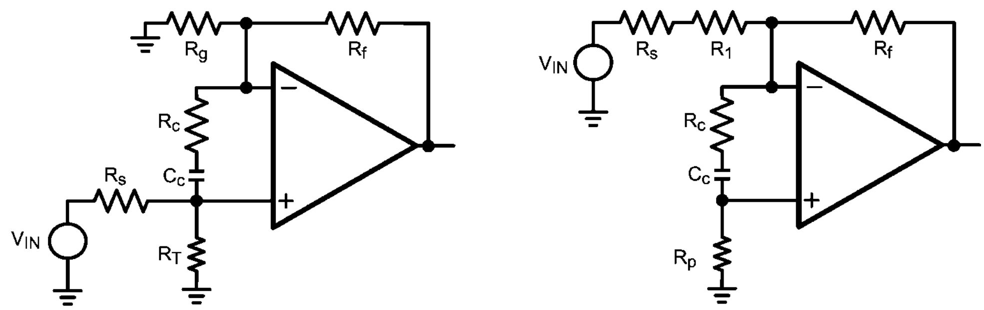
The LMH6629 has two compensation settings that can be controlled by the COMP pin (LLP-8 package only). The default setting is set through an internal pull down resistor and places the COMP pin at the logic 0 state. In this configuration the on-chip compensation is set to the maximum and bandwidth is reduced to enable stability at gains as low as 4V/V.

When this pin is driven to the logic 1 state, the internal compensation is decreased to allow higher bandwidth at higher gains. In this state, the minimum stable gain is 10V/V. Due to the reduced compensation, slew rate and large signal bandwidth are significantly enhanced for the higher gains.

As mentioned earlier, the SOT23-5 package does not offer the two compensation settings that the LLP-8 offers. The SOT23-5 is internally set for a minimum gain of 10 V/V.

It is possible to externally compensate the LMH6629 for any of the following reasons, as shown in *Figure 4*:

- To operate the SOT23-5 package (which does not offer the COMP pin) at closed loop gains < 10V/V.
- To operate the LLP-8 package at gains below the minimum stable gain of 4V /V when the COMP pin is LO. **Note:** In this case, *Figure 4* "Constraint 1" may be changed to ≥ 4 V/V instead of ≥ 10 V/V.
- To operate either package at low gain and need maximum slew rate (COMP pin HI).



a) Non-inverting

$R_p = R_s || R_T$

COMP pin = HI

$R_{EQ} = R_f || R_g$

b) Inverting

$R_g = R_s + R_1$

$$\text{Constraint 1:} \quad (1+\frac{R_f}{R_g})(1+\frac{R_p+R_{EQ}}{R_c}) \geq 10\text{V/V}$$

$$\text{Costraint 2:} \quad \frac{1}{2\pi C_c R_c} \leq 90\text{ MHz}$$

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FIGURE 4. External Compensation

This circuit operates by increasing the Noise Gain (NG) beyond the minimum stable gain of the LMH6629 while maintaining a positive loop gain phase angle at 0dB. There are two constraints shown in *Figure 4*; "Constraint 1" ensures that NG has increased to at least 10 V/V when the loop gain approaches 0dB, and "Constraint 2" places an upper limit on the feedback phase lead network frequency to make sure it is fully effective in the frequency range when loop gain approaches 0dB. These two constraints allow one to estimate the "starting value" for R_c and C_c which may need to be fine tuned for proper response.

Here is an example worked out for more clarification:

Assume that the objective is to use the SOT23-5 version of the LMH6629 for a closed loop gain of +3.7 V/V using the technique shown in *Figure 4*.

Selecting R_f = 249Ω → R_g = 91Ω → R_{EQ}= 66.6Ω.

For 50Ω source termination (R_s= 50Ω), select R_T= 50Ω → R_p = 25Ω.

Using "Constraint 1" (= 10V/V) allows one to compute Rc ≅ 56Ω. Using "Constraint 2" (= 90 MHz) defines the appropriate value of C_c≅ 33 pF.

The frequency response plot shown in *Figure 5* is the measured response with R_c and C_c values computed above and shows a -3dB response of about 1GHz.

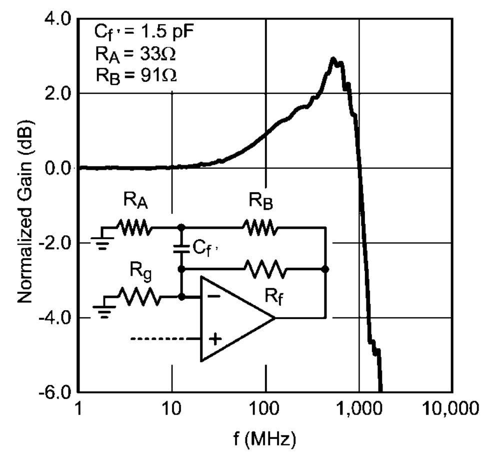

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FIGURE 5. SOT23-5 Package Low Closed Loop Gain Operation with External Compensation

For the *Figure 5* measured results, a compensation capacitor ($C_{f'}$) was used across R_f to compensate for the summing node net capacitance due to the board and the SOT23–5 LMH6629. The R_A and R_B combination reduces the effective capacitance of Cf' by the ratio of $1+R_B / R_A$, with the constraint that $R_B << R_f$, thereby allowing a practical capacitance value (> 1pF) to be used. The LLP-8 package does not need this compensation across R_f due to its lower parasitics.

With the COMP pin HI (LLP-8 package only) or with the SOT23–5 package, this circuit achieves high slew rate and takes advantage of the LMH6629's superior low-noise characteristics without sacrificing stability, while enabling lower gain applications. It should be noted that the R_c, C_c combination *does* lower the input impedance and increases noise gain at higher frequencies. With these values, the input impedance reduces by 3dB at 490 MHz. The Noise Gain transfer function "zero" is given by the equation below and it has a 3dB increase at 32.8 MHz with these values:

$$\text{Noise Gain "zero"} \cong \frac{1}{2\pi(R_C + R_p + R_{EQ})C_C}$$

Equation 1: External Compensation Noise Gain Increase (1)

CANCELLATION OF OFFSET ERRORS DUE TO INPUT BIAS CURRENTS

The LMH6629 offers exceptional offset voltage accuracy. In order to preserve the low offset voltage errors, care must be taken to avoid voltage errors due to input bias currents. This is important in both inverting and non inverting applications.

The non-inverting circuit is used here as an example. To cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in *Figure 6*. Combining this constraint with the non-inverting gain equation also seen in *Figure 6* allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V\text{-}1)$$

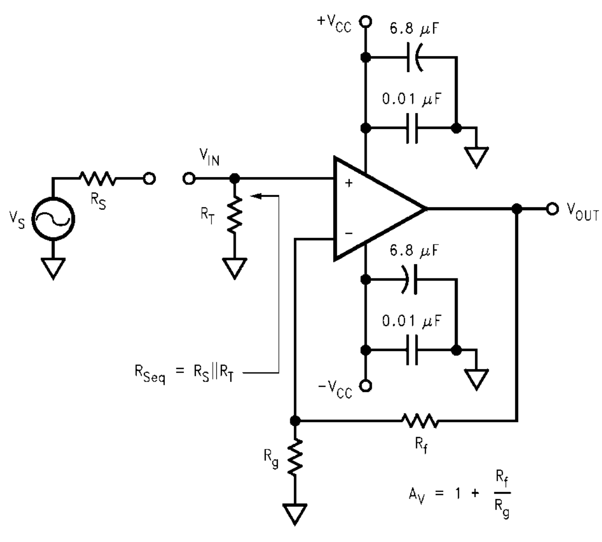


FIGURE 6. Non-Inverting Amplifier Configuration

When driven from a 0Ω source, such as the output of an op amp, the non-inverting input of the LMH6629 should be isolated with at least a 25Ω series resistor.

As seen in *Figure 7*, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input (R_f || (R_g+R_s)). R_b should to be no less than 25Ω for optimum LMH6629 performance. A shunt capacitor (not shown) can minimize the additional noise of R_b.

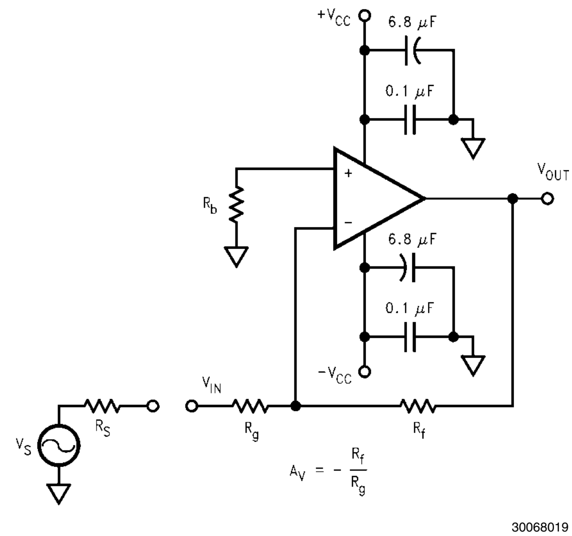


FIGURE 7. Inverting Amplifier Configuration

TOTAL INPUT NOISE vs. SOURCE RESISTANCE

To determine maximum signal-to-noise ratios from the LMH6629, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary. *Figure 8* describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) source, there is also thermal voltage noise ($e_t = \sqrt{(4KTR)}$) associated with each of the external resistors.

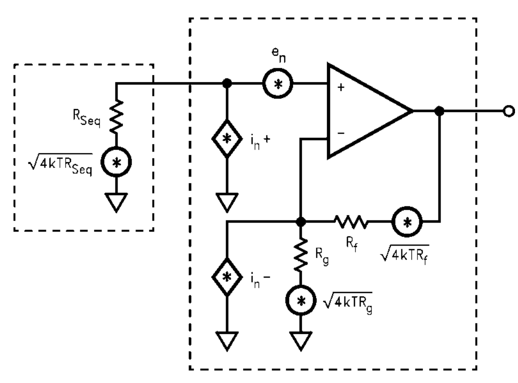


FIGURE 8. Non-Inverting Amplifier Noise Model

Equation 2 provides the general form for total equivalent input voltage noise density (e_{ni}).

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+}R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f||R_g\right)\right)^2 + 4kT\left(R_f||R_g\right)}$$

Equation 2: General Noise Equation (2)

Equation 3 is a simplification of *Equation 2* that assumes R_f || $R_g = R_{seq}$ for bias current cancellation:

$$e_{ni} = \sqrt{e_n{}^2 + 2(i_nR_{Seq})^2 + 4kT(2R_{Seq})}$$

Equation 3: Noise Equation with R_f || $R_g = R_{seq}$ (3)

Figure 9 schematically shows e_{ni} alongside V_{IN} (the portion of V_S source which reaches the non-inverting input of *Figure 6*) and external components affecting gain ($A_v = 1 + R_f / R_g$), all connected to an ideal noiseless amplifier.

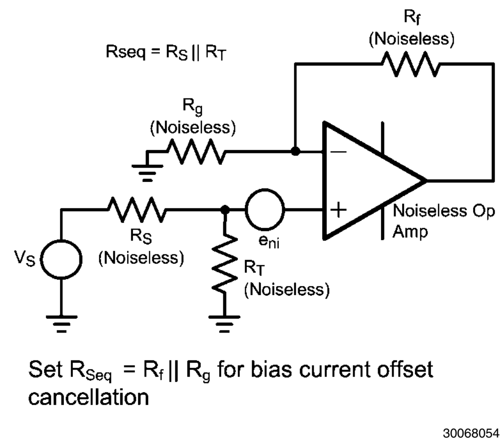


FIGURE 9. Non-Inverting Amplifier Equivalent Noise Source Schematic

Figure 10 illustrates the equivalent noise model using this assumption. *Figure 11* is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise source of *Equation 3*. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f || R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni} * A_V$.

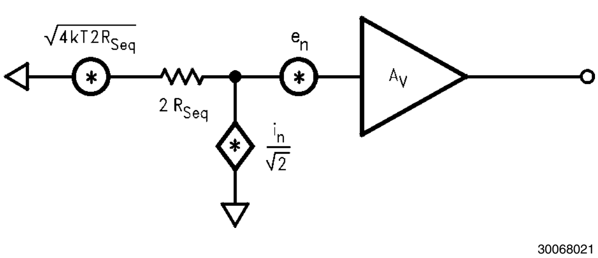


FIGURE 10. Noise Model with $R_f || R_g = R_{seq}$

As seen in *Figure 11*, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 15Ω. Between 15Ω and 2.5 kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{(4kT(2R_{seq}))}$) of the equivalent source resistance R_{seq}; incidentally, this is the range of R_{seq} values where the LMH6629 has the best (lowest) Noise Figure (NF) for the case where $R_{seq} = R_f || R_g$.

Above 2.5 kΩ, e_{ni} is dominated by the amplifier's current noise ($i_n = \sqrt{(2)}\, i_n R_{seq}$). When R_{seq} = 190Ω (i.e., $R_{seq} = e_n/\sqrt{(2)}\, i_n$), the contribution from voltage noise and current noise of LMH6629 is equal. For example, configured with a gain of +10V/V giving a −3dB of 825 MHz and driven from $R_{seq} = R_f || R_g$ = 20Ω (e_{ni} = 1.07 nV√Hz from *Figure 11*), the LMH6629 produces a total equivalent output noise voltage (e_{ni} * 10 V/V * √(1.57 * 825 MHz)) of 385 μV_{rms}.

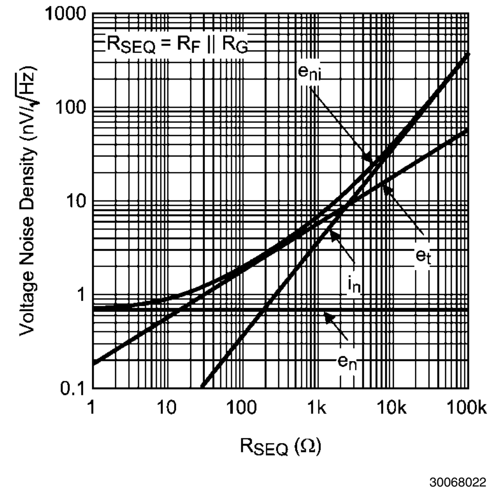


FIGURE 11. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f || R_g$ need not equal R_{seq}. In this case, according to *Equation 2*, $R_f || R_g$ should be as low as possible to minimize noise. Results similar to *Equation 2* are obtained for the inverting configuration of *Figure 7* if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, *Equation 2* will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains ($1+R_g/R_f$).

NOISE FIGURE

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\}$$

Equation 4: General Noise Figure Equation (4)

Looking at the two parts of the NF expression (inside the log function) yields:

$S_i/S_o \rightarrow$ Inverse of the power gain provided by the amplifier

$N_o/N_i \rightarrow$ Total output noise power, including the contribution of R_S, divided by the noise power at the input due to R_S

To simplify this, consider N_a as the noise power added by the amplifier (reflected to its input port):

$S_i/S_o \rightarrow 1/G$

$N_o/N_i \rightarrow G * (N_i+N_a) / N_i$ (where $G*(N_i+N_a) = N_o$)

Substituting these two expressions into the NF expression:

$$NF = 10\log\left[\frac{1}{G}\left(\frac{G(N_i+N_a)}{N_i}\right)\right] = 10\log\left(1+\frac{N_a}{N_i}\right)$$

Equation 5: Simplified Noise Figure Equation (5)

The noise figure expression has simplified to depend only on the ratio of the noise power added by the amplifier at its input (considering the source resistor to be in place but noiseless in getting N_a) to the noise power delivered by the source resistor (considering all amplifier elements to be in place but noiseless in getting N_i).

For a given amplifier with a desired closed loop gain, to minimize noise figure:

- Minimize $R_f || R_g$

- Choose the Optimum R_S (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx e_n / i_n$$

Figure 12 is a plot of NF vs R_S with the circuit of *Figure 6* (R_f = 240Ω, A_V = +10V/V). The NF curves for both Unterminated (R_T = open) and Terminated systems ($R_T = R_S$) are shown. *Table 1* indicates NF for various source resistances including $R_S = R_{OPT}$.

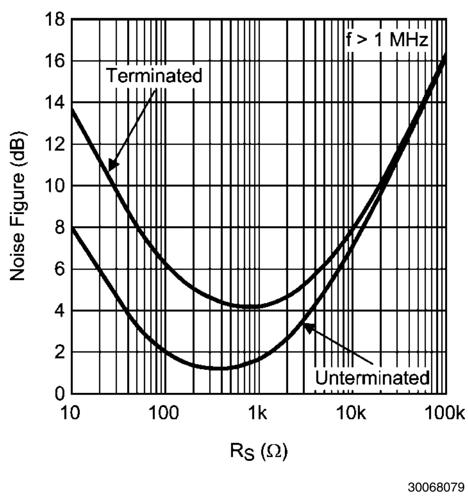


FIGURE 12. Noise Figure vs. Source Resistance

TABLE 1. Noise Figure for Various R_s

R_S (Ω)	NF (Terminated) (dB)	NF (Unterminated) (dB)
50	8	3.2
R_{OPT}	4.1 (R_{OPT} = 750Ω)	1.1 (R_{OPT} = 350Ω)

SINGLE-SUPPLY OPERATION

The LMH6629 can be operated with single power supply as shown in *Figure 13*. Both the input and output are capacitively coupled to set the DC operating point.

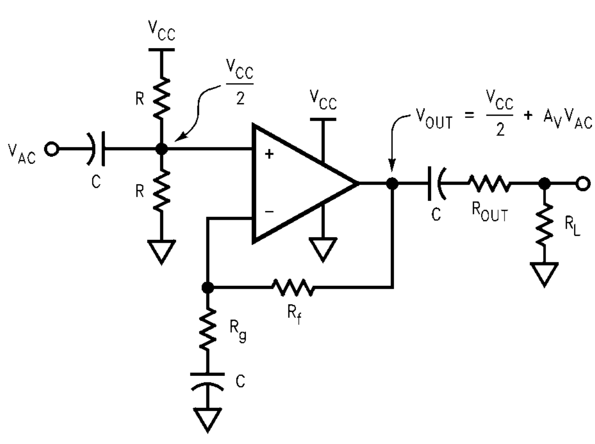


FIGURE 13. Single Supply Operation

LOW-NOISE TRANSIMPEDANCE AMPLIFIER

Figure 14 implements a high-speed, single-supply, low-noise Transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_F.

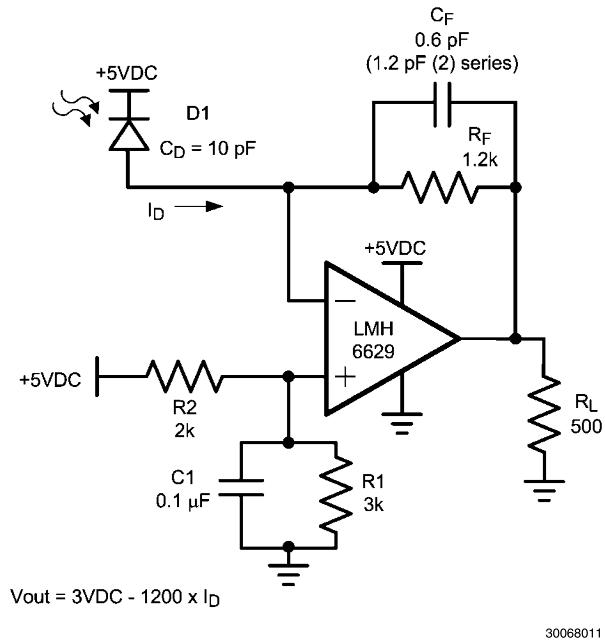


FIGURE 14. 200MHz Transimpedance Amplifier Configuration

Figure 15 shows the Noise Gain (NG) and transfer function (I-V Gain). As with most Transimpedance amplifiers, it is required to compensate for the additional phase lag (Noise Gain zero at f_Z) created by the total input capacitance (C_D (diode capacitance) + C_{CM} (LMH6629 input capacitance)) looking into R_F; this is accomplished by placing C_F across R_F to create enough phase lead (Noise Gain pole at f_P) to stabilize the loop.

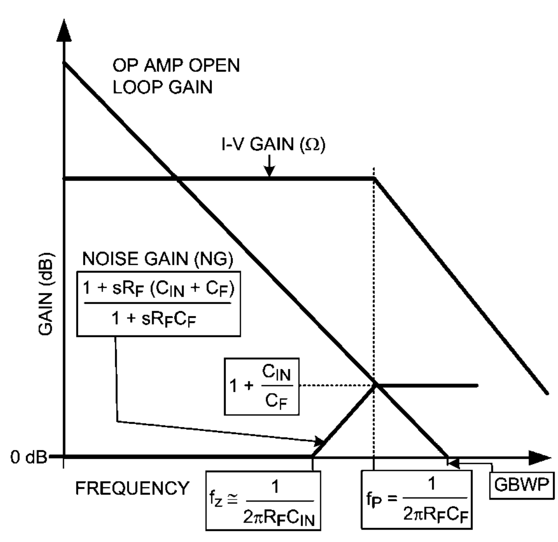


FIGURE 15. Transimpedance Amplifier Noise Gain & Transfer Function

The optimum value of C_F is given by *Equation 6* resulting in the I-V -3dB bandwidth shown in *Equation 7*, or around 200 MHz in this case (assuming GBWP= 4GHz with COMP pin = HI for LLP-8 package). This C_F value is a "starting point" and C_F needs to be tuned for the particular application as it is often less than 1pF and thus is easily affected by board parasitics, etc. For maximum speed, the LMH6629 COMP pin should be HI (for LLP-8 package). This CF value is a "starting point" and CF needs to be tuned for the particular application as it is often less than 1pF and thus is easily affected by board parasitics, etc. For maximum speed, the LMH6629 COMP pin should be HI (or use the SOT23 package).

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}}$$

Equation 6: Optimum C_F Value (6)

$$f_{-3\,dB} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}}$$

Equation 7: Resulting -3dB Bandwidth (7)

Equation 8 provides the total input current noise density (i_{ni}) equation for the basic Transimpedance configuration and is plotted against feedback resistance (R_F) showing all contributing noise sources in *Figure 16*. The plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_F). This is depicted in the schematic of *Figure 17* where total equivalent current noise density (i_{ni}) is shown at the input of a noiseless amplifier and noiseless feedback resistor (R_F). The total equivalent output voltage noise density (e_{no}) is i_{ni}*R_F.

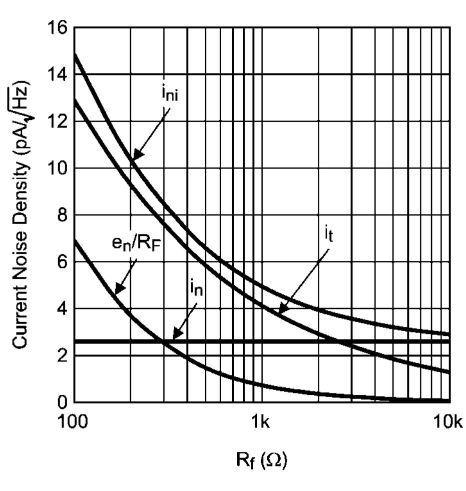


FIGURE 16. Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 8: Noise Equation for Transimpedance Amplifier (8)

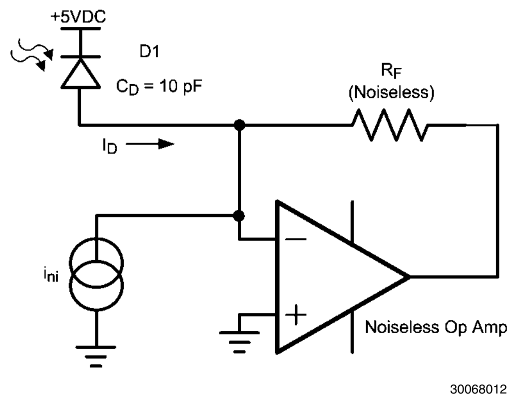


FIGURE 17. Transimpedance Amplifier Equivalent Input Source Model

From *Figure 16*, it is clear that with LMH6629's extremely low-noise characteristics, for $R_F < 2.5\text{k}\Omega$, the noise performance is entirely dominated by R_F thermal noise. Only above this R_F threshold, LMH6629's input noise current (i_n) starts being a factor and at no R_F setting does the LMH6629 input noise voltage play a significant role. This noise analysis has ignored the possible noise gain increase, due to photo-diode capacitance, at higher frequencies.

LOW-NOISE INTEGRATOR

Figure 18 shows a deBoo integrator implemented with the LMH6629. Positive feedback maintains integration linearity. The LMH6629's low input offset voltage and matched inputs allow bias current cancellation and provide for very precise integration. Keeping R_G and R_S low helps maintain dynamic stability.

$$V_O \cong V_{IN}\frac{K_O}{sR_SC}\quad ; \quad K_O = 1 + \frac{R_F}{R_G}$$

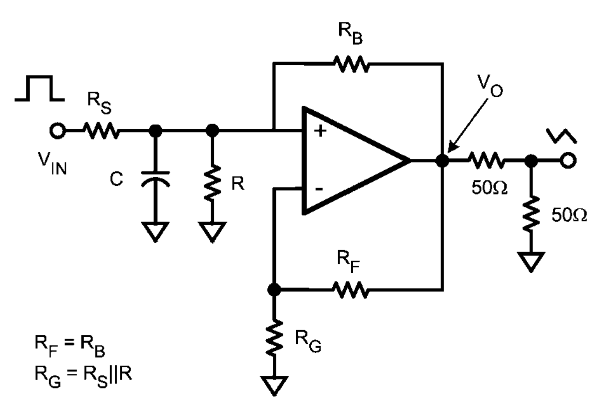


FIGURE 18. Low-Noise Integrator

HIGH-GAIN SALLEN-KEY ACTIVE FILTERS

The LMH6629 is well suited for high-gain Sallen-Key type of active filters. *Figure 19* shows the 2nd order Sallen-Key low-pass filter topology. Using component predistortion methods discussed in OA-21 enables the proper selection of components for these high-frequency filters.

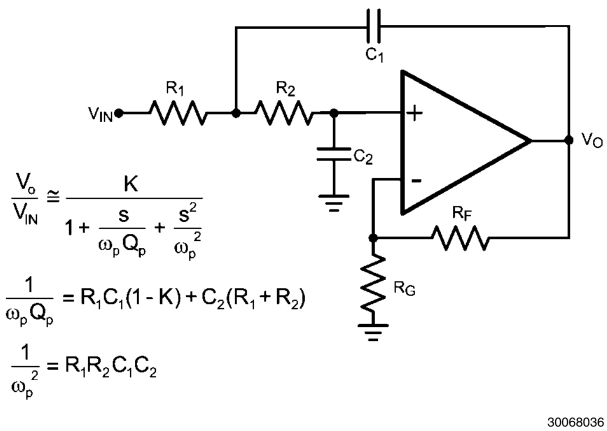


FIGURE 19. Low Pass Sallen-Key Active Filter Topology

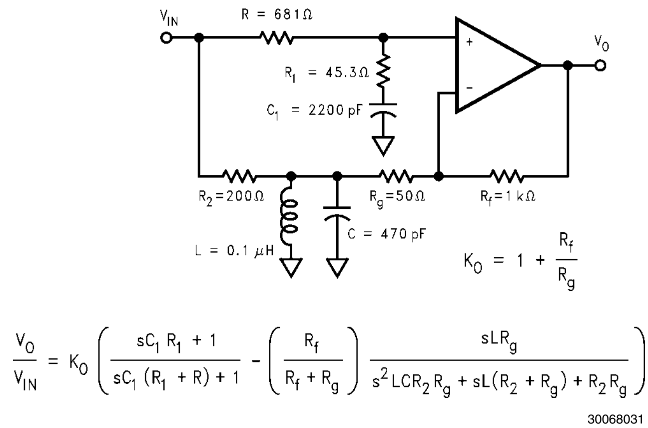


FIGURE 20. Low-Noise Magnetic Media Equalizer

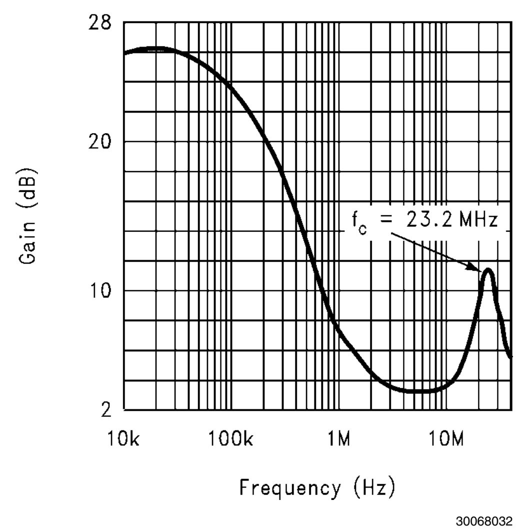


FIGURE 21. Equalizer Frequency Response

LOW-NOISE MAGNETIC MEDIA EQUALIZER

Figure 20 shows a high-performance low-noise equalizer for such applications as magnetic tape channels using the LMH6629. The circuit combines an integrator (used to limit noise) with a bandpass filter (used to boost the response centered at a frequency or over a band of interest) to produce the low-noise equalization. The circuit's simulated frequency response is illustrated in *Figure 21*.

In this circuit, the bandpass filter center frequency is set by

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$

For higher selectivity, use high C values; for wider bandwidth, use high L values, while keeping the product of L and C values the same to keep f_c intact. The integrator's -3dB roll-off is set by

$$\frac{1}{2\pi C_1 (R_1 + R)}$$

If

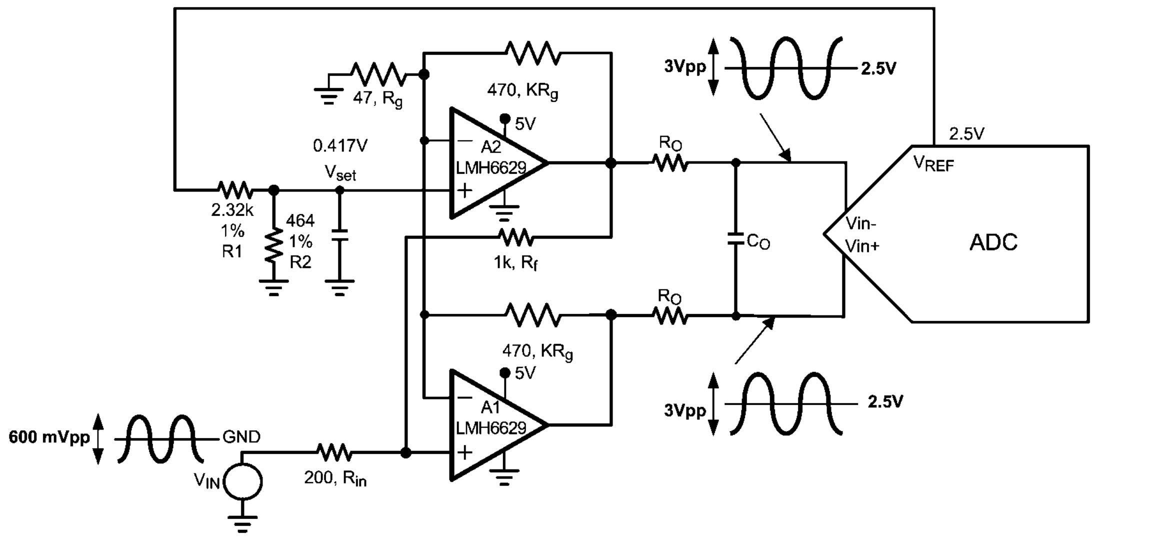
$$\frac{1}{2\pi C_1 R_1} << f_C$$

the integrator and the bandpass filter frequency interaction is minimized so that the operating frequencies of each can be set independently. Lowering the value of R2 increases the bandpass gain (boost) without affecting the integrator frequencies. With the LMH6629's wide Gain Bandwidth (4GHz), the center frequency could be adjusted higher without worries about loop gain limitation. This increases flexibility in tuning the circuit.

LOW-NOISE SINGLE ENDED TO DIFFERENTIAL CONVERTER / DRIVER

Many high-resolution data converters (ADC's) require a differential input driver. In order to preserve the ADC's dynamic range, the analog input driver must have a noise floor which is lower than the ADC's noise floor. For an ADC with N bits, the quantization Signal-to-noise ratio (SNR) is 6.02* N + 1.76 in dB. For example, a 12-bit ADC has a SNR of 74 dB (= 5000 V/V). Assuming a full-scale differential input of 2Vpp (0.707 V_RMS), the quantization noise referred to the ADC's input is ~140 μV_RMS (= 0.707 V_RMS / 5000 V/V) over the bandwidth "visible" to the ADC. Assuming an ADC input bandwidth of 20 MHz, this translates to just 25 nV/RtHz (= 141μV_RMS / SQRT(20 MHz * π/2)) noise density at the output of the driver. Using an amplifier to form the single-ended (SE) to Differential converter / driver for such an application is challenging, especially when there is some gain required. In addition, the input driver's linearity (harmonic distortion) must also be high enough such that the spurs that get through to the ADC input are below the ADC's LSB threshold or -73 dBc (= 20*log (1/2^{12})) or lower in this case. Therefore, it is essential to use a low-noise / low-distortion device to drive a high resolution ADC in order to minimize the impact on the quantization noise and to make sure that the driver's distortion does not dominate the acquired data.

Figure 22 shows a ground referenced bipolar input (symmetrical swing around 0V) SE to differential converter used to drive a high resolution ADC. The combination of LMH6629's low noise and the converter architecture reduces the impact on the ADC noise.



Governing Expressions:

$$K = \frac{V_{o\_diff}}{V_{in}}$$

$$R_{in} = \frac{2R_f}{K}$$

$$V_{set} = \frac{2V_{o\_CM}}{K+2}$$

Example:

$V_{o\_CM} = 2.5V$; $\quad K = 10$, Let $R_f = 1k\Omega \rightarrow Rin = 200\Omega$

$V_{o\_diff} = 6Vpp$; $\quad V_{set} = \frac{2 \times 2.5V}{10+2} = 0.417V$

$V_{in} = 600\,mVpp$

30068055

FIGURE 22. Low-Noise Single-Ended (SE) to Differential Converter

In this circuit, the required gain dictates the resistor ratio "K". With "K" and the driver output CM voltage (V_{O_CM}) known, V_{SET} can be established. Reasonable values for R_f and R_g can be set to complete the design.

In terms of output swing, with the LMH6629 output swing capability which requires ~0.85V of headroom from either rail, the maximum total output swing into the ADC is limited to 6.6 V_{PP} (=(5 – 2 x 0.85V) x 2); that is true with V_{O_CM} set to mid-rail between V+ and V-. It should also be noted that the LMH6629's input CMVR range includes the lower rail (V-) and that is the reason there is great flexibility in setting V_{o_CM} by controlling V_{SET}. Another feature is that A1 and A2 inputs act like "virtual grounds" and thus do not see any signal swing. Note that due to the converter's biasing, the source, V_{IN}, needs to sink a current equal to V_{SET} / R_{IN}.

The converter example shown in *Figure 22* operates with a noise gain of 6 (=1+ K / 2) and thus requires that the COMP pin to be tied low (LLP-8 package only). The 1st order approximated small signal bandwidth will be 280 MHz (=1.7 GHz / 6V/V) which is computed using 1.7GHz as the GBWP with COMP pin LO .

From a noise point of view, concentrating only on the dominant noise sources involved, here is the expression for the expected differential noise density at the input of the ADC:

$$V_{noise} \cong \sqrt{[e_n(1+K/2)]^2 .2^3 + [(e_{Rin\_thermal})K/2)]^2 .2^2 + [(e_{Rg\_thermal})K)]^2}$$

Equation 9: Converter Noise Expression (9)

e_n is the LMH6629 input noise voltage and $e_{Rin\_thermal}$ is the thermal noise of R_{IN}. The "2³" and the "2²" multipliers account for the different instances of each noise source (2 for e_n, and 1 for $e_{Rin\_thermal}$).

Equation 9 evaluated for the circuit example of *Figure 22* is shown below:

$$V_{noise} \cong \sqrt{[0.69\,nV/RtHz \times 6]^2 .2^3 + [1.82\,nV/RtHz \times 5]^2 .2^2 + [0.88\,nV/RtHz \times 10]^2} = 23.4\,nV/RtHz$$

Equation 10: Converter Noise Expression Evaluated (10)

Because of the LMH6629's low input noise voltage (e_n), noise is dominated by the thermal noise of R_{IN}. It is evident that the input resistor, R_{IN}, can be reduced to lower the noise with lower input impedance as the trade-off.

LAYOUT CONSIDERATIONS

National Semiconductor offers evaluation board(s) to aid in device testing and characterization and as a guide for proper layout. As is the case with all high-speed amplifiers, accepted-practice RF design technique on the PCB layout is mandatory. Generally, a good high-frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground may cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). Use high-quality chip capacitors with values in the range of 1000 pF to 0.1F for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, connect a tantalum capacitor with a value between 4.7 μF and 10 μF in parallel with the chip capacitor.

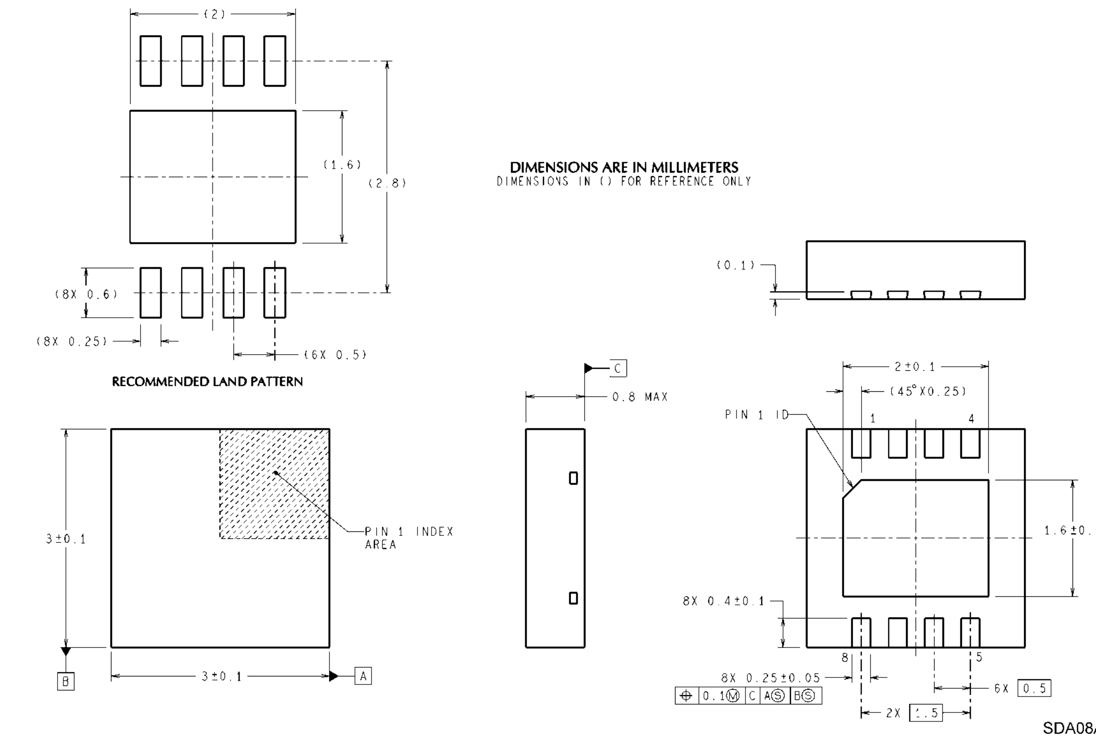
Harmonic Distortion, especially HD2, is strongly influenced by the layout and in particular can be affected by decoupling capacitors placed between the V^+ and V^- terminals as close to the device leads as possible.

Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Place input and output termination resistors as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

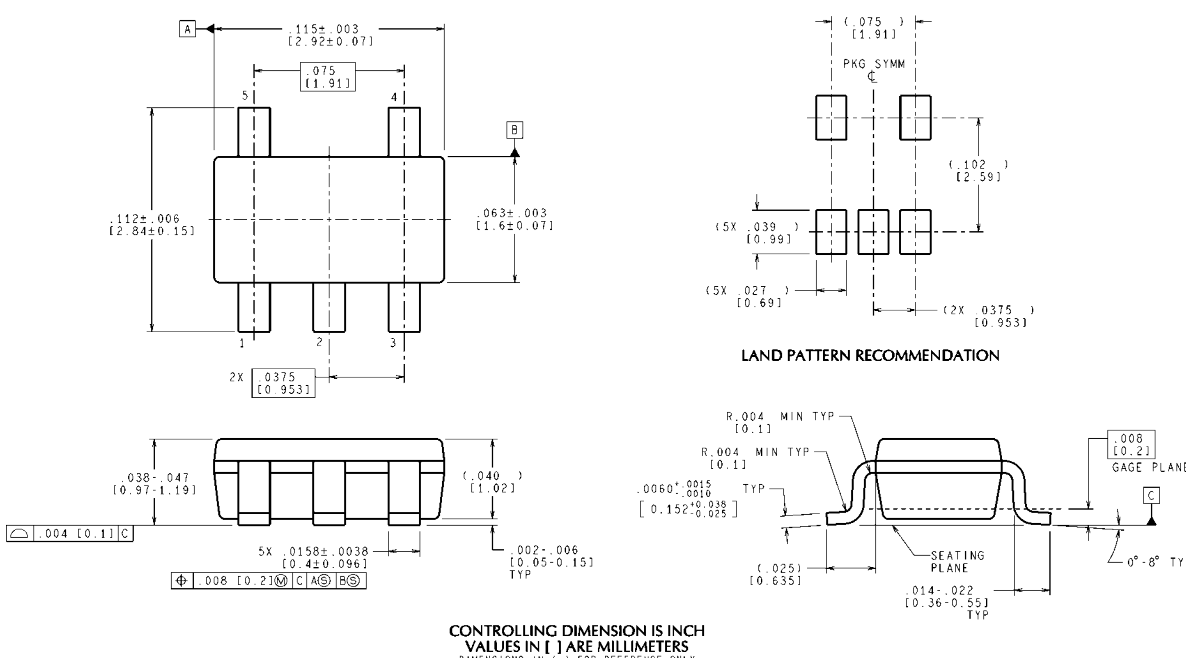
Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained to minimize the imbalance of amplitude and phase of the differential signal.

Component value selection is another important parameter in working with high-speed / high-performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and high distortion.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin LLP
NS Package Number SDA08A



MF05A (Rev D)

SOT23-5 Package
NS Package Number MF05A

Notes

Notes

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