

AN-2014 LMH2110 Evaluation Board

General Description

The evaluation board is designed to help the evaluation of the Texas Instruments LMH2110, which is a 45 dB Logarithmic RMS power detector particularly suited for accurate power measurement of modulated RF signals that exhibit large peak-to-average ratios, that is, large variations of the signal envelope. Such signals are encountered in W-CDMA and LTE cell phones. The RMS measurement topology inherently ensures a modulation insensitive measurement.

The device has an RF frequency range from 50 MHz to 8 GHz. It provides an accurate, temperature and supply insensitive, output voltage that relates linearly to the RF input power in dBm. The LMH2110's excellent conformance to a logarithmic response enables an easy integration by using slope and intercept only, reducing calibration effort significantly. The device operates with a single supply from 2.7V to 5V. The LMH2110 has an RF power detection range from -40 dBm to 5 dBm and is ideally suited for use in combination with a directional coupler. Alternatively a resistive divider can be used as well.

The device is active for EN = High, otherwise it is in a low power consumption shutdown mode. To save power and prevent discharge of an external filter capacitance, the output (OUT) is high-impedance during shutdown.

The LMH2110 power detector is offered in a tiny 6-bump DSBGA package.

[LMH2110 Evaluation Board](#) shows the LMH2110 Evaluation Board.

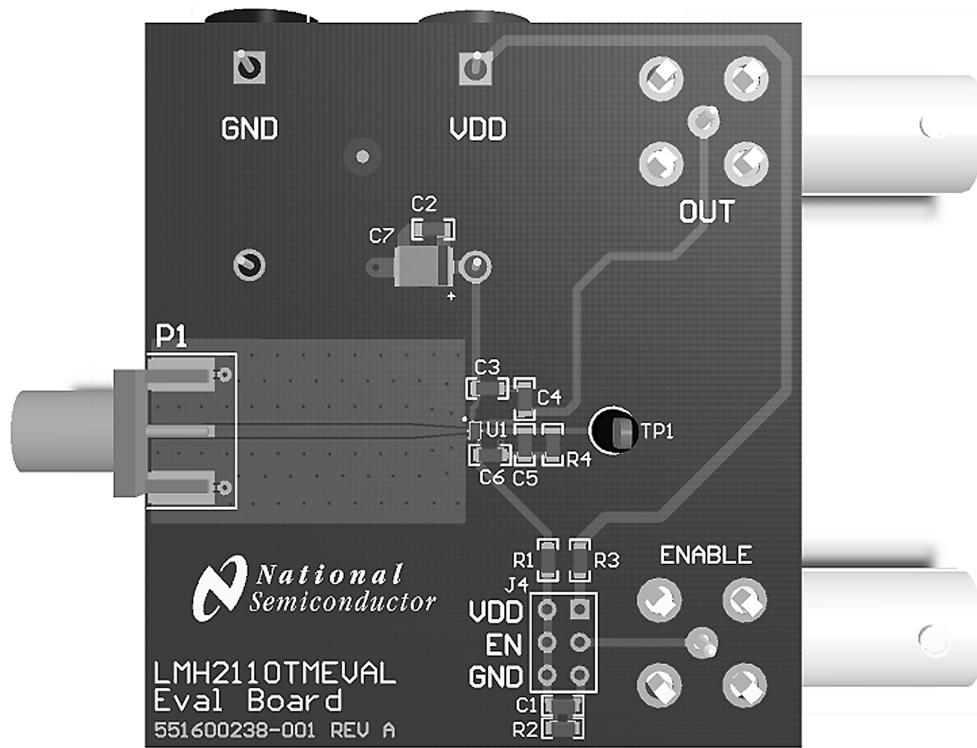
Basic Operation

The circuit operates with a single supply from 2.7V to 5V and has an RF power detection range from -40 dBm to 5 dBm. The board consists of a single LMH2110 along with external components soldered on a printed circuit board. External supply voltages and input signals can be applied to the on-board connectors. The supply voltage is applied with connectors P21 (VDD) and P22 (GND). The RF input signal is applied by SMA connector P1. This RF signal is applied through an RF generator and is connected with a 50Ω SMA cable. The detector output can be measured via BNC connector P3.

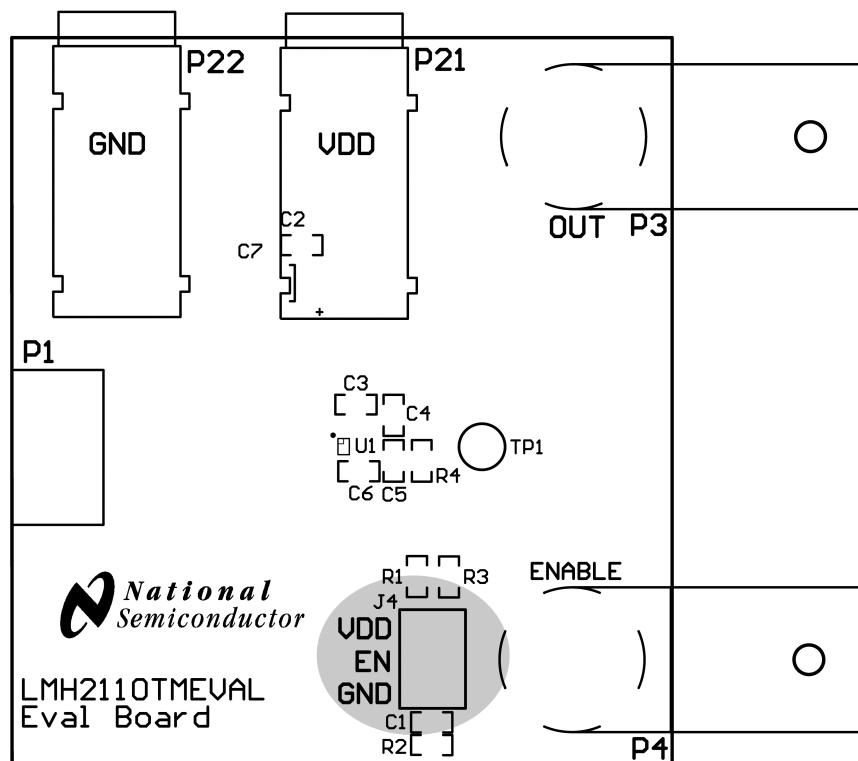
Configuration

The LMH2110 evaluation board can be configured via jumper settings. The device is active when EN = High. This can be accomplished by setting the jumper J4 to VDD or by using external control on P4 by setting the jumper J4 to EN. Since the device has an internal operating voltage of 2.5V, the voltage level on the enable should not be higher than 3V to prevent damage to the device. Also enable voltage levels lower than 400 mV below GND should be prevented. In both cases the ESD devices start to conduct when the enable voltage range is exceeded and excessive current will be drawn. To guarantee a correct operation a voltage divider formed by R2 and R3 is present on the evaluation board. The absolute maximum ratings are also exceeded when the enable (EN) is switched to HIGH (from shutdown to active mode) while the supply voltage is switched off. This situation should be prevented at all times. A solution to protect the device is the resistor R1 of 1 kΩ in series with the enable input to limit the current.

An overview of the various jumper positions on the board is given in [Jumper Positions](#). The settings of these jumpers and their functions are listed in [Jumper and Header Overview](#).



LMH2110 Evaluation Board



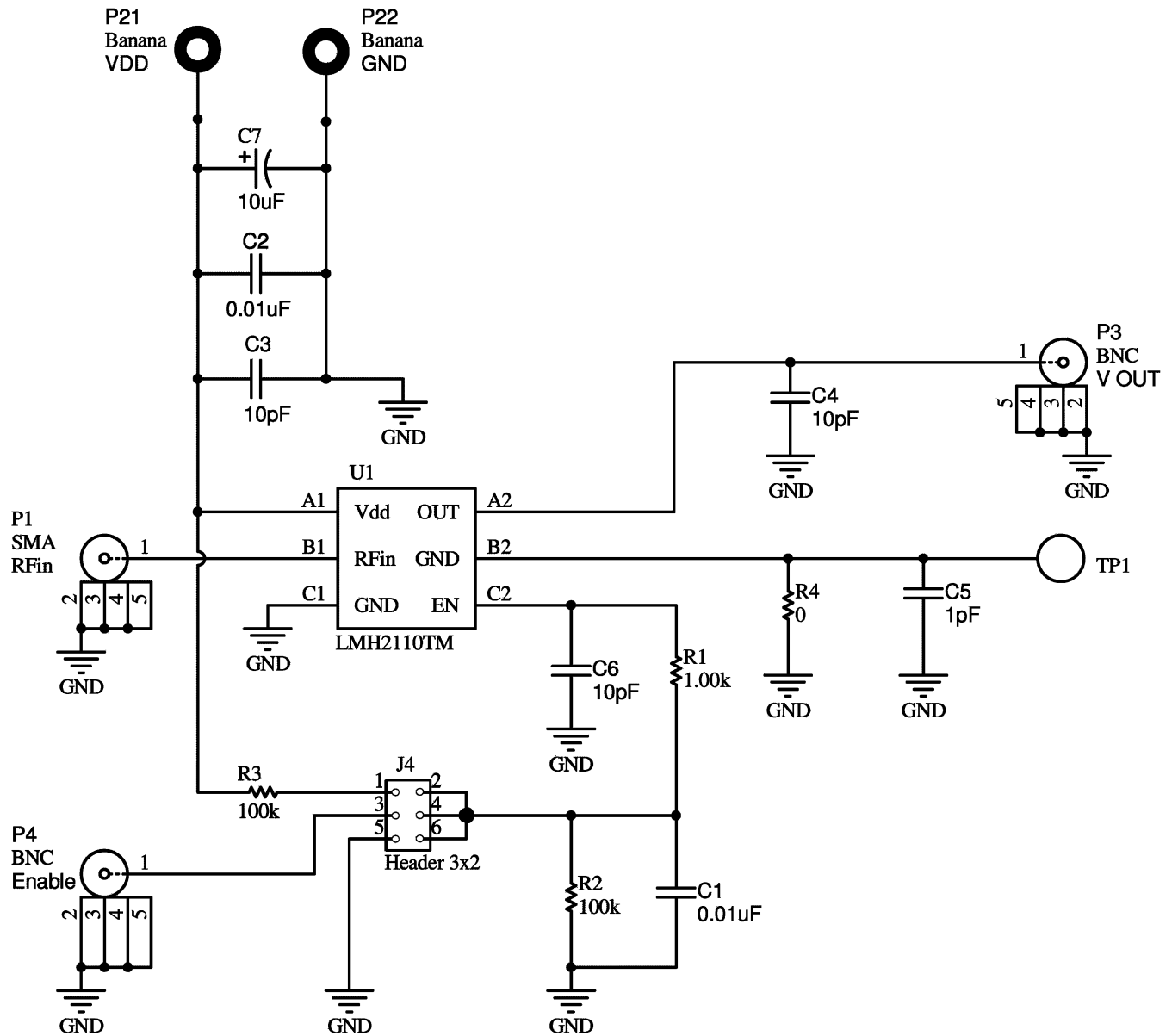
Jumper Positions

Jumper and Header Overview

Jumper	Function	Jumper Position	Description
J4	Enable	1-2	Active, Connects Enable Pin to VDD (factory default configuration)
		3-4	External Control, Connects Enable Pin to Enable P4
		5-6	Shutdown, Connects Enable Pin to GND

Schematic

The schematic of the evaluation board is shown in [Evaluation Board Schematic](#).



Evaluation Board Schematic

Bill of Materials

The Bill of Material (BOM) of the evaluation board is listed in [Bill of Materials of the Evaluation Board](#).

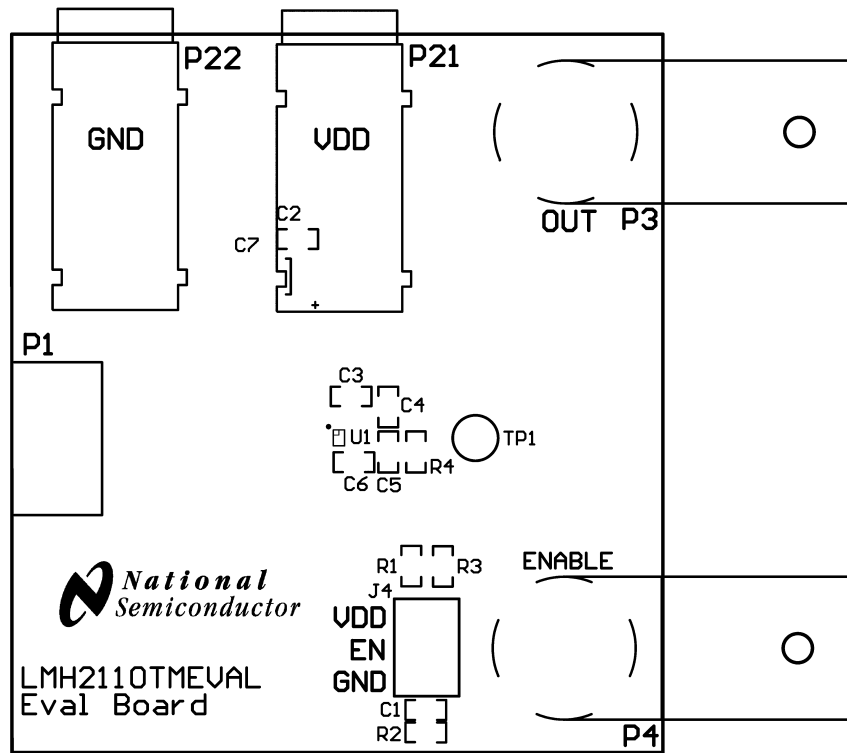
Bill of Materials of the Evaluation Board

Designator	Description	Comment
C1, C2	0603 Capacitor	10 nF
C3, C4, C6	0603 Capacitor	10 pF
C5	0603 Capacitor	1 pF
C7	0603 Capacitor	10 μ F
J4	Header	2x3
P1	Connector	SMA
P21, P22	Connector	Banana
P3	Connector	BNC
P4	Connector	BNC
R1	0603 Resistor	1 k Ω
R2, R3	0603 Resistor	100 k Ω
R4	0603 Resistor	0 Ω
TP1	Test Point	GND
U1	DSBGA	LMH2110

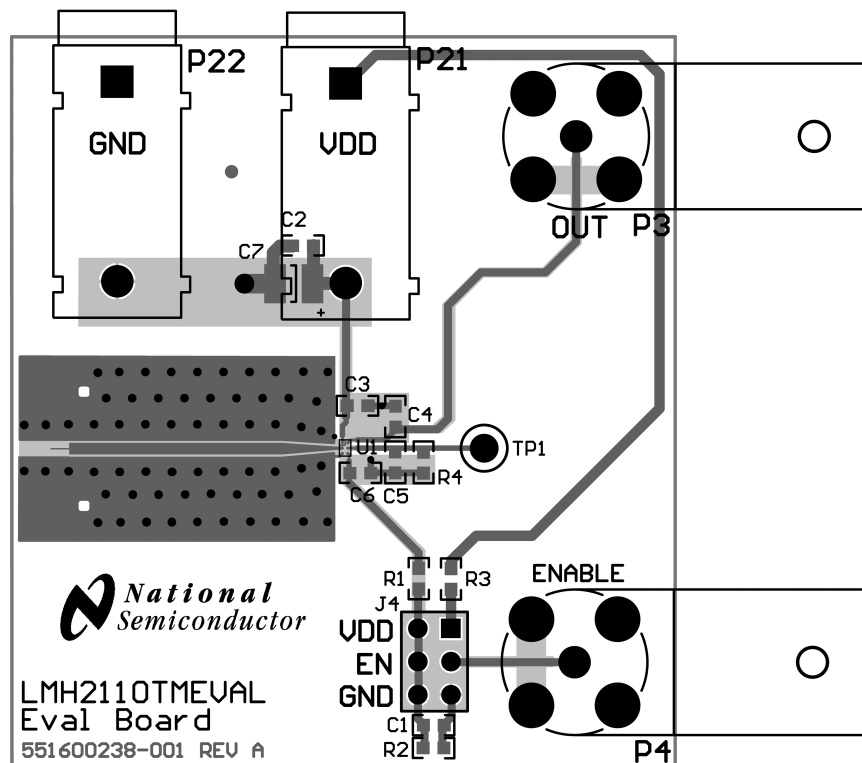
Board Layout

As with any other RF device, careful attention must be paid to the board layout. If the board layout isn't properly designed, performance might be less than can be expected for the application. The LMH2110 is designed to be used in RF applications, having a characteristic impedance of 50 Ω . To achieve this impedance, the input of the LMH2110 needs to be connected via a 50 Ω transmission line. Transmission lines can be created on PCBs using microstrip or (grounded) coplanar waveguide (GCPW) configurations. In order to minimize injection of RF interference into the LMH2110 through the supply lines, the PCB traces for VDD and GND should be minimized for RF signals. This can be done by placing a small decoupling capacitor between the VDD and GND. It should be placed as close as possible to the VDD and GND pins of the LMH2110.

[Component Locations of Evaluation Board](#) shows the component locations of the LMH2110 evaluation board and [Board Layout of Evaluation Board](#) shows the board layout of the LMH2110 evaluation board.



Component Locations of Evaluation Board

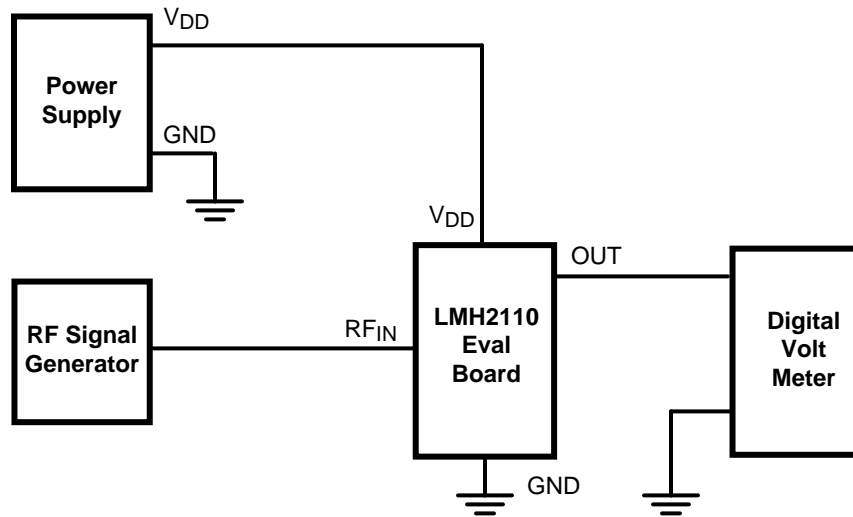


Board Layout of Evaluation Board

Measurement Procedure

The performance of the LMH2110 can be measured with the setup shown in [Measurement Setup](#).

An external power supply provides a voltage of 2.7V to 5V to the evaluation board. An accurate and stable RF Signal Generator is used to produce the test signal. It is recommended to use low loss cables to ensure reliable measurement data. The detected output voltage can be measured with a Digital Voltage Meter (DVM).



Measurement Setup

1 Measurement Results

[Figure 1](#) shows the output voltage versus frequency for various power levels on RF_{IN} . The frequency range is from 10 MHz to 10 GHz. [Figure 2](#) shows the output voltage versus RF input power for various frequencies.

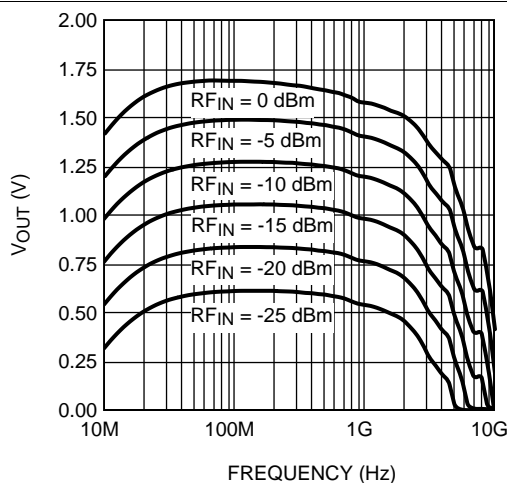


Figure 1. Output Voltage vs. Frequency

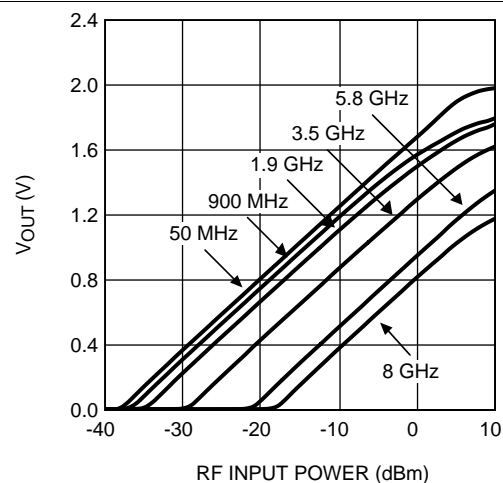


Figure 2. Output Voltage vs. RF Input Power

Revision History

Changes from A Revision (April 2013) to B Revision **Page**

- Changed Figures 7 and 8 to correct for Y axis values placement [7](#)
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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