National Semiconductor

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LM8801

High Precision 6MHz, 600 mA Synchronous Step-Down DC-DC Converter for Mobile Applications

General Description

The LM8801 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Li-Ion cell and input voltage rails from 2.3V to 5.5V. It provides up to 600 mA load current over the entire input voltage range.

The LM8801 has a mode-control pin that allows the user to select continuous PWM operation over the complete load range or an auto PFM-PWM mode that changes modes automatically depending on the load. During PWM mode, the device operates at a fixed-frequency of 6 MHz (typ.). In Auto PFM-PWM mode, hysteretic PFM extends the battery life through reduction of the quiescent current during light loads and system standby.

The LM8801 is available in a 6-bump micro SMD package. Only three compact external surface-mount components, an inductor and two capacitors, are required.

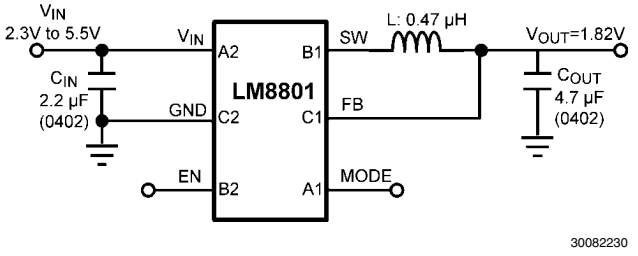
Features

- Over 90% efficiency at 6 MHz Operation
- 600 mA maximum load capability
- 6 MHz PWM fixed switching frequency (typ.)
- 27 µA (typ.) quiescent current in PFM mode
- Wide Input Voltage Range: 2.3V to 5.5V
- ±1.5% DC output voltage precision over temperature
- Best-in-class load transient response
- Low output ripple in PFM mode
- Automatic PFM/PWM mode switching
- Current overload and thermal shutdown protection
- Internal soft-start
- Micro SMD 6–bump package (1.065 x 1.265 , 0.6 mm or 0.25 mm height)
- Total solution size < 7mm² (works with 0402 capacitors)
- UVLO

Applications

- Mobile Phones
- MP3 players
- Wireless LAN
- PDAs, Pocket PCs
- Portable Hard Disk Drives

Typical Application Circuit



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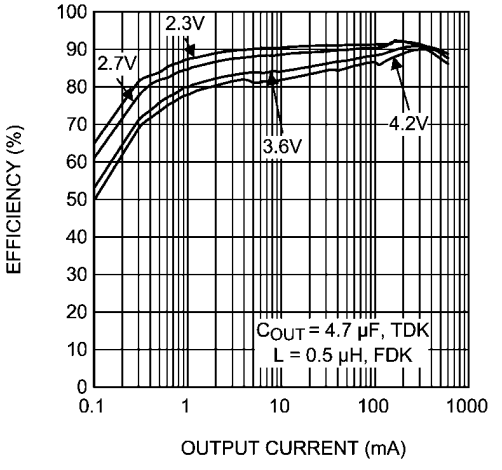
Efficiency vs. Output Current (Auto Mode, V_{OUT} = 1.82V)



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Connection Diagram and Package Mark Information

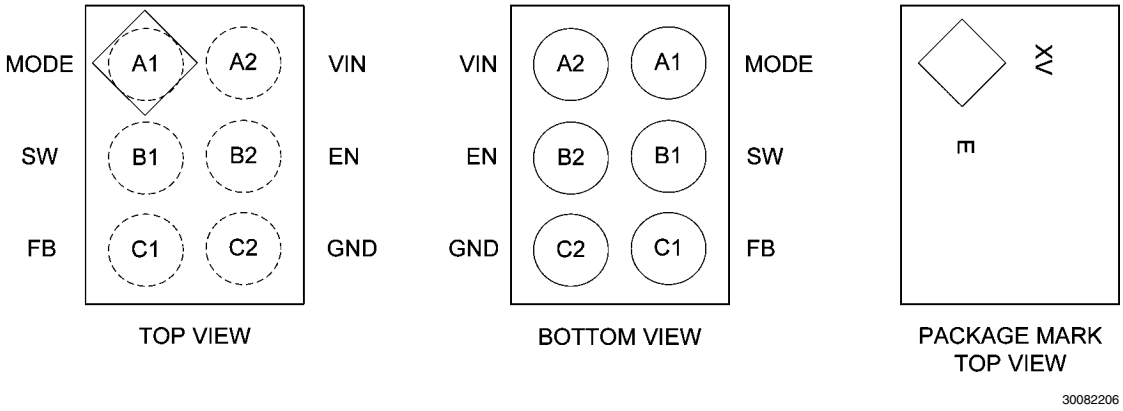

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FIGURE 1. 6-Bump micro SMD Package

Note: The actual physical placement of the package marking will vary from part to part. The package marking "X" designates the date code; "V" is an NSC internal code for die traceability. Both will vary in production.

Pin Descriptions

Pin Number	Name	Description
A1	Mode	Auto mode and forced PWM mode selection. Forced PWM = HIGH; Auto = LOW.
A2	VIN	Power supply input. Connect to the input filter capacitor (Typical Application Circuit, page 1).
B1	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
B2	EN	Enable pin. The device is in shutdown mode when voltage to this pin is < 0.4V and enabled when > 1.2V. Do not leave this pin floating.
C1	FB	Feedback analog input. Connect directly to the output filter capacitor (Typical Application Circuit, page 1).
C2	GND	Ground pin.

Ordering Information (6-Bump micro SMD)

Order Number 6–bump Micro SMD	Package Marking	Supplied As
LM8801TME-1.82*	E	250 units, Tape-and-Reel
LM8801TMX-1.82*	E	3000 units, Tape-and-Reel
LM8801TME-2.9	E	250 units, Tape-and-Reel
LM8801TMX-2.9	E	3000 units, Tape-and-Reel
LM8801XUE-1.82	E	250 units, Tape-and-Reel
LM8801XUX-1.82	E	3000 units, Tape-and-Reel

* Samples available

Dissipation Rating Table

θ_{JA}	$T_A \leq 25°C$ Power Rating	$T_A = 60°C$ Power Rating	$T_A = 85°C$ Power Rating
85°C/W (*Note 6*)	1176 mW	765 mW	470 mW

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} Pin to GND	−0.2V to 6.0V
EN, MODE pin to GND	−0.2V to 6.0V
FB, SW pin	(GND−0.2V) to (V_{IN} + 0.2V) w/ 6.0V max
Junction Temperature ($T_{J\text{-}MAX}$)	+150°C
Storage Temperature Range	−65°C to +150°C
Continuous Power Dissipation (*Note 3*)	Internally Limited
Maximum Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating (*Note 4*)	
Human Body Model	2 kV
Machine Model	200V

Operating Ratings (*Note 1*, *Note 2*)

Input Voltage Range	2.3V to 5.5V
Recommended Load Current	0 mA to 600 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (*Note 5*)	−30°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Micro SMD) (*Note 6*)	85°C/W

Electrical Characteristics (*Note 2*, *Note 7*, *Note 8*)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−30°C ≤ T_A = T_J ≤ +85°C). Unless otherwise noted, specifications apply to the LM8801 open loop Typical Application Circuit with V_{OUT} = 1.82V, V_{IN} = EN = 3.6V.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{FB}	Feedback Voltage Tolerance	PWM	**-1.5**		**+1.5**	%
V_{OUT}	Line Reg. (closed loop)	2.3V ≤ V_{IN} ≤ 5.5V; I_{OUT} = 10 mA (PFM)		0.2		%/V
		2.3V ≤ V_{IN} ≤ 5.5V; I_{OUT} = 200 mA (PWM)		0.048		
	Load Reg. (closed loop)	0.1 mA ≤ I_{OUT} ≤ 600 mA; V_{IN} = 3.6V (Auto)		0.0019		%/mA
I_{SHDN}	Shutdown Supply Current	EN = 0V, SW = GND		0.08	**1.0**	µA
I_{Q_PFM}	Quiescent Current in PFM Mode	No load, device is not switching		27	**35**	µA
I_{Q_PWM}	Quiescent Current in PWM Mode	No load, device is not switching		0.57	**0.7**	mA
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	V_{IN} = V_{GS} = 3.6V		220		mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for Sync NFET	V_{IN} = V_{GS} = 3.6V		180		mΩ
I_{LIM}	PFET Peak Current Limit		**900**	1100	**1300**	mA
V_{IH}	Logic High Input, all control pins		**1.2**			V
V_{IL}	Logic Low Input				**0.4**	V
$I_{EN,MODE}$	Pin Input Current			0.01	1	µA
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**5.6**	6.0	**6.4**	MHz
UVLO	Under-Voltage Lock Out			2.0		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).

Note 4: The Human Body Model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883–3015.7.

Note 5: In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction-to-ambient thermal resistance of the part/package (θ_{JA}) in the application, as given by the following equation: $T_{A-MAX} = T_{J-MAX} - (\theta_{JA} \times P_{D-MAX})$. Due to the pulsed nature of testing the part, the temp in the Electrical Characteristic table is specified as $T_A = T_J$.

Note 6: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.

Note 7: Min and Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: The parameters in the electrical characteristic table are tested under open loop conditions at V_{IN} = 3.6V unless otherwise specified. For performance over the input voltage range and closed loop condition, refer to the datasheet curves.

Block Diagram

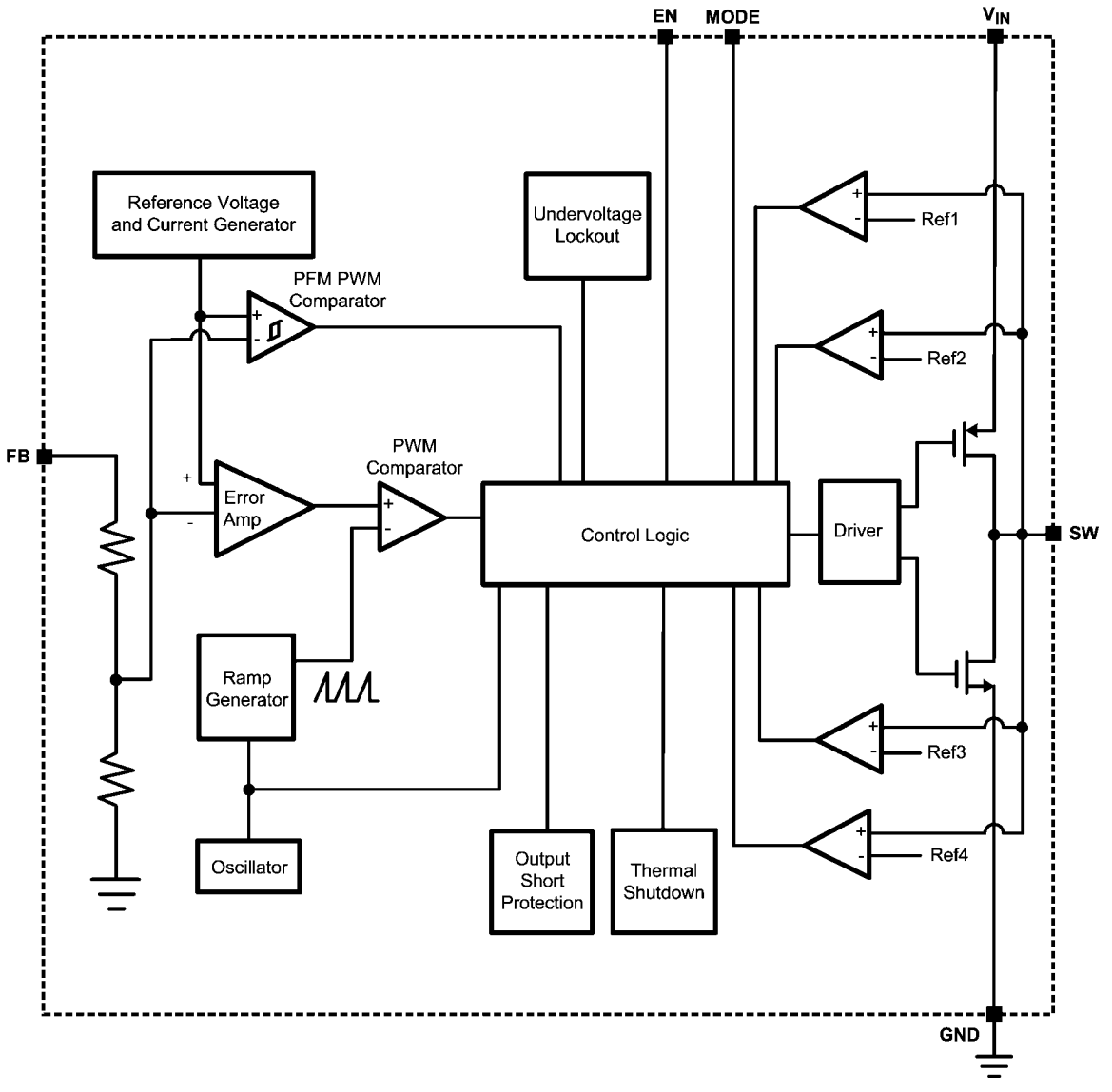
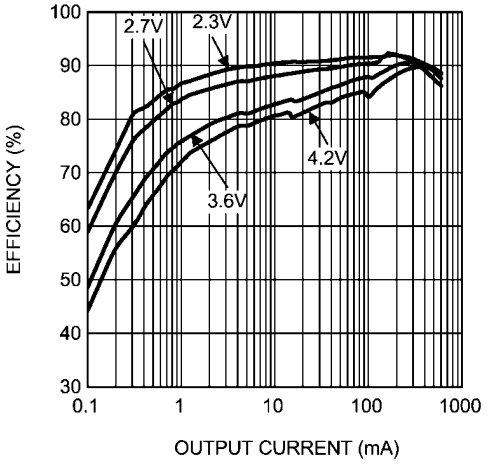


FIGURE 2. Simplified Functional Diagram

Typical Performance Characteristics

LM8801TM-1.82, Typical Application Circuit (page 1), V_{OUT} = 1.82V, V_{IN} = 3.6V, T_A = 25°C, C_{IN} = 2.2 µF, 0402 (JMK105BJ225MV-F), C_{OUT} = 4.7 µF, 0402, 6.3V (CL05A475MQ5NRNC), L = 0.5 µH, 2012 (MIPSZ2012D0R5), unless otherwise noted.

Efficiency vs. Output Current (Auto Mode)



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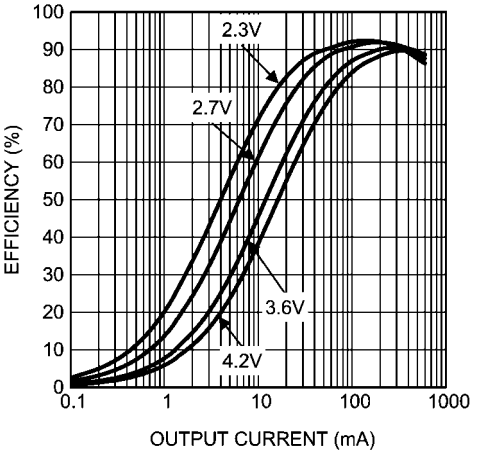
Efficiency vs. Output Current (PWM Mode)



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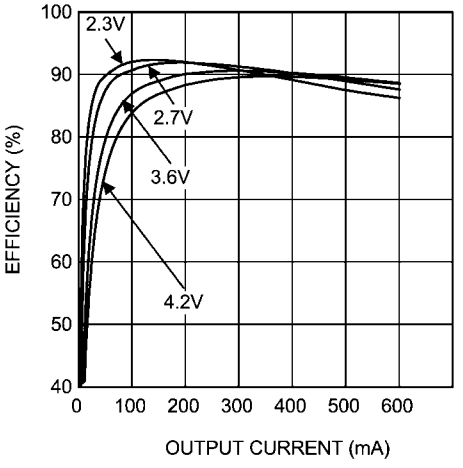
Efficiency vs. Output Current (PWM Mode)



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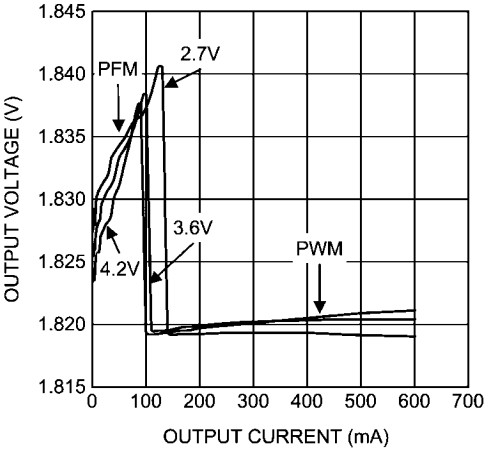
Output Voltage vs. Output Current (Auto Mode)



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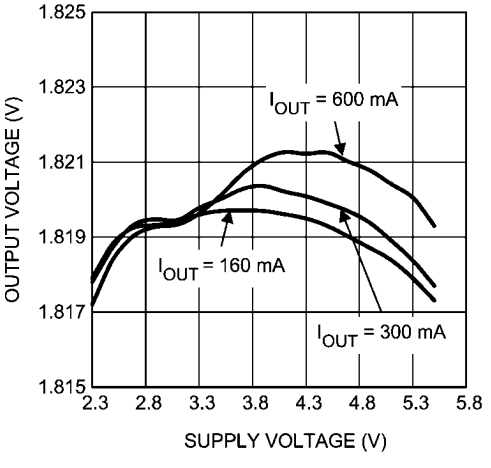
Output Voltage vs. Supply Voltage (PWM)



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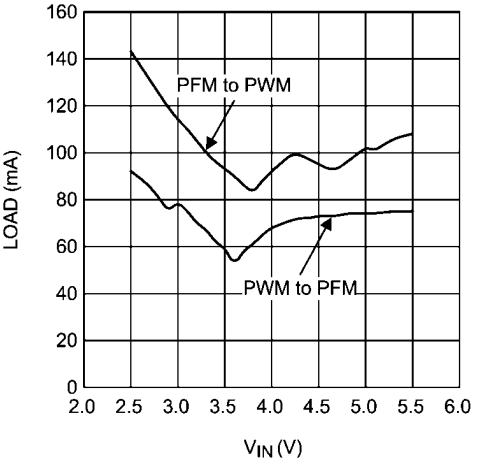
PFM ↔ PWM Mode Change Point



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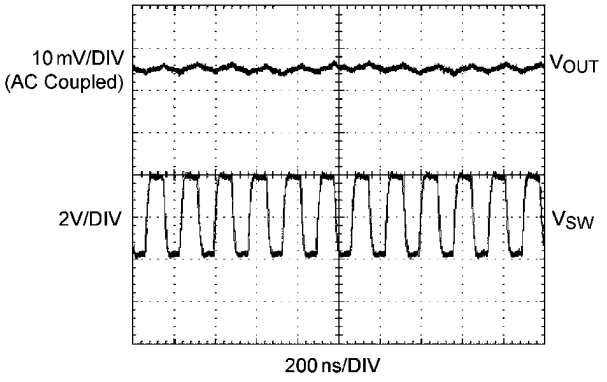
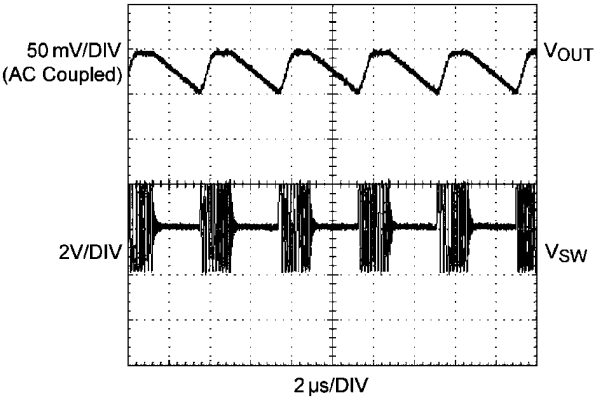
Typical Switching Waveform
(PWM Mode, I_{OUT} = 300 mA)



30082210

Typical Switching Waveform
(PFM Mode I_{OUT} = 50 mA)



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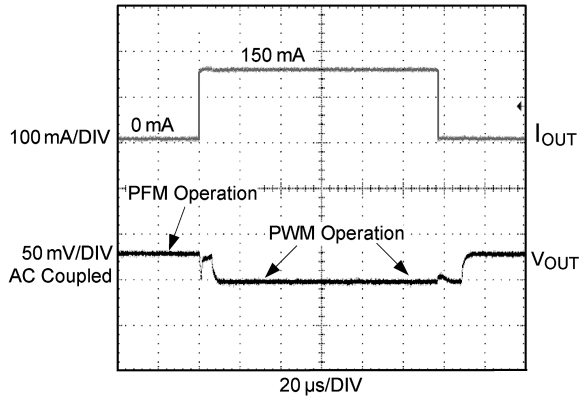
Load Transient Response
(0 ↔ 150 mA)



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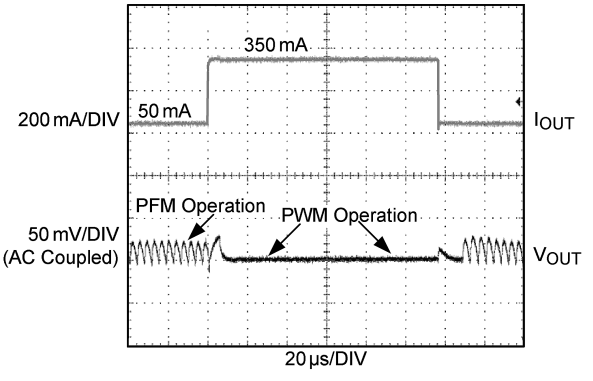
Load Transient Response
(50 ↔ 350 mA)



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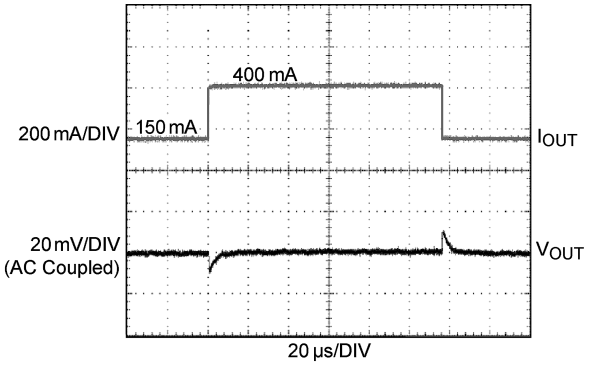
Load Transient Response
(150 ↔ 400 mA)



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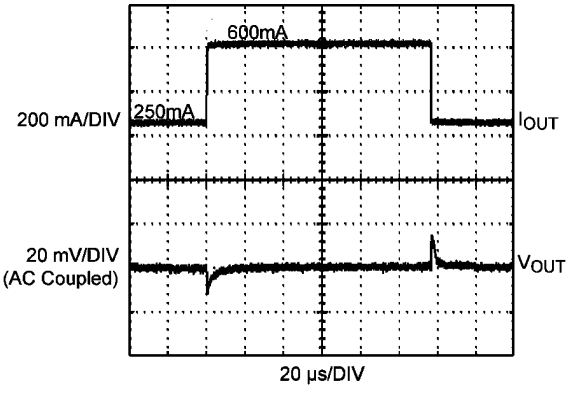
Load Transient Response
(250 ↔ 600 mA)



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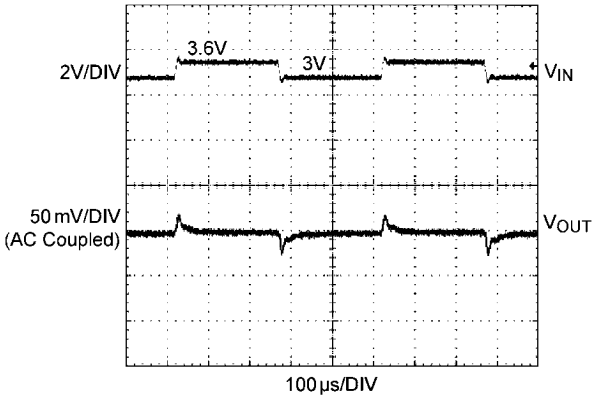
Line Transient Response
(3.0 V_{IN} ↔ 3.6 V_{IN}, 250 mA)



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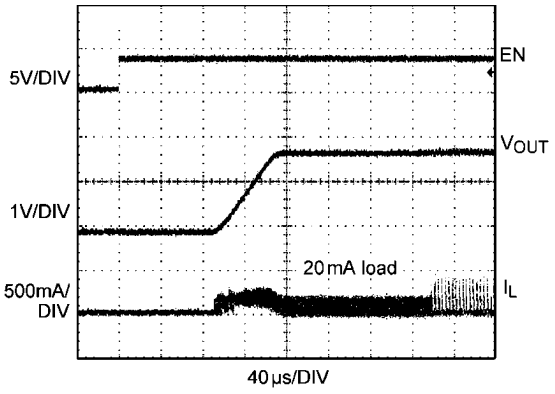
Startup in PFM Mode (I_{OUT} = 20 mA)



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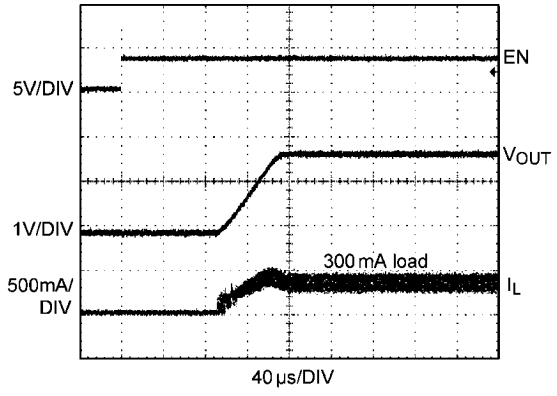
Startup in PWM Mode (I_{OUT} = 300 mA)



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Operation Description

DEVICE INFORMATION

The LM8801, a high-efficiency, step-down DC-DC switching buck converter, delivers a constant voltage from either a single Li-Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM8801 has the ability to deliver up to 600 mA depending on the input voltage and output voltage, ambient temperature, and the inductor chosen.

There are three modes of operation depending on the current required - PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation), and shutdown. The device operates in PWM mode at load currents of approximately 80 mA or higher, having voltage precision of ±1.5% with 90% efficiency or better. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_Q = 27 µA typ.) and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.08 µA typ.).

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in the Typical Application Circuit, only three external power components are required for implementation.

CIRCUIT OPERATION

The LM8801 operates as follows. During the first portion of each switching cycle, the control block in the LM8801 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} - V_{OUT})/L$, by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $-V_{OUT}/L$.

The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation, the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

AUTO MODE OPERATION

Setting Mode pin low places the LM8801 in Auto mode. By doing so the device will automatically switch between PFM state and PWM (Pulse Width Modulation) state based on load demand. At light loads (less than 50 mA), the device enters PFM mode and operates with reduced switching cycle and supply current to maintain high efficiency. During PFM operation, the converter positions the output voltage slightly higher (+15 mV typ.) than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load.

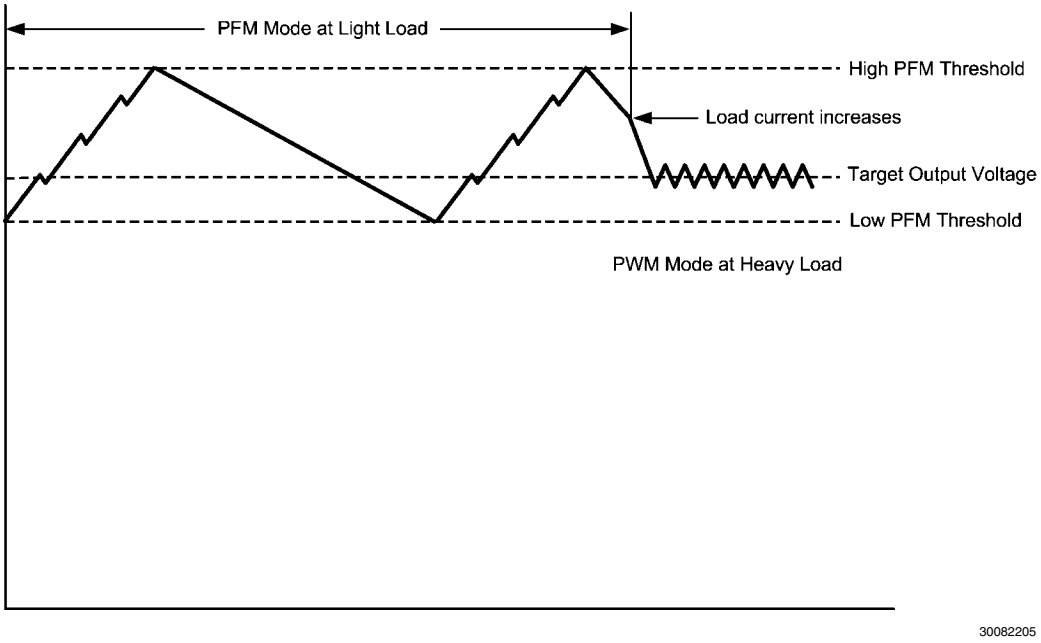


FIGURE 3. Operation in PFM Mode and Transfer to PWM Mode

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the LM8801 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows the LM8801 to protect itself and external components during overload conditions. PWM mode implements current limit using an internal comparator that trips at 1.1A (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

SHUTDOWN MODE

Setting the EN input pin low (<0.4V) places the LM8801 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM8801 are turned off. Setting EN high (>1.2V) enables normal operation. While turning on the device with EN soft-start is activated. EN pin should be set low to turn off the LM8801 during system power up and under-voltage conditions when the supply is less than 2.3V. Do not leave the EN pin floating.

SOFT-START

The LM8801 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.3V.

THERMAL SHUTDOWN PROTECTION

The LM8801 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 130°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

UVLO (UNDER-VOLTAGE LOCK OUT)

The LM8801 has an UVP comparator to turn the power device off in the case the input voltage or battery voltage is too low. The typical UVP threshold is around 2V with 100 mV hysteresis.

Application Information

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings at maximum ambient temperature of application should be requested from manufacturer.

Minimum value of inductance to guarantee good performance is 0.3 µH at (I_{LIM} typ.) bias current over the ambient temp range.

Shielded inductors radiate less noise and should be preferred. There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average to peak inductor current
- I_{OUTMAX}: maximum load current (600 mA)
- V_{IN}: maximum input voltage in application
- L: minimum inductor value including worst case tolerances (30% drop can be considered for method 1)
- f: minimum switching frequency (5.4 MHz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that can handle the maximum current limit of 1300 mA.

The inductor's resistance should be less than around 0.1Ω for good efficiency. *Table 1* lists suggested inductors and suppliers.

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 2.2 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0402 and 0603.

The input filter capacitor supplies current to the top switch of the LM8801 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating.

The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f \times I_{OUTMAX} \times V_{IN}}$$

The worst case is when $V_{IN} = 2 \times V_{OUT}$.

TABLE 1. Suggested Inductors and Suppliers

Model	Vendor	Dimensions LxWxH (mm)
MIPSZ2012D0R5	FDK	2.0 x 1.2 x 1.0
LQM21PNR54MG0D	Murata	2.0 x 1.2 x 0.9
HSLI-201208AG-R47	Hitachi Metals	2.0 x 1.2 x 0.8

OUTPUT CAPACITOR SELECTION

Use a 4.7 µF, 6.3V ceramic capacitor, X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes 0402 and 0603. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. **Minimum output capacitance to guarantee good performance is 2.2 µF (for 4.7 µF capacitor) at 1.8V DC bias including tolerances and over ambient temp range.**

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance =

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4 * f * C}$$

Voltage peak-to-peak ripple due to ESR =

$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR}$

Because these two components are out of phase, the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared =

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2}$$

Note that the output voltage ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 2 lists suggested capacitors and suppliers.

TABLE 2. Suggested Capacitors and Suppliers

Model	Vendor	Case Size Inch (mm)
GRM155R60J225ME15 (C_{IN})	Muruta	0402 (1005)
JMK105BJ225MV-F (C_{IN})	Taiyo Yuden	0402 (1005)
CL05A475MQ5NRNC (C_{IN} or C_{OUT})	Samsung	0402 (1005)

MICRO SMD PACKAGE ASSEMBLY AND USE

Use of the micro SMD package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in National Semiconductor Application Note 1112. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device.

The pad style used with micro SMD package must be the NSMD (Non-Solder Mask Defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 for specific instructions how to do this.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the micro SMD package and board pads. Poor solder joints can result in erratic or degraded performance.

Good layout for the LM8801 can be implemented by following a few simple design rules, as illustrated in *Figure 4*.

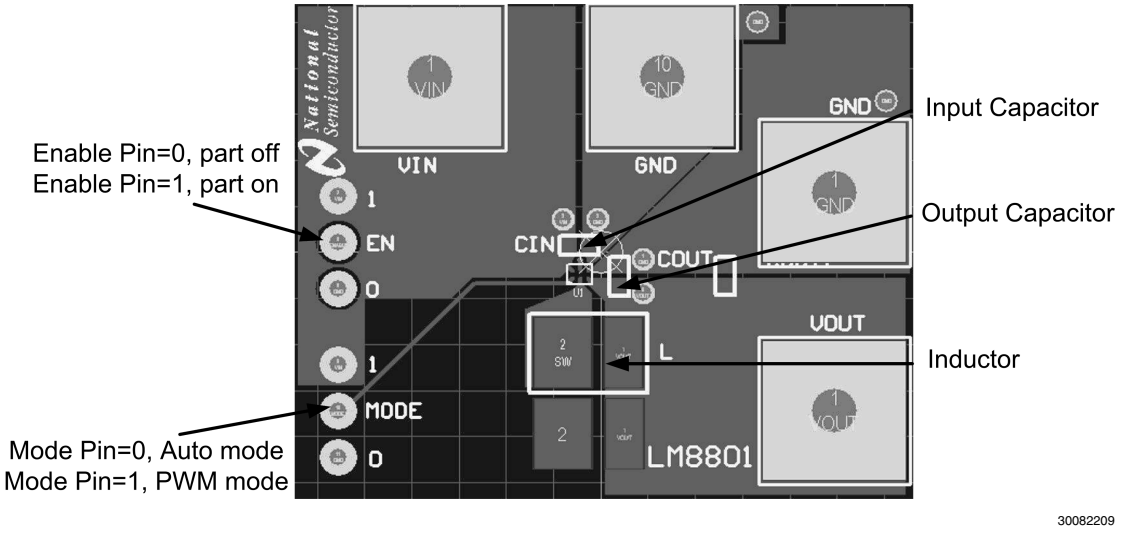


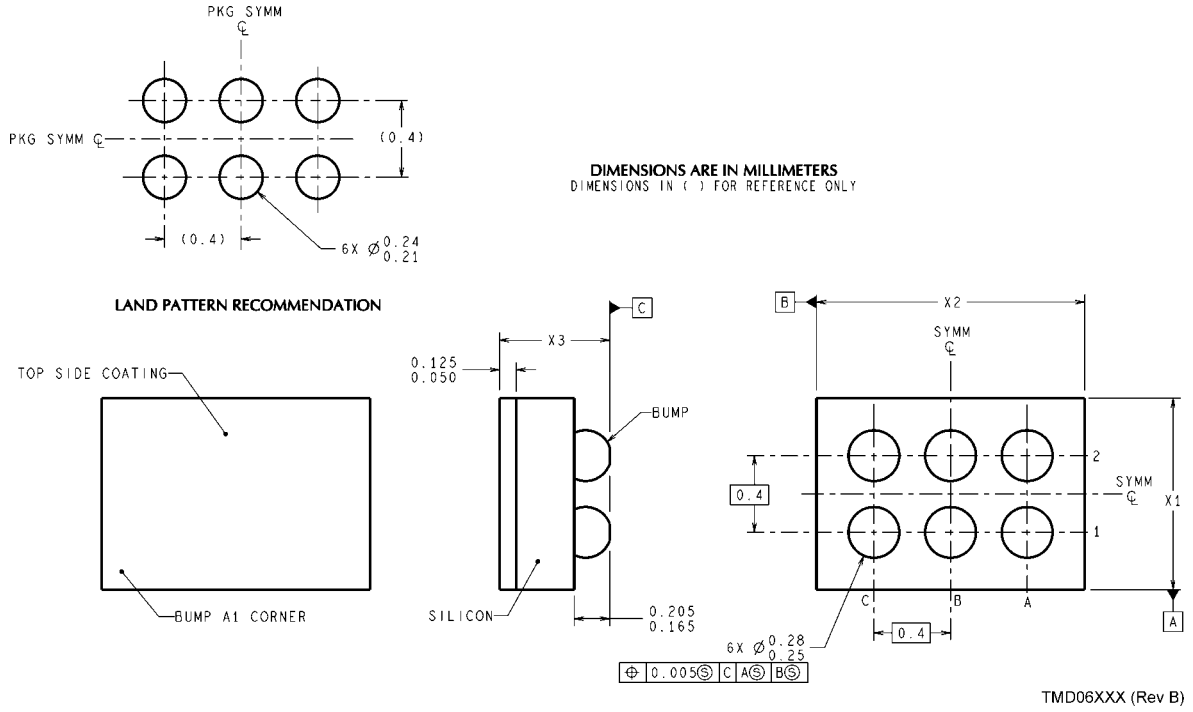
FIGURE 4. LM8801 Board Layout (Top View)

1. Place the LM8801 on 8.26 mil pads. As a thermal relief, connect each pad with a 7 mil wide, approximately 7 mil long trace, and then incrementally increase each trace to its optimal width. The important criterion is symmetry to ensure the solder bumps re-flow evenly (see AN-1112, *Micro SMD Package Assembly and Use*).
2. Place the LM8801, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM8801 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM8801 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pins of the LM8801, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM8801 by giving it a low-impedance ground connection.

5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The voltage feedback trace must remain close to the LM8801 circuit and should be routed directly from FB to V_{OUT} at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
7. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

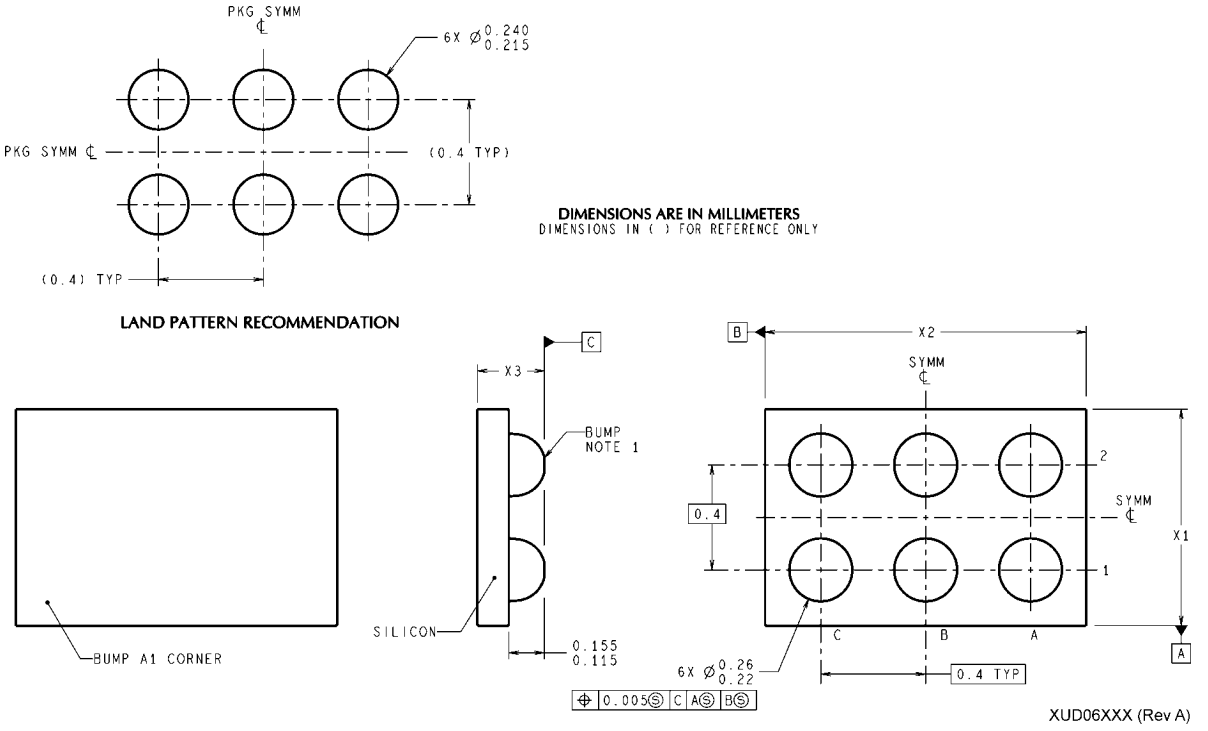
In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

Physical Dimensions inches (millimeters) unless otherwise noted



TMD06XXX (Rev B)

6–bump (Large) micro SMD, 0.4 mm pitch
NS Package Number TMD06LCA
X1 = 1.065 mm ± 0.030 mm
X2 = 1.265 mm ± 0.030 mm
X3 = 0.6 mm ± 0.075 mm
*** Pin A1 is established by lower left corner with respect to text orientation**



6–bump Thin micro SMD, 0.4 mm pitch
NS Package Number XUD06LCA
X1 = 1.065 mm ± 0.030 mm
X2 = 1.265 mm ± 0.030 mm
X3 = 0.25 mm ± 0.045 mm

*** Pin A1 is established by lower left corner with respect to text orientation**

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