LM2984 Microprocessor Power Supply System

Check for Samples: LM2984

FEATURES

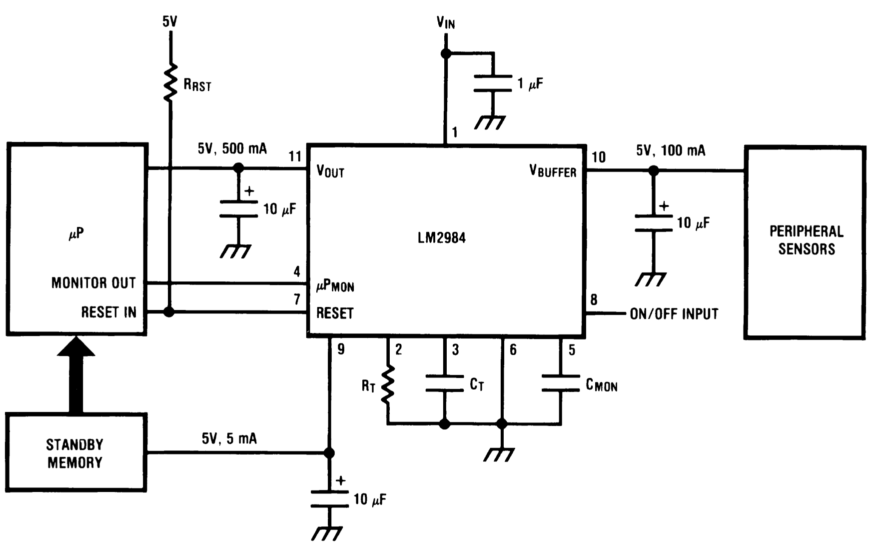
- Three Low Dropout Tracking Regulators
- Output Current in Excess of 500 mA
- Fully Specified for −40°C to +125°C Operation
- Low Quiescent Current Standby Regulator
- Microprocessor Malfunction RESET Flag
- Delayed RESET on Power-Up
- Accurate pretrimmed 5V outputs
- Reverse Battery Protection
- Overvoltage Protection
- Reverse Transient Protection
- Short Circuit Protection
- Internal Thermal Overload Protection
- ON/OFF Switch for High Current Outputs
- P^+ Product Enhancement Tested

DESCRIPTION

The LM2984 positive voltage regulator features three independent and tracking outputs capable of delivering the power for logic circuits, peripheral sensors and standby memory in a typical microprocessor system. The LM2984 includes circuitry which monitors both its own high-current output and also an external μP. If any error conditions are sensed in either, a reset error flag is set and maintained until the malfunction terminates. Since these functions are included in the same package with the three regulators, a great saving in board space can be realized in the typical microprocessor system. The LM2984 also features very low dropout voltages on each of its three regulator outputs (0.6V at the rated output current). Furthermore, the quiescent current can be reduced to 1 mA in the standby mode.

Designed also for vehicular applications, the LM2984 and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. Familiar regulator features such as short circuit and thermal overload protection are also provided. Fixed outputs of 5V are available in the plastic TO-220 power package.

Typical Application Circuit



C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curves.

Figure 1. Package Number NDJ0011B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2]

Input Voltage	
Survival Voltage (<100 ms)	60V
Operational Voltage	26V
Internal Power Dissipation	Internally Limited
Operating Temperature Range (T_A)	−40°C to +125°C
Maximum Junction Temperature	
[3]	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 10 sec.)	230°C
ESD Susceptability [4]	2000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Thermal resistance without a heatsink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 40°C/W.
(4) Human body model, 100 pF capacitor discharged through a 1500Ω resistor.

Electrical Characteristics

V_{IN} = 14V, I_{OUT} = 5 mA, C_{OUT} = 10 µF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C [1] .

Parameter	Conditions	Typical	Limit [2]	Units
V_{OUT} (Pin 11)				
Output Voltage	5 mA ≤ I_O ≤ 500 mA	5.00	4.85/**4.75**	V_{min}
	6V ≤ V_{IN} ≤ 26V		5.15/**5.25**	V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25/**25**	mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50/**50**	mV_{max}
Load Regulation	5 mA ≤ I_{OUT} ≤ 500 mA	12	50/**50**	mV_{max}
Output Impedance	250 mA_{dc} and 10 mA_{rms}, f_o = 120 Hz	24		mΩ
Quiescent Current	I_{OUT} = 500 mA	38	100/**100**	mA_{max}
	I_{OUT} = 250 mA	14	50/**50**	mA_{max}
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 100 mA	100		µV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60/**50**	dB_{min}
Dropout Voltage	I_{OUT} = 500 mA	0.53	0.80/**1.1**	V_{max}
	I_{OUT} = 250 mA	0.28	0.50/**0.70**	V_{max}
Current Limit		0.92	0.75/**0.60**	A_{min}
Maximum Operational Input Voltage	Continuous DC	32	26/**26**	V_{min}
Maximum Line Transient	V_{OUT} ≤ 6V, R_{OUT} = 100Ω, T ≤ 100 ms	65	60/**60**	V_{min}
Reverse Polarity Input Voltage DC	V_{OUT} ≥ −0.6V, R_{OUT} = 100Ω	−30	−15/**−15**	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{OUT} = 100Ω	−55	−35/**−35**	V_{min}

(1) To ensure constant junction temperature, low duty cycle pulse testing is used.
(2) Tested Limits are ensured and 100% production tested.

Electrical Characteristics (continued)

V_{IN} = 14V, I_{OUT} = 5 mA, C_{OUT} = 10 µF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C (1) .

Parameter	Conditions	Typical	Limit (2)	Units
V_{buffer} (Pin 10)				
Output Voltage	5 mA ≤ I_O ≤ 100 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85/**4.75** 5.15/**5.25**	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25/**25**	mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50/**50**	mV_{max}
Load Regulation	5 mA ≤ I_{buf} ≤ 100 mA	15	50/**50**	mV_{max}
Output Impedance	50 mA_{dc} and 10 mA_{rms}, f_O = 120 Hz	200		mΩ
Quiescent Current	I_{buf} = 100 mA	8.0	15/**15**	mA_{max}
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 100 mA	100		µV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60/**50**	dB_{min}
Dropout Voltage	I_{buf} = 100 mA	0.35	0.50/**0.80**	V_{max}
Current Limit		0.23	0.15/**0.15**	A_{min}
Maximum Operational Input Voltage	Continuous DC	32	26/**26**	V_{min}
Maximum Line Transient	V_{buf} ≤ 6V, R_{buf} = 100Ω, T ≤ 100 ms	65	60/**60**	V_{min}
Reverse Polarity Input Voltage DC	V_{buf} ≥ −0.6V, R_{buf} = 100Ω	−30	−15/**−15**	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{buf} = 100Ω	−55	−35/**−35**	V_{min}
$V_{standby}$ (Pin 9)				
Output Voltage	1 mA ≤ I_O ≤ 7.5 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85/**4.75** 5.15/**5.25**	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25/**25**	mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50/**50**	mV_{max}
Load Regulation	0.5 mA ≤ I_{OUT} ≤ 7.5 mA	6	50/**50**	mV_{max}
Output Impedance	5 mA_{dc} and 1 mA_{rms}, f_o = 120 Hz	0.9		Ω
Quiescent Current	I_{stby} = 7.5 mA	1.2	2.0/**4.0**	mA_{max}
	I_{stby} = 2 mA	0.9	1.5/**4.0**	mA_{max}
Output Noise Voltage	10 Hz–100 kHz, I_{stby} = 1 mA	100		µV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60/**50**	dB_{min}
Dropout Voltage	I_{stby} = 1 mA	0.26	0.50/**0.60**	V_{max}
	I_{stby} = 7.5 mA	0.38	0.60/**0.70**	V_{max}
Current Limit		15	12/**12**	mA_{min}
Maximum Operational Input Voltage	4.5V ≤ V_{stby} ≤ 6V, R_{stby} = 1000Ω	65	60/**60**	V_{min}
Maximum Line Transient	V_{stby} ≤ 6V, T ≤ 100 ms, R_{stby} = 1000Ω	65	60/**60**	V_{min}
Reverse Polarity Input Voltage DC	V_{stby} ≥ −0.6V, R_{stby} = 1000Ω	−30	−15/**−15**	V_{min}

Electrical Characteristics (continued)

V_{IN} = 14V, I_{OUT} = 5 mA, C_{OUT} = 10 µF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C (1) .

Parameter	Conditions	Typical	Limit (2)	Units
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{stby} = 1000Ω	−55	−35/**−35**	V_{min}
Tracking and Isolation				
Tracking V_{OUT}–V_{stby}	I_{OUT} ≤ 500 mA, I_{buf} = 5 mA, I_{stby} ≤ 7.5 mA	±30	±100/**±100**	mV_{max}
Tracking V_{buf}–V_{stby}	I_{OUT} = 5 mA, I_{buf} ≤ 100 mA, I_{stby} ≤ 7.5 mA	±30	±100/**±100**	mV_{max}
Tracking V_{OUT}–V_{buf}	I_{OUT} ≤ 500 mA, I_{buf} ≤ 100 mA, I_{stby} = 1 mA	±30	±100/**±100**	mV_{max}
Isolation (3) V_{buf} from V_{OUT}	R_{OUT} = 1Ω, I_{buf} ≤ 100 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}
Isolation (3) V_{stby} from V_{OUT}	R_{OUT} = 1Ω, I_{stby} ≤ 7.5 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}
Isolation (3) V_{OUT} from V_{buf}	R_{buf} = 1Ω, I_{OUT} ≤ 500 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}
Isolation (3) V_{stby} from V_{buf}	R_{buf} = 1Ω, I_{stby} ≤ 7.5 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}
Computer Monitor/Reset Functions				
I_{reset} Low	V_{IN} = 4V, V_{rst} = 0.4V	5	2/**0.50**	mA_{min}
V_{reset} Low	V_{IN} = 4V, I_{rst} = 1 mA	0.10	0.40/**0.40**	V_{max}
R_t voltage	(Pin 2)	1.22	1.15/**0.75**	V_{min}
		1.22	1.30/**2.00**	V_{max}
Power On Reset Delay	VµP$_{mon}$ = 5V	50	45/**17.0**	ms_{min}
	(T_{dly} = 1.2 R_t C_t)	50	55/**80.0**	ms_{max}
ΔV_{OUT} Low Reset Threshold	(4)	−350	−225/**−175**	mV_{min}
			−500/**−550**	mV_{max}
ΔV_{OUT} High Reset Threshold	(4)	600	225/**175**	mV_{min}
			750/**800**	mV_{max}
Reset Output Leakage	VµP$_{mon}$ = 5V, V_{rst} = 12V	0.01	1/**5.0**	$µA_{max}$
µP$_{mon}$ Input Current (Pin 4)	VµP$_{mon}$ = 2.4V	7.5	25/**25**	$µA_{max}$
	VµP$_{mon}$ = 0.4V	0.01	10/**15**	$µA_{max}$
µP$_{mon}$ Input Threshold Voltage		1.22	0.80/**0.80**	V_{min}
		1.22	2.00/**2.00**	V_{max}
µP Monitor Reset Oscillator Period	VµP$_{mon}$ = 0V	50	45/**30**	ms_{min}
	(T_{window} = 0.82 $R_t C_{mon}$)	50	55/**70**	ms_{max}
µP Monitor Reset Oscillator Pulse Width	VµP$_{mon}$ = 0V	1.0	0.7/**0.4**	ms_{min}
	($RESET_{pw}$ = 2000 C_{mon})	1.0	1.3/**2.10**	ms_{max}
Minimum µP Monitor Input Pulse Width	(5)	2		µs

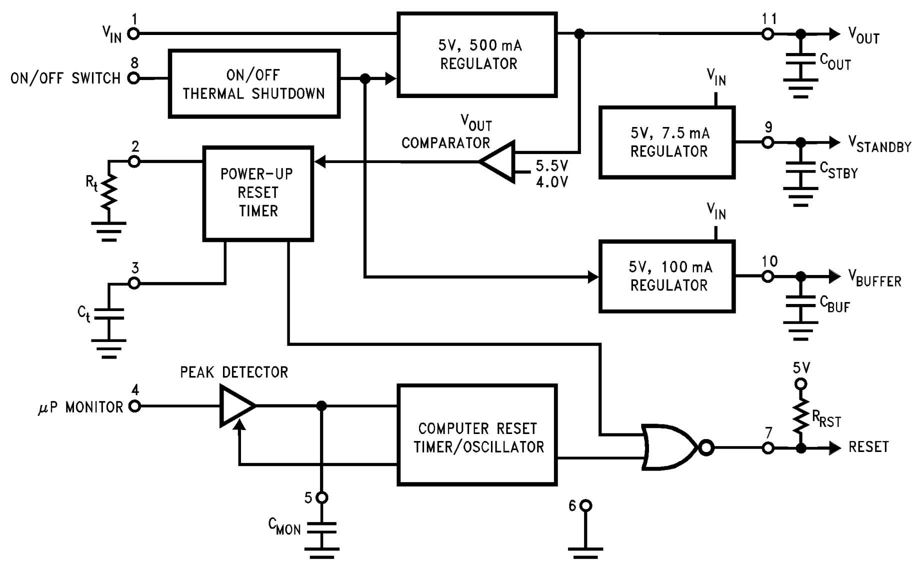
(3) Isolation refers to the ability of the specified output to remain within the tested limits when the other output is shorted to ground.
(4) Internal comparators detect when the main regulator output (V_{OUT}) changes from the measured output voltage (with V_{IN} = 14V) by the specified amount, ΔV_{OUT} High or ΔV_{OUT} Low, and set the Reset Error Flag low. The Reset Error Flag is held low until V_{OUT} returns to regulation. The Reset Error Flag is then allowed to go high again after a delay set by $R_t$and C_t. (see Application Hints section).
(5) This parameter is a measure of how short a pulse can be detected at the µP Monitor Input. This parameter is primarily influenced by the value of C_{mon}. (See Application Hints Section.)

Electrical Characteristics (continued)

V_{IN} = 14V, I_{OUT} = 5 mA, C_{OUT} = 10 µF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C [1] .

Parameter	Conditions	Typical	Limit [2]	Units
Reset Fall Time	R_{rst} = 10k, V_{rst} = 5V, C_{rst} ≤ 10 pF	0.20	1.00/**1.00**	$µs_{max}$
Reset Rise Time	R_{rst} = 10k, V_{rst} = 5V, C_{rst} ≤ 10 pF	0.60	1.00/**1.50**	$µs_{max}$
On/Off Switch Input	V_{ON} = 2.4V	7.5	25/**25**	$µA_{max}$
Current (Pin 8)	V_{ON} = 0.4V	0.01	10/**10**	$µA_{max}$
On/Off Switch Input		1.22	0.80/**0.80**	V_{min}
Threshold Voltage		1.22	2.00/**2.00**	V_{max}

BLOCK DIAGRAM



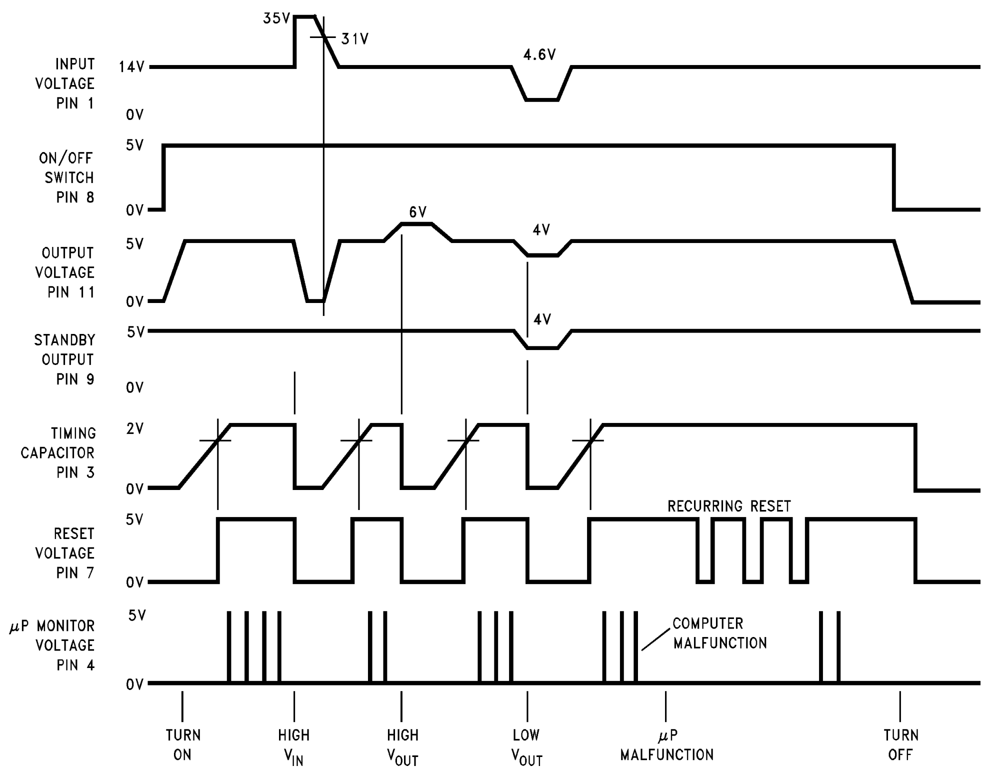
Pin Descriptions

Pin No.	Pin Name	Comments
1	V_{IN}	Positive supply input voltage
2	R_t	Sets internal timing currents
3	C_t	Sets power-up reset delay timing
4	$µP_{mon}$	Microcomputer monitor input
5	C_{mon}	Sets µC monitor timing
6	Ground	Regulator ground
7	Reset	Reset error flag output
8	ON/OFF	Enables/disables high current regulators
9	$V_{standby}$	Standby regulator output (7.5 mA)
10	V_{buffer}	Buffer regulator output (100 mA)
11	V_{OUT}	Main regulator output (500 mA)

External Components

Component	Typical Value	Component Range	Comments
C_{IN}	1 µF	0.47 µF–10 µF	Required if device is located far from power supply filter.
R_t	130k	24k–510k	Sets internal timing currents.
C_t	0.33 µF	0.033 µF–3.3 µF	Sets power-up reset delay.
C_{tc}	0.01 µF	0.001 µF–0.1 µF	Establishes time constant of AC coupled computer monitor.
R_{tc}	10k	1k–100k	Establishes time constant of AC coupled computer monitor. (See Application Hints section.)
C_{mon}	0.47 µF	0.047 µF–4.7 µF	Sets time window for computer monitor. Also determines period and pulse width of computer malfunction reset. (See Application Hints section.)
R_{rst}	10k	5k–100k	Load for open collector reset output. Determined by computer reset input requirements.
C_{stby}	10 µF	10 µF–no bound	A 10 µF is required for stability but larger values can be used to maintain regulation during transient conditions.
C_{buf}	10 µF	10 µF–no bound	A 10 µF is required for stability but larger values can be used to maintain regulation during transient conditions.
C_{OUT}	10 µF	10 µF–no bound	A 10 µF is required for stability but larger values can be used to maintain regulation during transient conditions.

Typical Circuit Waveforms



Connection Diagram

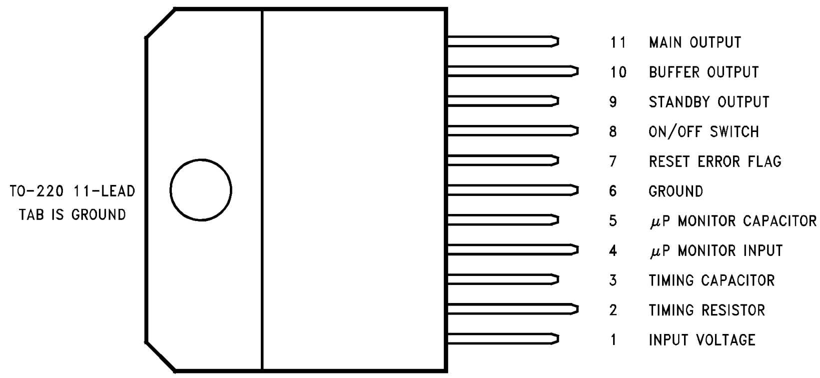


Figure 2. Package Number NDJ0011B

Typical Performance Characteristics

Dropout Voltage (V_{OUT})

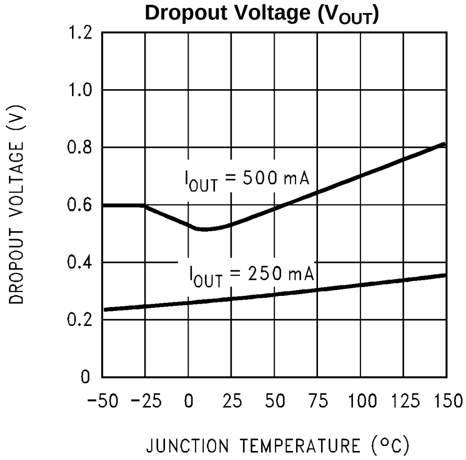


Figure 3.

Dropout Voltage (V_{buf})

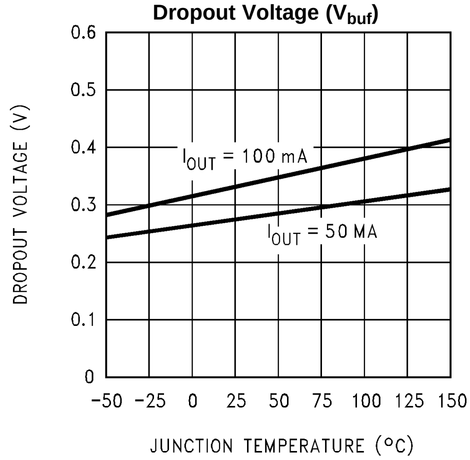


Figure 4.

Dropout Voltage (V_{stby})

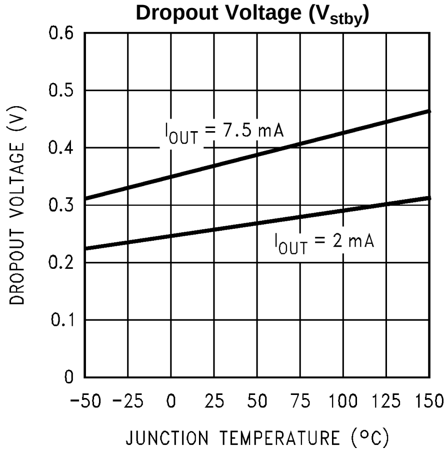


Figure 5.

Dropout Voltage (V_{OUT})

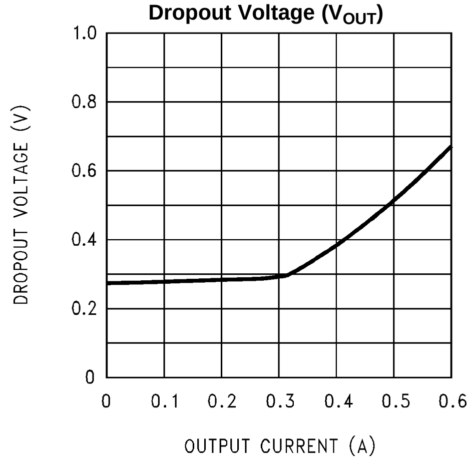


Figure 6.

Dropout Voltage (V_{buf})

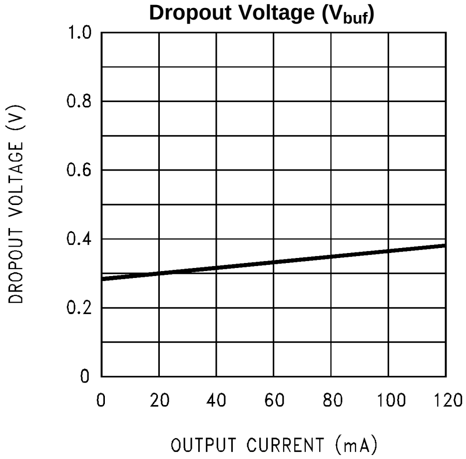


Figure 7.

Dropout Voltage (V_{stby})

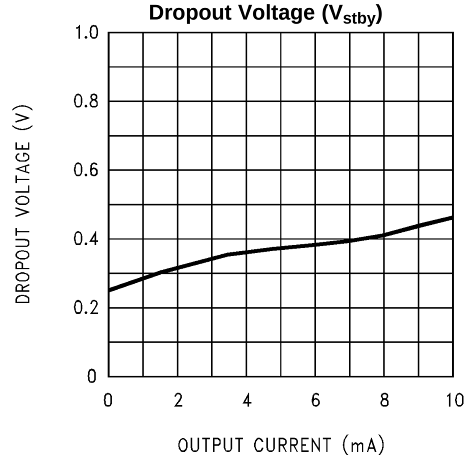


Figure 8.

Typical Performance Characteristics (continued)

Peak Output Current (V_{OUT})

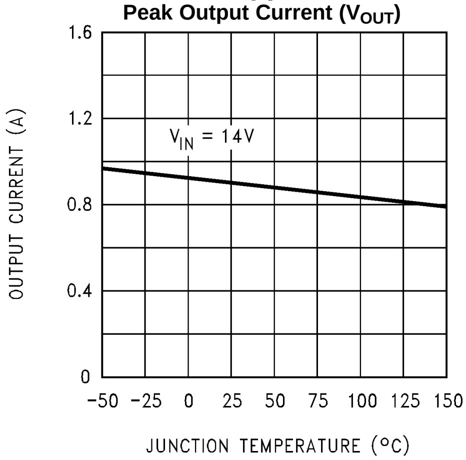


Figure 9.

Peak Output Current (V_{buf})

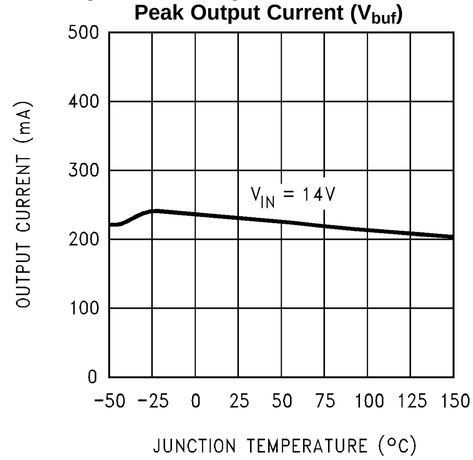


Figure 10.

Peak Output Current (V_{stby})

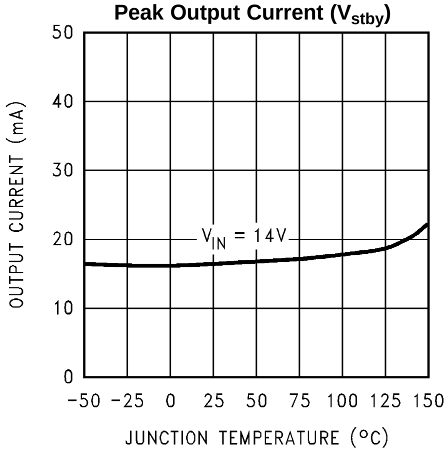


Figure 11.

Quiescent Current (V_{OUT})

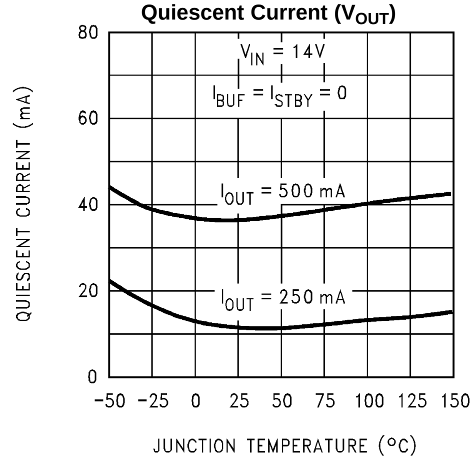


Figure 12.

Quiescent Current (V_{buf})

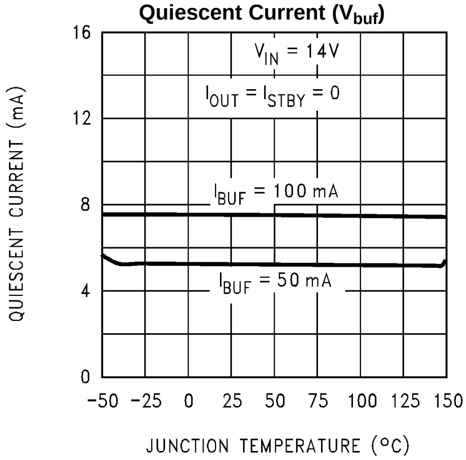


Figure 13.

Quiescent Current (V_{stby})

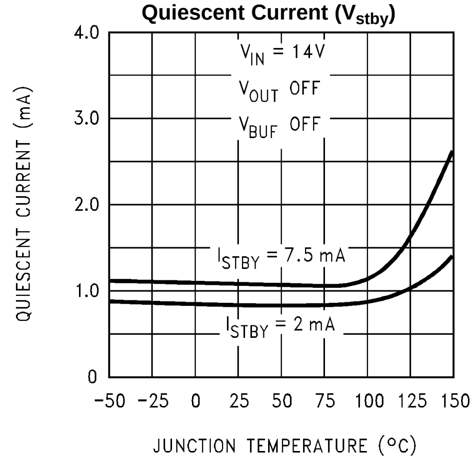


Figure 14.

Typical Performance Characteristics (continued)

Quiescent Current (V_{OUT})

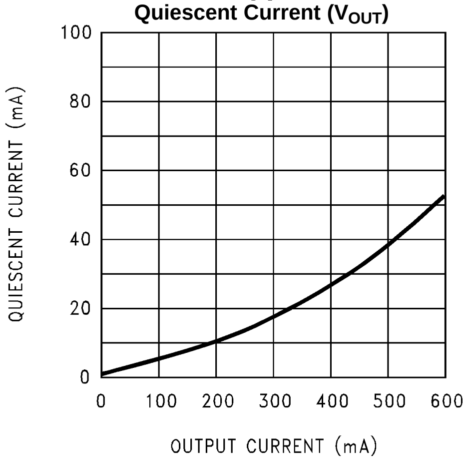


Figure 15.

Quiescent Current (V_{buf})

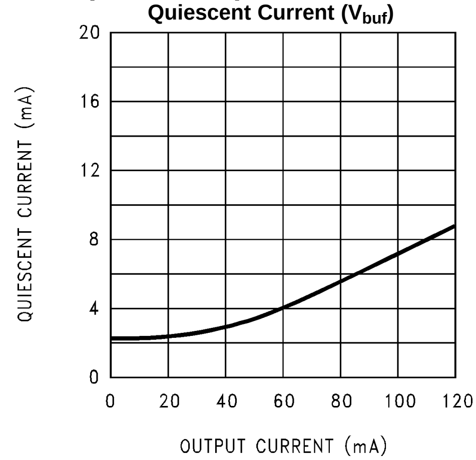


Figure 16.

Quiescent Current (V_{stby})

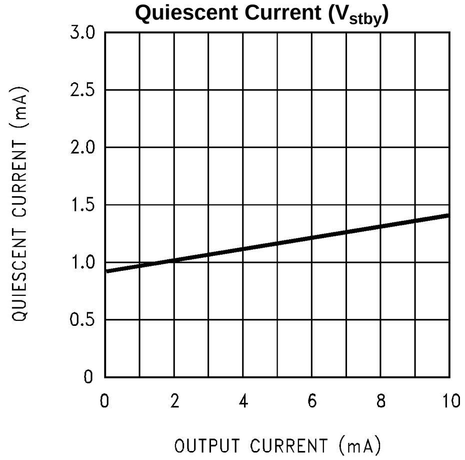


Figure 17.

Quiescent Current (V_{OUT})

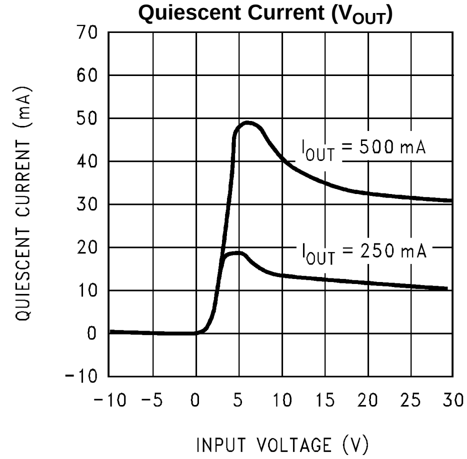


Figure 18.

Quiescent Current (V_{buf})

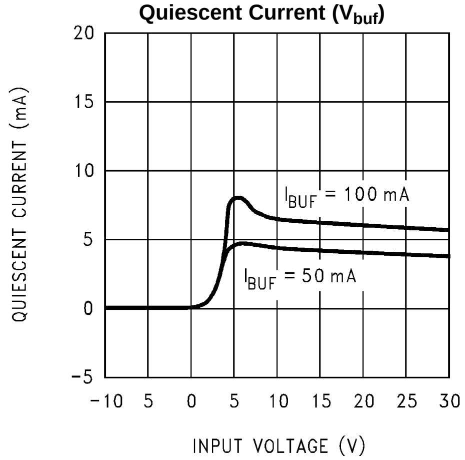


Figure 19.

Quiescent Current (V_{stby})

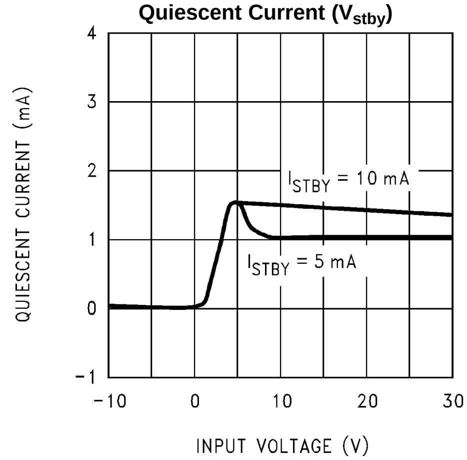


Figure 20.

Typical Performance Characteristics (continued)

Output Voltage (V_{OUT})

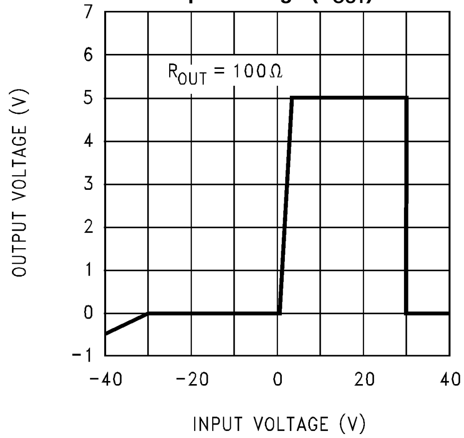


Figure 21.

Output Voltage (V_{buf})

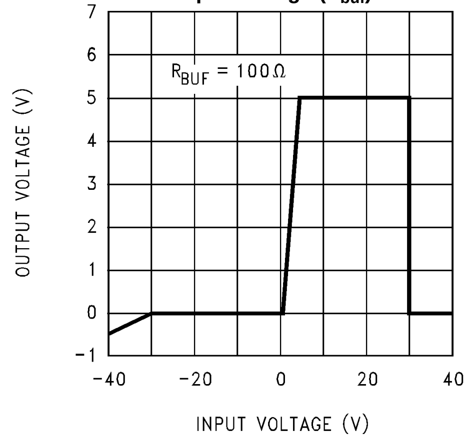


Figure 22.

Output Voltage (V_{stby})

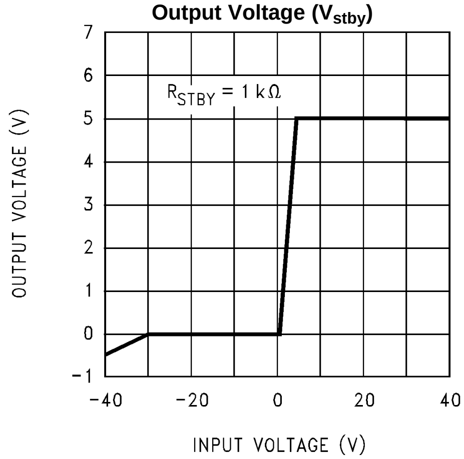


Figure 23.

Low Voltage Behavior (V_{OUT})

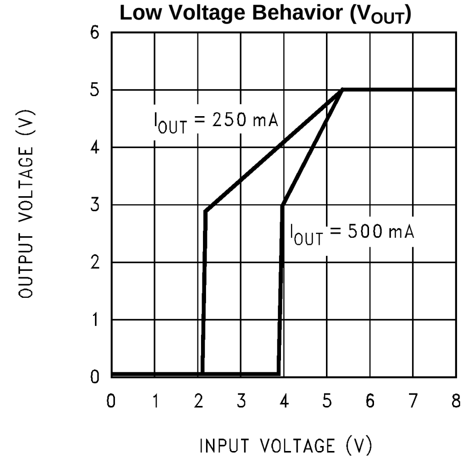


Figure 24.

Low Voltage Behavior (V_{buf})

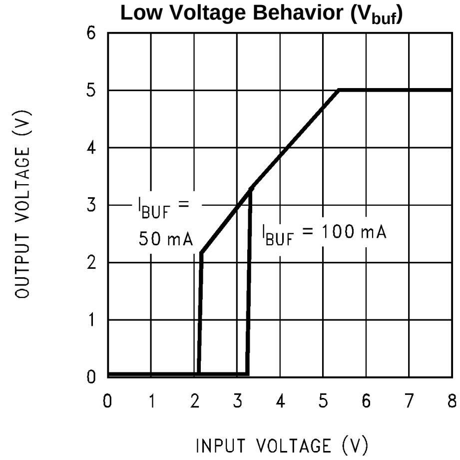


Figure 25.

Low Voltage Behavior (V_{stby})

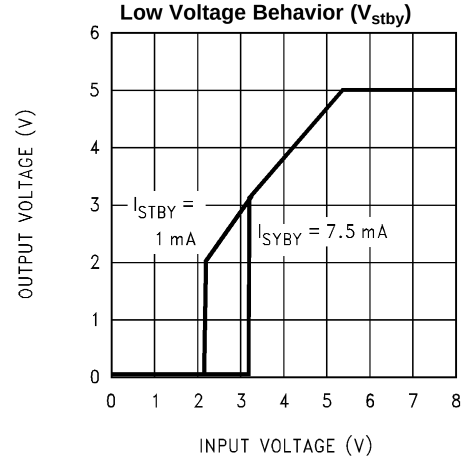


Figure 26.

Typical Performance Characteristics (continued)

Line Transient Response (V_{OUT})

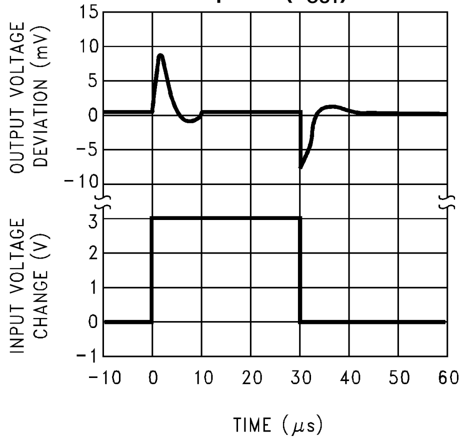


Figure 27.

Line Transient Response (V_{buf})

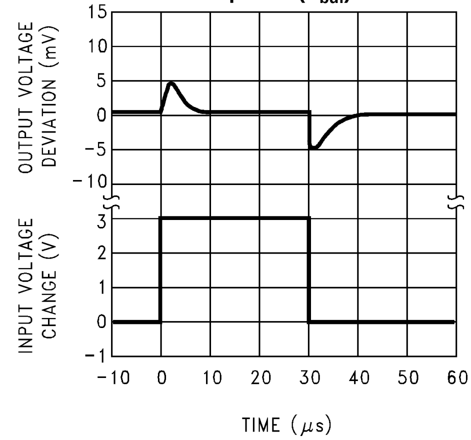


Figure 28.

Line Transient Response (V_{stby})

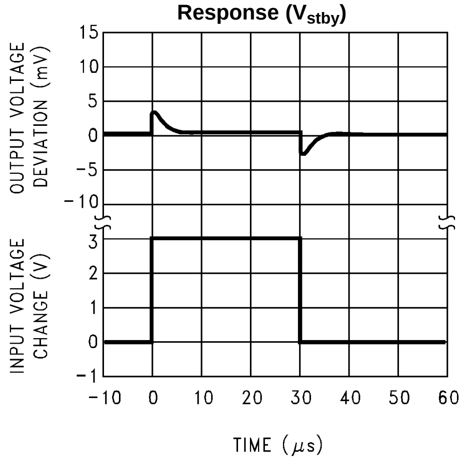


Figure 29.

Load Transient Response (V_{OUT})

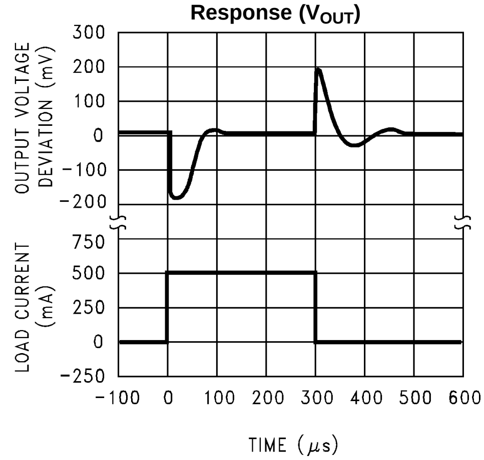


Figure 30.

Load Transient Response (V_{buf})

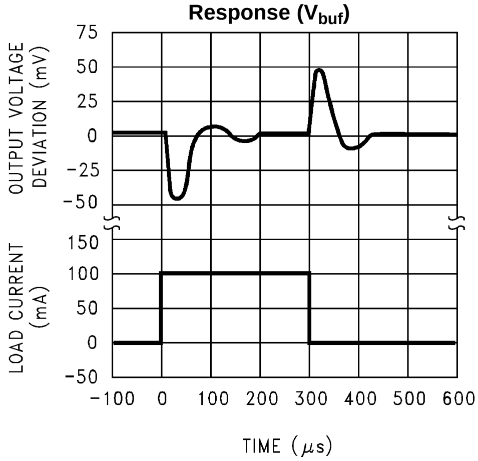


Figure 31.

Load Transient Response (V_{stby})

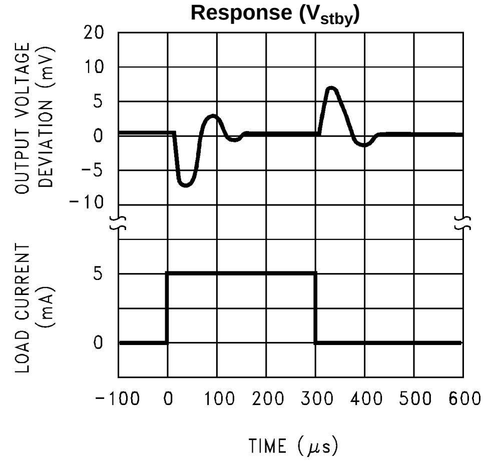


Figure 32.

Typical Performance Characteristics (continued)

Output Impedance (V_{OUT})

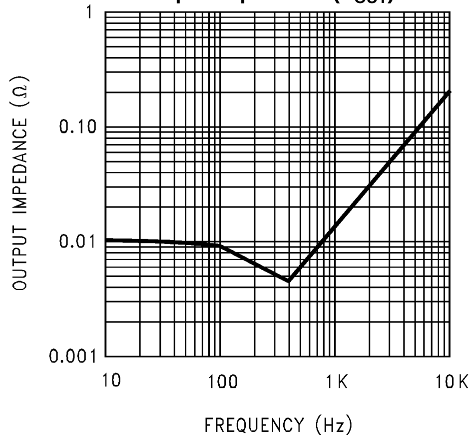


Figure 33.

Output Impedance (V_{buf})

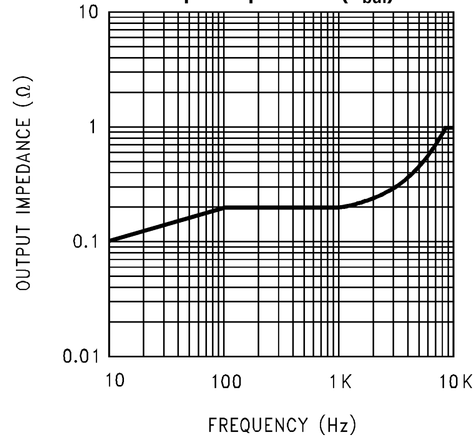


Figure 34.

Output Impedance (V_{stby})

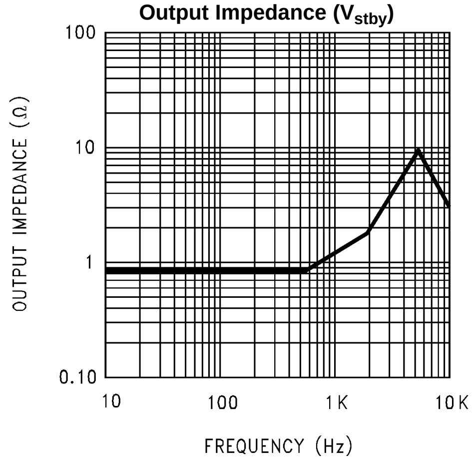


Figure 35.

Ripple Rejection (V_{OUT})

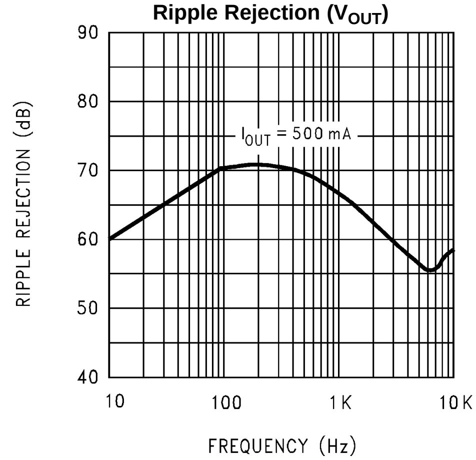


Figure 36.

Ripple Rejection (V_{buf})

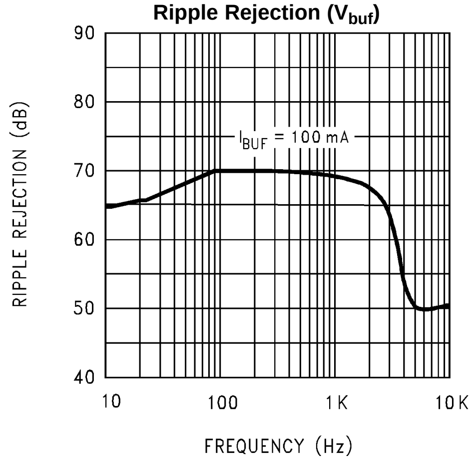


Figure 37.

Ripple Rejection (V_{stby})

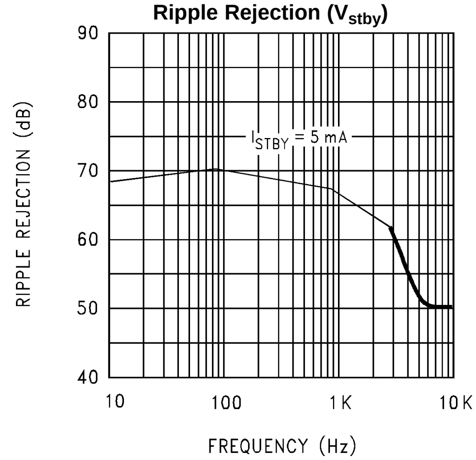


Figure 38.

Typical Performance Characteristics (continued)

Output Voltage

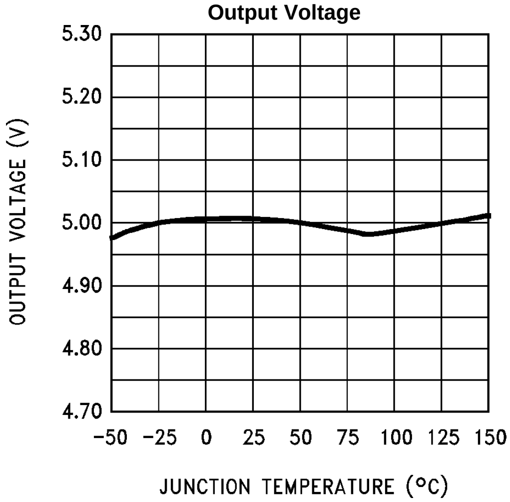


Figure 39.

Device Dissipation vs Ambient Temperature

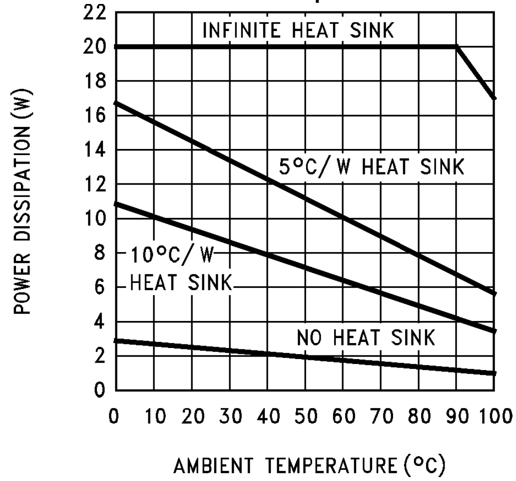


Figure 40.

Output Capacitor ESR (Standby Output, Pin 9)

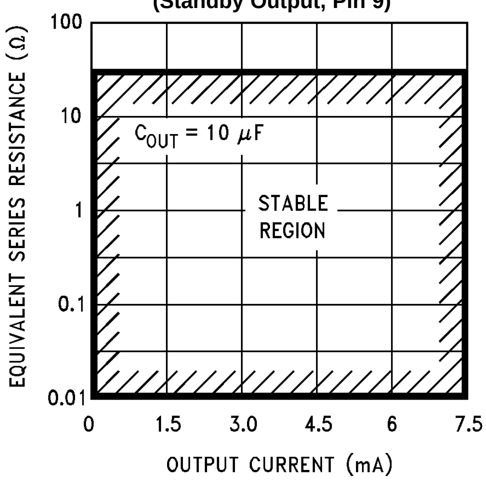


Figure 41.

Output Capacitor ESR (Buffer Output, Pin 10)

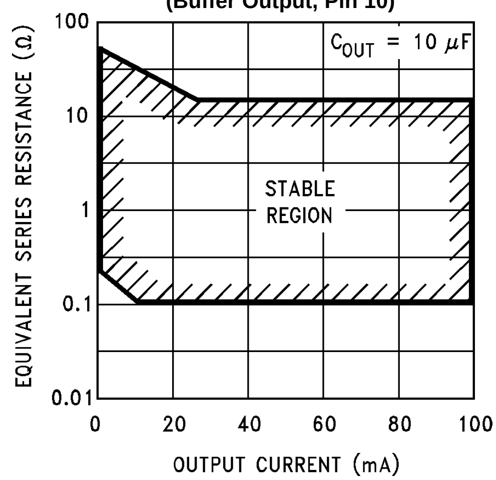


Figure 42.

Output Capacitor ESR (Main Output, Pin 11)

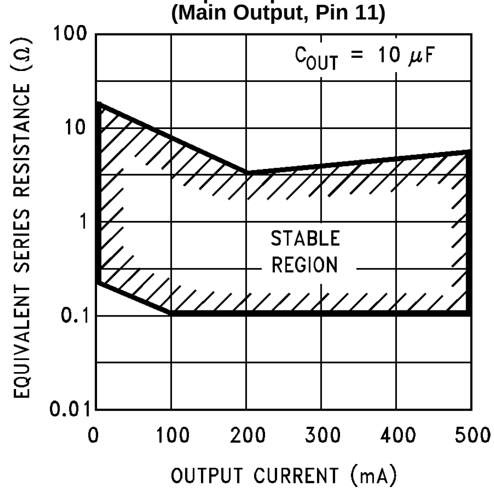


Figure 43.

APPLICATION HINTS

OUTPUT CAPACITORS

The LM2984 output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10 µF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also affects the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst case is usually determined at the minimum ambient temperature and the maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

Each output **must** be terminated by a capacitor, even if it is not used.

STANDBY OUTPUT

The standby output is intended for use in systems requiring standby memory circuits. While the high current regulator outputs are controlled with the ON/OFF pin described later, the standby output remains on under all conditions as long as sufficient input voltage is supplied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<1.5 mA) when the other regulator outputs are off.

The capacitor on the output of this regulator can be increased without bound. This will help maintain the output voltage during negative input transients and will also help to reduce the noise on all three outputs. Because the other two track the standby output: therefore any noise reduction here will also reduce the other two noise voltages.

BUFFER OUTPUT

The buffer output is designed to drive peripheral sensor circuitry in a µP system. It will track the standby and main regulator within a few millivolts in normal operation. Therefore, a peripheral sensor can be powered off this supply and have the same operating voltage as the µP system. This is important if a ratiometric sensor system is being used.

The buffer output can be short circuited while the other two outputs are in normal operation. This protects the µP system from disruption of power when a sensor wire, etc. is temporarily shorted to ground, i.e. only the sensor signal would be interrupted, while the µP and memory circuits would remain operational.

The buffer output is similar to the main output in that it is controlled by the ON/OFF switch in order to save power in the standby mode. It is also fault protected against overvoltage and thermal overload. If the input voltage rises above approximately 30V (e.g. load dump), this output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is necessary since this output is one of the dominant sources of power dissipation in the IC.

MAIN OUTPUT

The main output is designed to power relatively large loads, i.e. approximately 500 mA. It is therefore also protected against overvoltage and thermal overload.

This output will track the other two within a few millivolts in normal operation. It can therefore be used as a reference voltage for any signal derived from circuitry powered off the standby or buffer outputs. This is important in a ratiometric sensor system or any system requiring accurate matching of power supply voltages.

ON/OFF SWITCH

The ON/OFF switch controls the main output and the buffer output. The threshold voltage is compatible with most logic families and has about 20 mV of hysteresis to insure “clean” switching from the standby mode to the active mode and vice versa. This pin can be tied to the input voltage through a 10 kΩ resistor if the regulator is to be powered continuously.

POWER DOWN OVERRIDE

Another possible approach is to use a diode in series with the ON/OFF signal and another in series with the main output in order to maintain power for some period of time after the ON/OFF signal has been removed (see Figure 44). When the ON/OFF switch is initially pulled high through diode D1, the main output will turn on and supply power through diode D2 to the ON/OFF switch effectively latching the main output. An open collector transistor Q1 is connected to the ON/OFF pin along with the two diodes and forces the regulators off after a period of time determined by the µP. In this way, the µP can override a power down command and store data, do housekeeping, etc. before reverting back to the standby mode.

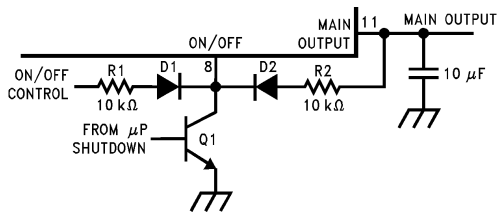


Figure 44. Power Down Override

RESET OUTPUT

This output is an open collector NPN transistor which is forced low whenever an error condition is present at the main output or when a µP error is sensed (see µP MONITOR RESET section). If the main output voltage drops by 350 mV or rises out of regulation by 600 mV typically, the RESET output is forced low and held low for a period of time set by two external components, R_t and C_t. There is a slight amount of hysteresis in these two threshold voltages so that the RESET output has a fast rise and fall time compatible with the requirements of most µP RESET inputs.

DELAYED RESET

Resistor R_t and capacitor C_t set the period of time that the RESET output is held low after a main output error condition has been sensed. The delay is given by the formula:

$$T_{dly} = 1.2\ R_t C_t \text{ (seconds)} \quad (1)$$

The delayed RESET will be initiated any time the main output is out of regulation, i.e. during power-up, short circuit, overvoltage, low line, thermal shutdown or power-down. The µP is therefore RESET whenever the output voltage is out of regulation. (It is important to note that a RESET is only initiated when the main output is in error. The buffer and standby outputs are not directly monitored for error conditions.)

µP MONITOR RESET

There are two distinct and independent error monitoring systems in the LM2984. The one described above monitors the main regulator output and initiates a delayed RESET whenever this output is in error. The other error monitoring system is the µP watchdog. These two systems are OR'd together internally and both force the RESET output low when either type of error occurs.

This watchdog circuitry continuously monitors a pin on the µP that generates a positive going pulse during normal operation. The period of this pulse is typically on the order of milliseconds and the pulse width is typically on the order of 10's of microseconds. If this pulse ever disappears, the watchdog circuitry will time out and a RESET low will be sent to the µP. The time out period is determined by two external components, R_t and C_{mon}, according to the formula:

$$T_{window} = 0.82\ R_t C_{mon} \text{ (seconds)} \quad (2)$$

The width of the RESET pulse is set by C_{mon} and an internal resistor according to the following:

$$RESET_{pw} = 2000\ C_{mon}\ (seconds) \tag{3}$$

A square wave signal can also be monitored for errors by filtering the C_{mon} input such that only the positive edges of the signal are detected. Figure 45 is a schematic diagram of a typical circuit used to differentiate the input signal. Resistor R_{tc} and capacitor C_{tc} pass only the rising edge of the square wave and create a short positive pulse suitable for the µP monitor input. If the incoming signal continues in a high state or in a low state for too long a period of time, a RESET low will be generated.

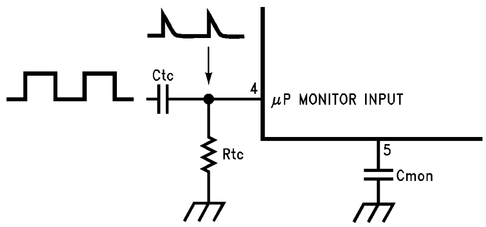


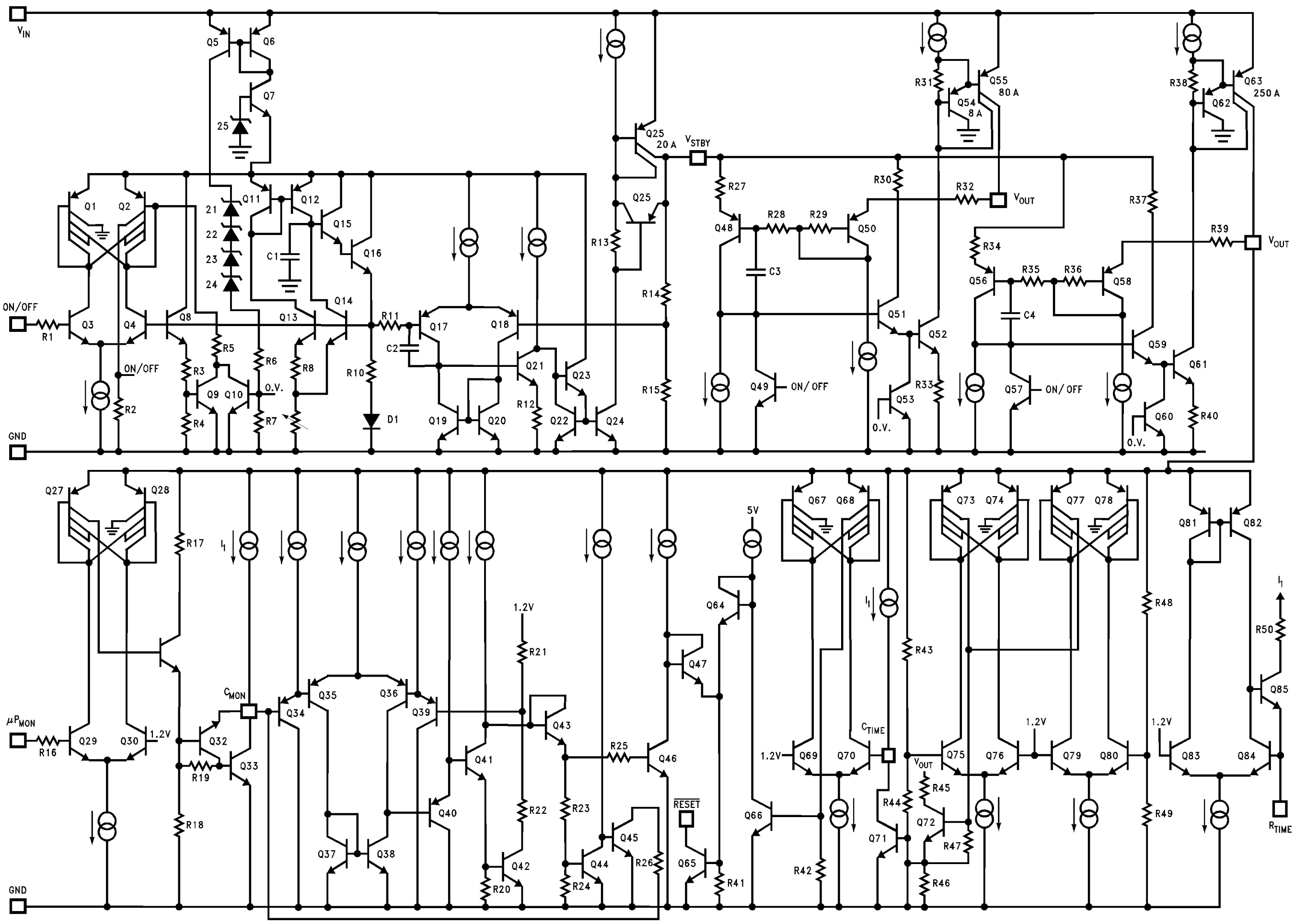
Figure 45. Monitoring Square Wave µP Signals

The threshold voltage and input characteristics of this pin are compatible with nearly all logic families.

There is a limit on the width of a pulse that can be reliably detected by the watchdog circuit. This is due to the output resistance of the transistor which discharges C_{mon} when a high state is detected at the input. The minimum detectable pulse width can be determined by the following formula:

$$PW_{min} = 20\ C_{mon}\ (seconds) \tag{4}$$

Equivalent Schematic Diagram



REVISION HISTORY

Changes from Revision B (March 2013) to Revision C **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2984T	ACTIVE	TO-220	NDJ	11	20	TBD	Call TI	Call TI	-40 to 125	LM2984T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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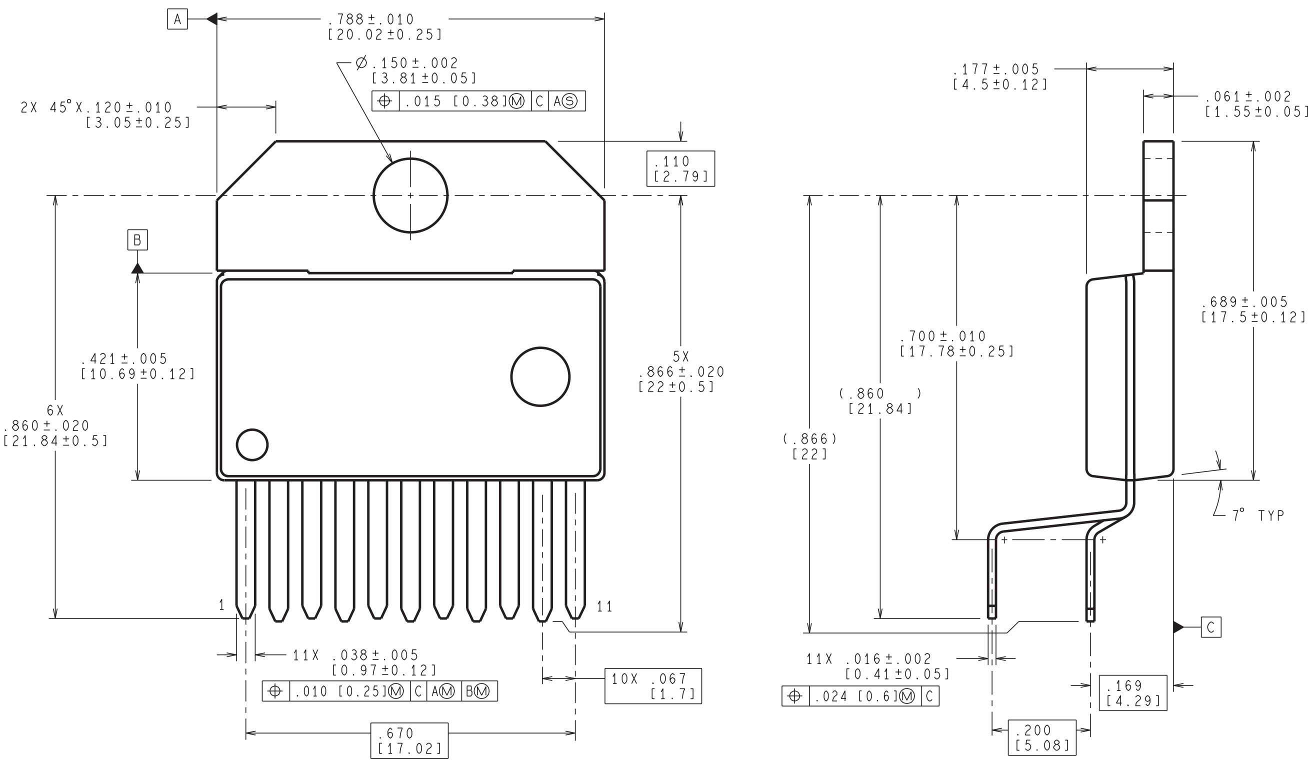

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