GC5328 Low-Power Wideband Digital Predistortion Transmit Processor

Check for Samples: GC5328

FEATURES

- **Integrated DUC, CFR, and DPD Solution**
- **20-MHz Max. Signal Bandwidth, Based on Max. DPD Clock of 200 Mhz, Fifth-Order Correction**
- **DUC: Up to 12 CDMA2000/TDSCDMA, 4 W-CDMA, 2–10 MHz or 1–20 MHz OFDMA Carriers**
- **CFR: Typically Meets 3GPP TS 25.141 < 6.5 dB PAR, < 8.5 dB PAR for OFDMA Signals**
- **DPD: Short-Term Memory Compensation, Typical ACLR Improvement > 20 dB**
- **GC5328IZER PBGA Package, 23 mm × 23 mm**
- **1.2-V Core, 1.8-V HSTL, 3.3-V I/O**
- **2.5-W Typical Power Consumption**
- **TMS320C6727 DPD Optimization Software**
- **Supports Direct Interface to TI High-Speed Data Converters**

APPLICATIONS

- **3 GPP (W-CDMA) Base Stations**
- **3 GPP2 (CDMA2000) Base Stations**
- **WiMAX, WiBRO, and LTE (OFDMA) Base Stations**
- **Multicarrier Power Amplifiers (MCPAs)**

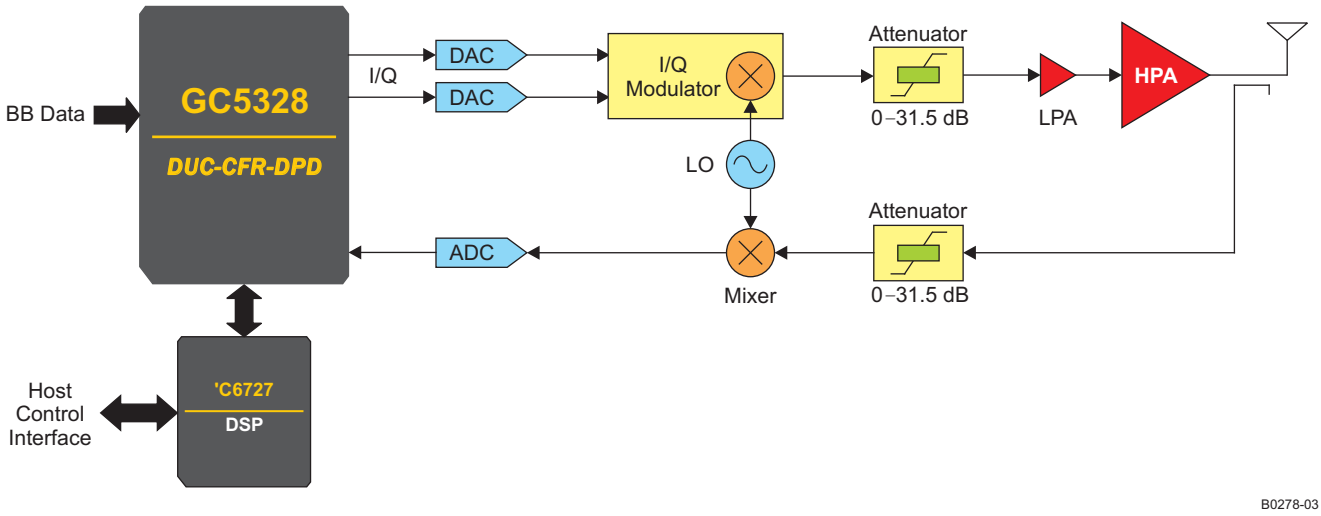


Figure 1. GC5328 System Block Diagram

DESCRIPTION

The GC5328 is a lower-power version of the GC5322 wideband digital predistortion transmit processor. The GC5328 includes a digital upconverter (DUC) block, a crest factor reduction (CFR) block, a digital predistortion (DPD) block, feedback (FB) block, and capture buffer (CB) blocks.

The GC5328 GPP block receives the interleaved IQ data from the baseband input. The individual IQ channels are gain-adjusted in the GPP and routed to the DUC. The GPP and DUC can be bypassed to input a combined IQ signal. The DUC provides three stages of interpolation and a complex mixer. There are two DUC blocks. The output from the DUC blocks is combined in the sum chain. Each of the 1 to 12 DUC channels can be summed, and the composite signal can be scaled.

The CFR block has four serial stages of peak detection and cancellation. The CFR block cancellation filter can be programmed as real or complex. The CFR peak-reduced output is routed to the Farrow resampler. The Farrow resampler resamples the CFR output to the DPD clock rate. The Farrow resampler block also has a complex mixer for composite carrier frequency offset.

The DPD subsystem has a circular limiter, nonlinear DPD correction, and a transmit equalizer. The DPD correction can reduce the follow-on circuitry distortion products. The DPD output is sent to the BUC. The BUC provides a post-DPD interpolation, and also provides a complex mixer for frequency offset. The DAC interface converts the BUC signal output to the interleaved IQ or parallel IQ output signals for the DAC5682Z or DAC5688.

The CB block captures the selected internal reference signal, and the feedback block in two up to 4K capture buffers. The signal capture can be based on an externally timed event (standard capture buffer), delay after a timed event, or signal statistics (smart capture buffer). Normally the DPD input and feedback output are selected. The capture buffers are stored and read by the microprocessor.

The FB block receives the LVDS ADC information and performs signal processing to downconvert the received signal to 0IF. The FB block also has a feedback-path receive equalizer.

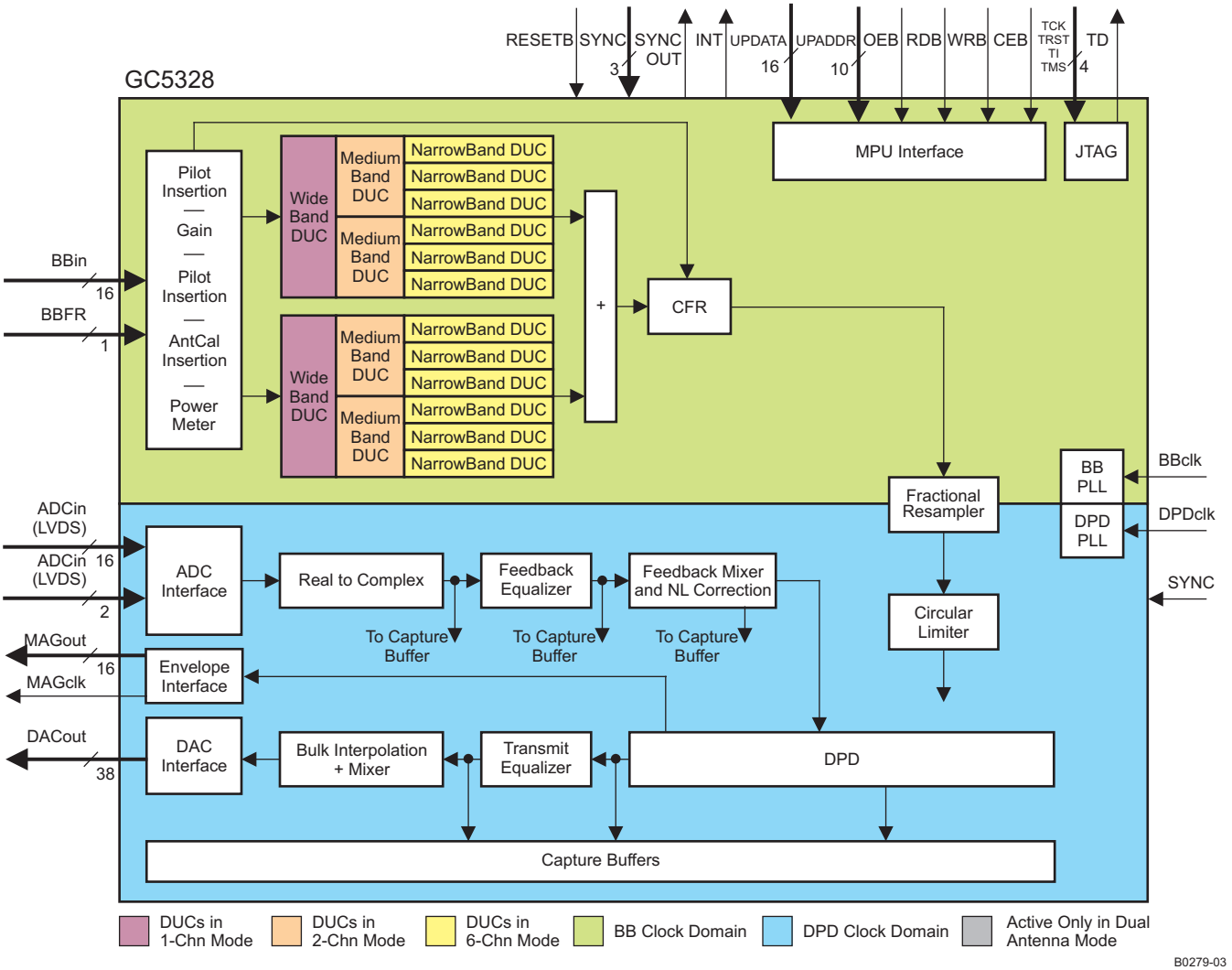


Figure 2. GC5328 Functional Block Diagram

AVAILABLE OPTIONS

T_C	PACKAGED DEVICE
	484-Ball PBGA Package, 23 mm × 23 mm
–40°C to 85°C	GC5328IZER

REFERENCES

1. GC532x Architecture Datasheet (NDA, obtain through local TI field application engineer)
2. GC5328 EVM User Guide, Schematic Diagram (obtain through local TI field application engineer)
3. GC5325 EVM User Guide, Schematic Diagram TI Web site under GC5325
4. GC5322 DPD Host Interface Guide (obtain through local TI Field Application Engineer)
5. GC5328 configuration (obtain through local TI Field Application Engineer)
6. DSP – TMS320C672x DSP Universal Host Port Interface Reference Guide (SPRU719)
7. DSP – TMS320C672x DSP External Memory Interface (EMIF) User's Guide (SPRU711)

GC5328 INTRODUCTION

The GC5328 is a flexible transmit sector processor that includes a digital upconverter (DUC) block, a crest factor reduction (CFR) block, and a digital predistortion (DPD) block and its associated feedback chain. The GC5328 processes composite input bandwidths of up to 20 MHz and processes DPD expansion bandwidths of up to 100 MHz. By reducing both the peak-to-average ratio (PAR) of the input signals using the CFR block and linearizing the power amplifier (PA) using the DPD block, the GC5328 reduces the costs of multicarrier PAs (MCPA) for wireless infrastructure applications. The GC5328 applies CFR and DPD while a separate microprocessor (a Texas Instruments TMS320C6727 DSP) is used to optimize performance levels and maintain target PA performance levels.

By including the GC5328 in their system architecture, manufacturers of BTS equipment can realize significant savings on power amplifier bill of materials (BOM) and overall operational costs due to the PA efficiency improvement. The GC5328 meets multicarrier 3G performance standards (PCDE, composite EVM, and ACLR) at PAR levels down to 6.5 dB and improves the ACLR, at the PA output, by 20 dB or more. The GC5328 integrates easily into the transmit signal chain between baseband processors (such as the Texas Instruments TMS320C64x™ DSP family) and TI high-performance data converters.

A typical GC5328 system application would include the following transmit-chain components:

- TMS320C6727B digital signal processor (DSP)
- DAC5682 16-bit, 1-Gsps DAC; DAC5688 16-bit, 800-Msps DAC (transmit path)
- CDCM7005, CDCE72010 clock generator
- TRF3761 integrated VCO/PLL synthesizer
- TRF3703 quadrature modulator
- ADS6149 14-bit, 250-Msps ADC or ADS5517 11-bit 200-Msps (feedback path)
- AMC7823 analog monitoring and control circuit with GPIO and SPI

BASEBAND INTERFACE

The GC5328 baseband interface block accepts baseband signals over an interleaved parallel interface at a data rate of up to 70 MHz. The input interface supports up to 12 separate baseband carriers. The baseband interface sends the interleaved IQ data to the DUC, or in DUC bypass to the sum chain, with up to 35-Mhz composite BW. The baseband interface has 18-bit data (top16) BBData[15.0], BBFrame, and two additional (bottom two data) MFIO(18,19).

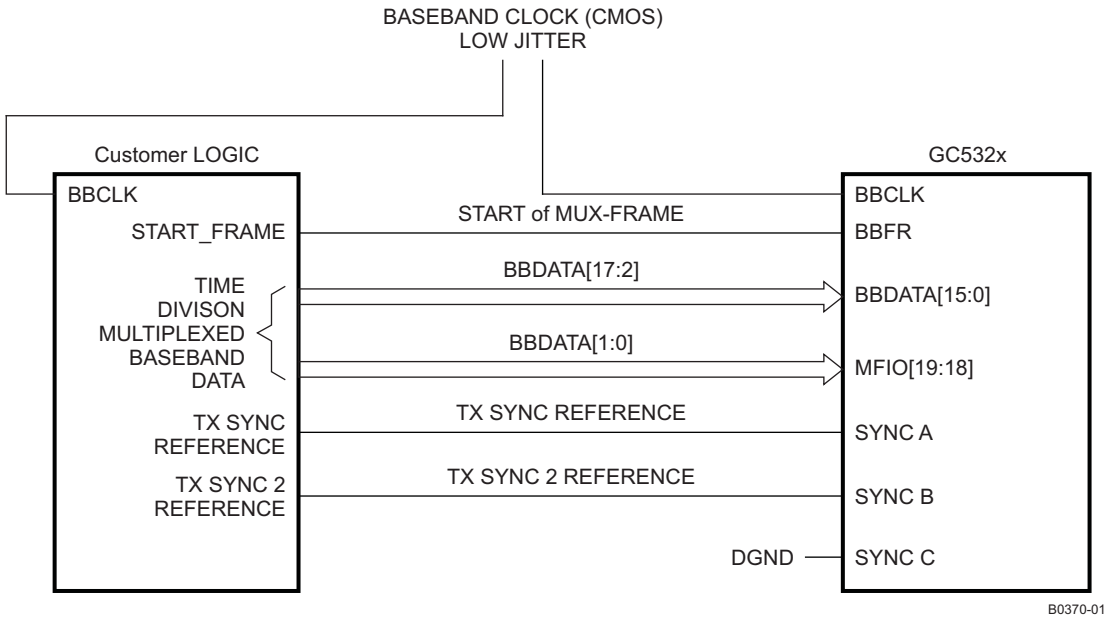


Figure 3. Baseband and Sync Interface to GC5328

BASEBAND CLOCK INPUT

The baseband clock input is a CMOS, low-jitter clock.

GAIN/PILOT INSERTION/AntCal INSERTION/POWER METER

Baseband gain can be applied on a per-carrier basis to control the individual channel power accurately through the system. A UMTS pilot sequence at a programmable gain can be added for antenna calibration. Each individual baseband channel has an integrated $I^2 + Q^2$ power accumulator. The baseband power meters have a common integration counter and interval counter for all channels. The GPP block has an IPDL detection and control section to select one of four CFR memories when IPDL autoselection is used. Normally, IPDL 0 is manually selected.

DIGITAL UPCONVERTERS (DUCs)

The GC5328 DUC block has interpolation filters, programmable delays, and complex mixers for each channel. There are two DUC blocks within the GC5328. The sum chain after the DUC channel combines the DUC channel streams or the bypass stream and sends the data to the CFR block. Each DUC can operate in one wide, two medium, or six CDMA channels. Each DUC has a PFIR for spectral shaping, a CFIR for interpolation and image rejection, and a bulk interpolation CIC.

The 2 DUCs can support:

- (6 channel/DUC mode) up to 12 – 1.23(8) Mhz CDMA, 1xEVDO, or TDSCDMA carriers
- (2 channel/DUC mode) up to 4 – WCDMA or LTE-5 carriers
- (1 channel/DUC mode) up to 2 – Wibro, Wimax, LTE 10 carriers
- (1 channel/DUC mode) 1 – Wimax or LTE20 carrier

Users can specify the filter characteristics of the DUC. The filters are the programmable finite impulse response (PFIR), compensating finite impulse response (CFIR), and cascade integrator comb (CIC) filters. Users can also specify the center frequencies of each carrier with a resolution of 0.25 mHz. Additional controls available in the DUCs include bulk and fractional-time delay adjustments, phase adjustments, and equalization. The maximum DUC output bandwidth is 40 MHz.

CREST FACTOR REDUCTION (CFR)

The GC5328 CFR block selectively reduces the peak-to-average ratio (PAR) of wideband digital signals. There are four peak detection cancellation sections in series in the CFR block. Each stage compares the estimated peak at the stage input with the target, and subtracts a scaled cancellation peak from the signal. There are 24 cancellers pooled among the four stages. The CFR interpolation filter must have at least 1.6× bandwidth, typical is 2× BBClock to signal bandwidth.

There are four canceller memories and an update shadow memory that can be used for the auto-IPDL UMTS select cancellation filter. The shadow memory allows the user to update one of the four filter banks during operation. The CFR block has a composite RMS meter that can select the CFR input or output for monitoring.

The CFR block for WCDMA reduces TM1, TM3 signals for four adjacent carriers to 6.5 db PAR within the 3GPP limit. The Wimax 10 reduction for two adjacent carriers is to 8.5 db PAR. TDSCDMA and CDMA performance is limited by the carrier allocations and carrier coding.The CFR processing complex BW is limited to 62.5% of the baseband clock rate.

FRACTIONAL FARROW RESAMPLER (FR)

The fractional resampler block takes the peak-reduced composite signals from CFR and resamples this through fractional interpolation to the DPD processing rate. The user-programmable Farrow resampler supports upsampling rates from 1× to 64×, with 16-bit precision on the interpolation ratio. After the fractional interpolation, a complex mixer is available to provide a composite carrier IF offset frequency. A peak I or Q monitor is provided.

DIGITAL PREDISTORTION (DPD)

The DPD block provides predistortion for up to Nth-order nonlinearities, and can correct multiple orders and lengths of PA memory effects. The circular hard limiter provides a circular clipper that limits the magnitude-squared value to –6 dbFS. This is optimized for hardware, and for the allowed gain expansion in the nonlinear DPD correction.

The DPD has an RMS power meter, and a peak I or Q monitor.

The predistortion is performed for the nonlinear correction in the DPD section. The linear correction is performed in the Tx equalizer. The predistortion correction terms are computed by an external processor (TMS320C6727 DSP) based on capture buffer information and the DPD software.

The DSP sets up the condition for collecting capture buffer data, retrieves the captured data over the EMIF bus, and then performs calculations to compute the error and corrections to be used for the transmit path.

The host interface controls the mode of operation of the software in the TI DSP. TI provides a base delivery of 'C6727 software to GC5328 customers that achieves a typical ACLR improvement of 20 dB or more when compared to a PA without DPD.

DPD CLOCK INPUT

The DPD clock input is an LVDS, low-jitter clock.

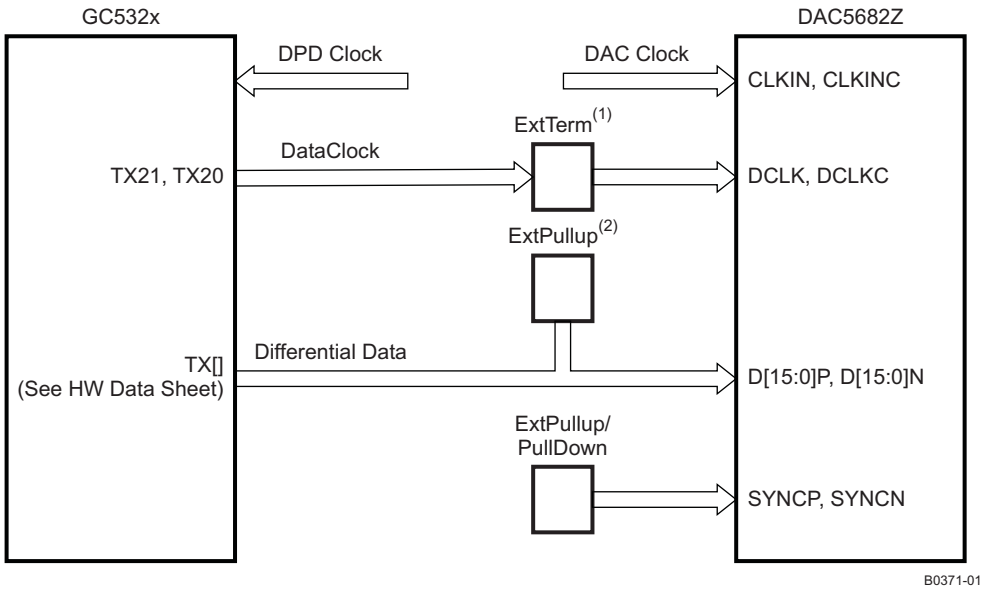
BULK UPCONVERTER (BUC)

The bulk upconverter block can interpolate the DPD block output by 1×, 1.5×, 2×, or 3× with a complex output. The BUC interpolation blocks of 2 and 1.5 can provide 1×, 2×, or 3× interpolation for complex signals. The 1.5× interpolation after DPD is performed by interpolating by 3 in the BUC and decimating by 2 in the OFMT block. The BUC mixer can translate the composite IQ predistorted Tx output if the BUC Interpolation is > 1. Note: the BUC interpolation of 1, 1.5, or 2 is recommended.

OUTPUT FORMATTER AND DAC INTERFACE (OFMT)

The output format and DAC interface presents the GC5328 output in the proper format for the different output interfaces. The output formatter supports a test pattern for testing the DAC5682Z interface. The two output interfaces supported for the GC5328 are:

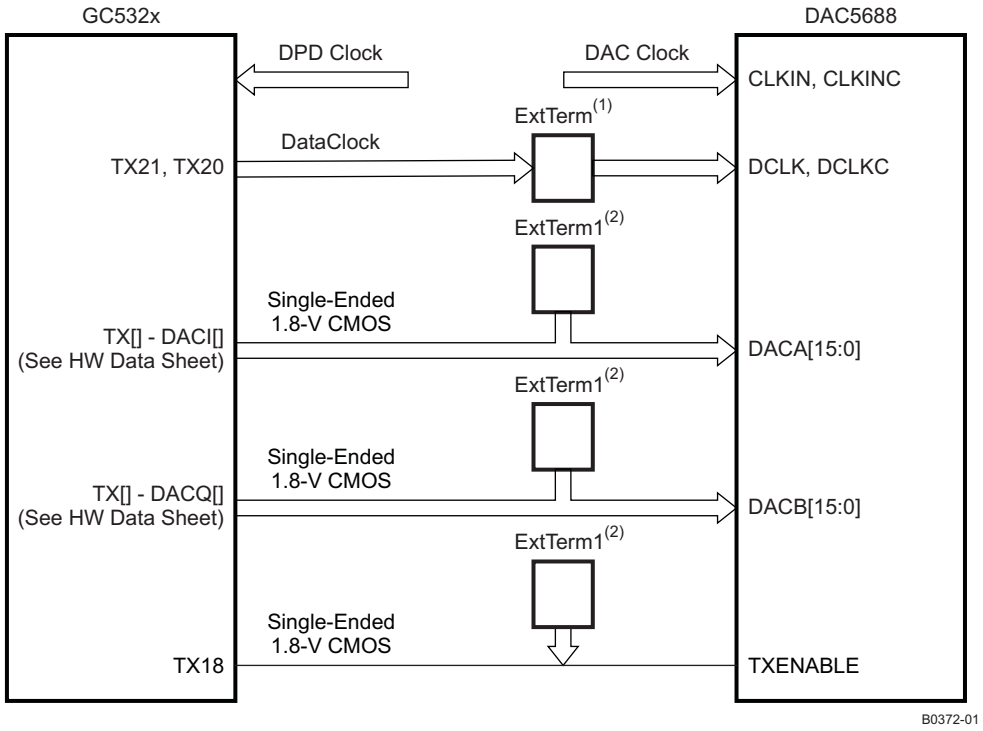
- DAC5682 interleaved IQ
- DAC5688 parallel IQ or interleaved IQ



(1) ExtTerm – see DAC data sheet.

(2) ExtPullup, 500 Ω to 1.8 V, only required when DAC Data Clock > 337 MHz

Figure 4. GC5328 to DAC5682Z Interface



(1) ExtTerm – see DAC data sheet.

(2) ExtTerm1 – tester uses 50 Ω to 0.9 V for termination.

Figure 5. GC5328 to DAC5688 Interface

FEEDBACK PATH (FB)

The feedback path has two LVDS input ports. The A port is preferred (it has better timing). The external ADC Input is converted or processed to generate a complex signal. The feedback equalizer has eight complex taps as a receive equalizer. The feedback path has a mixer to translate the complex IF to the 0IF reference. The ADC feedback rate is at the same rate as the DPD clock (f_S). The typical feedback is $f_S/4$, $f_S3/4$ (m), or $f_S5/4$ IF. The feedback equalizer can provide (m) inverted spectral output, if needed.

The FB complex mixer translates the frequency of the complex input signal to 0IF. The feedback path has the capability for nonlinear correction with a lookup table. TI ADCs that connect to the feedback path are the SDR type ADS5444, DDR type ADS5445 (6149, 5517), DDR with reversed data phase ADSC217. The ADC feedback path has modified connections for shared feedback path operation (see GC5325 schematic, User's Guide, in *References*). The GC5328 simplifies timing by providing a FIFO for each ADC port.

NOTE

There are eight LVDS data lanes and 1 LVDS clock lane. If the ADC has < 8 LVDS data lanes the MSB of the ADC is connected to LVDS lane 7 (MSB) of the A feedback port.

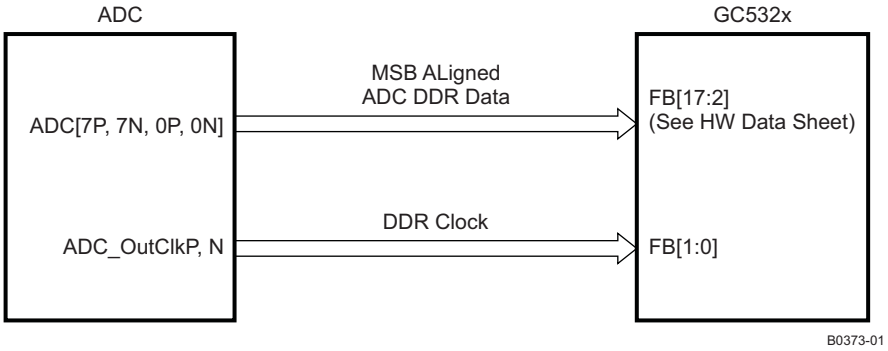


Figure 6. LVDS DDR ADC to GC5328 FB Interface

MICROPROCESSOR (MPU) INTERFACE

The MPU interface is designed to interface with external memory interface (EMIF) ports on TI DSPs operating in asynchronous mode. It consists of a 16-bit bidirectional data bus, a 10-bit address bus, and RDB, WRB, OEB, and CEB control signals. The CEB and OEB signals to the GC5328 require additional logic outside the TMS320C6727B; see Table 1.

Table 1. EMIF to GC5328 Microprocessor Interface

6727 DSP EMIF	GC5328	NOTES
EM_D[15.0]	UPDATA[15.0]	
EM_A[8.0]	UPADDR[9.1]	
EM_BA[1]	UPADDR[0]	
EM_CS2	CEB	Note: DSP HD[22.20] are used for logic for multiple chip-select, inverted outputs.
EM_RWB	OEB	Invert RWB send to OEB
EM_WEB	WRB	
EM_OEB	RDB	
AXRO[7]	Interrupt	Note: DSP [HD22.20] can also be used with a multiplexer to select GC5328 interrupt.

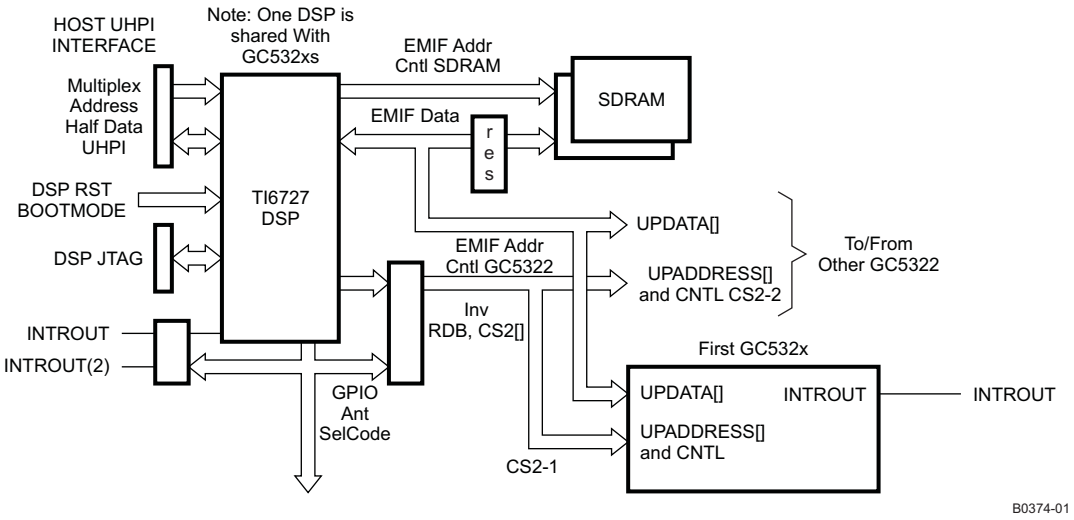


Figure 7. 6727 DSP to GC5328 EMIF Interface

CAPTURE BUFFERS (SCB)

The GC5328 has two capture buffers of 4096 complex words. The capture buffers are normally used to capture the Tx reference signal and the feedback output signal. Capture buffer A can capture:

- The TX reference from the DPD after the circular hard limiter
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(31:16)
- QRD error output

Capture buffer B can capture:

- The TX reference from the DPD after the circular hard limiter
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(15:0)

Standard capture mode – The capture buffers can be armed to collect the 4K complex samples after a programmable delay following a sync event.

Smart capture mode – There are two trigger conditions that combine the number of samples greater than a threshold; these are used to find a number of peak events while the transmit signal is above a threshold. In this case, the magnitude and magnitude-squared of the signal are compared against a threshold and counted. If the capture buffer finds the trigger condition, the capture logic captures the programmed capture-buffer depth after the trigger. This is a combination of DSP software and the GC5328 hardware.

NOTE

Capture buffer A has a special mode to source data for diagnostic testing.

The DSP host-interface software has a function to select and get capture-buffer data. The complex data is then passed from the GC5328 to the EMIF bus, to the DSP, and back to the host processor.

The DSP host software has a signal-power monitoring function. This uses the capture-buffer data to perform special monitoring, power measurement, and error measurements.

There are special DSP software PA protection modes that use the capture buffer to determine the DPD correction applied to the signal, the error between the DPD reference input and the feedback signal. The capture buffers are also used in the initial bulk delay and fractional delay alignment.

INPUT SYNCS AND OUTPUT SYNC

The GC5328 features multiple user-programmable input syncs. There are three syncs sampled with the BBClock, (A, B, and C), and the Sync D,DC as an LVDS sync sampled by the DPD clock. Internally, the GC5328 can also generate timed and software-controlled syncs. The sync A input is required for the GC5328 hardware to initialize. It should ideally be the start of the frame or frame downlink. The output sync is a test signal used for debugging.

The input syncs can be used to trigger:

- Power measurements
- DUC channel delay, dither, and mixer-phase alignment
- Initializing/loading the DUC, feedback, equalizer, LUTs, etc.
- Feedback path tuner alignment
- Capturing and sourcing of data through SCBs

NOTE

The sync A external synchronization should match the customer Tx frame (total Tx period – i.e., 5 ms).

See the baseband interface figure, these synchronization signals must meet the timing of the BBClk.

POWER METERS AND PEAK I–or–Q MONITORS

There are three integrated $I^2 + Q^2$ power meters in the GC5328:

- GPP – each baseband input channel
- CFR – the CFR input or output, and which antenna stream (0, 1)
- DPD – the input to the DPD nonlinear correction after the DPDL gain, and which antenna stream (0, 1)

There are several peak I or Q monitors within the GC5328.

- FRW– The resampled combined IQ interleaved input to the DPD
- DPD – The input to the DPD nonlinear correction after the DPDL gain
- DPD – After the nonlinear correction in DPD, and separately after the linear correction in DPD
- FDBK – There is a peak monitor at the output of the feedback path.

NOTE

The DSP host software has a HW POWER meter setup and Get(Monitor) function to configure and get data from the integrated I^2+Q^2 values.

PIN ASSIGNMENT AND DESCRIPTIONS

ZER Package
(Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB
22	VSS	VSS	VSS	VSS	VSS	UP ADDR	UP ADDR	UP ADDR	UP ADDR	RDB	UP DATA0	VSS	UP DATA3	UP DATA6	VPP1	UP DATA9	UP DATA12	UP DATA15	VSS1	VSS	VSS	VSS
21	VSS	VSS	VSS	VSS	VSS	UP ADDR	UP ADDR	UP ADDR	WRB	CEB	UP DATA1	VSS	UP DATA4	VPP1	UP DATA7	UP DATA10	UP DATA13	VSS	VSS	VSS	VSS	TEST MODE
20	BB0	BB1	BB2	VSS	VSS	UP ADDR	UP ADDR	UP ADDR	VDD SHV	OEB	UP DATA2	VDD SHV	UP DATA5	VDD SHV	UP DATA8	UP DATA11	UP DATA14	VSS	MVV DD2	MVV SS2	INTER-RUPT	TDO
19	BB3	BB4	BB5	BB6	VDD SHV	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD SHV	VDD	VDD	TDI	TCK
18	BB7	BB8	BB9	BB10	VDD	VDD	VDD	VDD	VDD1	VDD	VDD SHV	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VDD SHV	TRSTB	TMS
17	BB11	BB12	BB13	BB14	VDD	VDD	VDD SHV	VDD	VDD	VDD	VDD SHV	VDD	VDD	VDD	VDD	VDD SHV	VDD	VDD	TX37	TX36	TX35	TX34
16	BB15	BBFR	BBCLK	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	TX33	TX32	TX31	TX30
15	SYNC C	SYNC B	SYNC A	SYNC OUT	VDD SHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VHST LHV	VDD	TX29	TX28	TX27	TX26
14	VSSA1	VDDA1	VDD	VSS	VDD SHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VHST LHV	VDD	TX25	TX24	TX23	TX22
13	FB34	FB35	FB32	FB33	VDD SHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VHST LHV	VDD	DAC REFN	DAC REFP	TX21	TX20
12	FB30	FB31	FB28	FB29	VDD SHV	VDD	VSS	VSS	VSS	VSS	VSS1	VSS	VSS	VSS	VSS	VSS	VHST LHV	VDD	VSS	VSS	TX19	TX18
11	FB27	FB26	VDD	VDD	VDD SHV1	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VHST LHV	VDD	TX14	TX15	TX16	TX17
10	FB25	FB24	FB23	FB22	VDD SHV	VDD	VSS	VSS1	VSS1	VSS1	VSS1	VSS1	VSS1	VSS1	VSS1	VSS	VHST LHV	VDD	TX10	TX11	TX12	TX13
9	FB21	FB20	FB19	FB18	VDD SHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VHST LHV	VDD	TX6	TX7	TX8	TX9
8	FB17	FB16	ADC IREF	ADC VREF	VDD SHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VHST LHV	VDD	TX2	TX3	TX4	TX5
7	FB15	FB14	FB13	FB12	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDA	TX0	TX1
6	FB11	F10	VDD	VDD	VDD	VDD	VDD SHV	VDD	VDD	VDD	VDD SHV	VDD	VDD	VDD	VDD	VDD SHV	VDD	VDD	VSS	VSS	VDD SHV	VSSA
5	FB9	FB8	FB7	FB6	VDD	VDD	VDD	VDD	VDD	VDD	VDD SHV	VDD	VDD	VDD	VDD	VDD	VDD	VDD	DPD CLK	DPD CLKC	SYNC D	SYNC DC
4	FB4	FB5	FB2	FB3	VDD SHV	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD SHV	DPD IREF	DPD VREF	VSS
3	FB0	FB1	MFIO 0	MFIO 1	VSS	VPP	MFIO 5	VDD SHV	MFIO 10	MFIO 13	VDD SHV	MFIO 18	MFIO 21	MFIO 24	VDD SHV	MFIO 29	MFIO 32	VSS	RESET B	VSS	VSS	VSS
2	VSS	VSS	VSS	VSS	VSS	MFIO 3	MFIO 4	MFIO 7	MFIO 9	MFIO 12	MFIO 15	MFIO 17	MFIO 20	MFIO 23	MFIO 26	MFIO 28	MFIO 31	VSS	VSS	VSS	VSS	VSS
1	VSS	VSS	VSS	VSS	VSS	MFIO 2	VPP	MFIO 6	MFIO 8	MFIO 11	MFIO 14	MFIO 16	MFIO 19	MFIO 22	MFIO 25	MFIO 27	MFIO 30	MFIO 33	VSS	VSS	VSS	VSS

= Baseband Input
= Signal Interface
= Power and Biasing
= Microprocessor Interface
= Miscellaneous
= JTAG Interface

P0107-01

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
MICROPROCESSOR INTERFACE			
OEB	K20	I	Output enable(inv)
CEB	K21	I	Chip enable(inv)
RDB	K22	I	Read strobe (inv)
WRB	J21	I	Write strobe(inv)
UPADDR[9:0]	J22 ,H20, H21, H22, G20, G21, G22, F20, F21, F22	I	Microprocessor address
UPDATA[15:10]	V22, U20, U21, U22, T20, T21	I/O	Microprocessor data
UPDATA[9:0]	T22, R20, R21, P22, N20, N21, N22, L20, L21, L22	I/O	Microprocessor data
INTERRUPT	AA20	O	Microprocessor interrupt
POWER AND BIASING			
VDD	Y19, W19, W7, V18, V17, V16, V15, V14, V13, V12, V11, V10, V9, V8, V7, V6, V5, V4, U19, U18, U17, U16, U7, U6, U5, U4, T19, T18, T16, T7, T5, T4, R19, R18, R17, R16, R7, R6, R5, R4, P19, P18, P17, P16, P7, P6, P5, P4, N19, N18, N17, N16, N7, N6, N5, N4, M19, M18, M17, M16,M7, M6, M5, M4, L19, L16, L7, L4, K19, K18, K17, K16, K7, K6, K5, K4, J19, J18, J17, J16, J7, J6, J5, J4, H19, H18, H17, H16, H7, H6, H5, H4, G19, G18, G16, G7, G5, G4, F19, F18, F17, F16, F15, F14, F13, F12, F11, F10, F9, F8, F7, F6, F5, F4, E18, E17, E16, E7, E6, E5, D16, D11, D6, C14, C11, C6	PWR	1.2-V supply
VSS	AB22, AB4, AB3, AB2, AB1, AA22, AA21, AA3, AA2, AA1, Y22, Y21, Y12, Y6, Y3, Y2, Y1, W22, W21, W18, W12, W6, W2, W1, V21, V20, V3, V2, T15, T14, T13, T12, T11, T10, T9, T8, R15, R14, R13, R12, R11, R10, R9, R8, P15, P14, P13, P12, P11, P10, P9, P8, N15, N14, N13, N12, N11, N10, N9, N8, M22, M21, M15, M14, M13, M12, M11, M10, M9, M8, L15, L14, L13, L12, L11, L10, L9, L8, K15, K14, K13, K12, K11, K10, K9, K8, J15, J14, J13, J12, J11, J10, J9, J8, H15, H14, H13, H12, H11, H10, H9, H8, G15, G14, G13, G12, G11, G10, G9, G8, E22, E21, E20, E3, E2, E1, D22, D21, D20, D14, D2, D1, C22, C21, C2, C1, B22, B21, B2, B1, A22, A21, A2, A1	PWR	Ground
MVDD2	W20		1.2-V monitor, no connect
MVSS2	Y20		GND monitor, no connect
VHSTLHV	U15, U14, U13, U12, U11, U10, U9, U8	PWR	1.8-V supply
VDDSHV	AA6, Y18, W4, V19, T17, T6, R3, P20, M20, L18, L17, L6, L5, L3, J20, H3, G17, G6, E19, E15, E14, E13, E12, E11, E10, E9, E8, E4	PWR	3.3-V supply
VDDA	Y7	PWR	1.2-V supply (requires filtering)
VSSA	AB6	PWR	Ground (requires filtering)
VDDA1	B14	PWR	1.2-V supply (requires filtering)
VSSA1	A14	PWR	Ground (requires filtering)
VPP	G1, F3	PWR	1.2-V supply
VPP1	R22, P21	PWR	1.2-V supply
DPDIREF	Y4	PWR	DPD bias, 1 kΩ to VSS
DPDVREF	AA4	PWR	DPD bias to VDD
DACREFP	Y13	PWR	DAC bias, 50 Ω to VSS
DACREFN	W13	PWR	DAC bias, 50 Ω to VDDS
ADCIREF	C8	PWR	ADC bias, 1 kΩ to VSS
ADCVREF	D8	PWR	ADC bias to VDD
BASEBAND INPUT			
BB[15:10]	A16, D17, C17, B17, A17, D18	I	Baseband input signal

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
BB[9:0]	C18, B18, A18, D19, C19, B19, A19, C20, B20, A20	I	Baseband input signal
BBCLK	C16	I	Baseband input clock
BBFR	B16	I	Baseband frame for sample and channel timing
MISCELLANEOUS			
RESETB	W3	I	Chip reset (active-low)
TESTMODE	AB21	I	Tie to GND
SYNCA	C15	I	Programmable general-purpose sync
SYNCB	B15	I	Programmable general-purpose sync
SYNCC	A15	I	Programmable general-purpose sync
SYNCD	AA5	I	DPD-purpose sync
SYNCDC	AB5	I	Complementary DPD-purpose sync
SYNCOUT	D15	O	Programmable general-purpose output sync
DPDCLK	W5	I	Clock to DPD
DPDCLKC	Y5	I	Complementary clock to DPD
JTAG INTERFACE			
TCK	AB19	I	JTAG clock
TDI	AA19	I	JTAG data in
TDO	AB20	O	JTAG data out
TRSTB	AA18	I	JTAG reset (active-low)
TMS	AB18	I	JTAG mode select
SIGNAL INTERFACE (Tx-DAC, FB-ADC, see next section for Data Converter Connections)			
TX[37:30]	W17, Y17, AA17, AB17, W16, Y16, AA16, AB16	O	Transmit to DAC(s)
TX[29:20]	W15, Y15, AA15, AB15, W14, Y14, AA14, AB14, AA13, AB13	O	Transmit to DAC(s)
TX[19:10]	AA12, AB12, AB11, AA11, Y11, W11, AB10, AA10, Y10, W10	O	Transmit to DAC(s)
TX[9:0]	AB9, AA9, Y9, W9, AB8, AA8, Y8, W8, AB7, AA7	O	Transmit to DAC(s)
FB[35:30]	B13, A13, D13, C13, B12, A12	I	Feedback from ADC(s)
FB[29:20]	D12, C12, A11, B11, A10, B10, C10, D10, A9, B9	I	Feedback from ADC(s)
FB[19:10]	C9, D9, A8, B8, A7, B7, C7, D7, A6, B6	I	Feedback from ADC(s)
FB[9:0]	A5, B5, C5, D5, B4, A4, D4, C4, B3, A3	I	Feedback from ADC(s)
MFIO[33:0]	V1, U3, U2, U1	I/O	Multifunction input-output interface
MFIO[29:20]	T3, T2 T1, R2, R1, P3, P2, P1, N3, N2	I/O	Multifunction input-output interface
MFIO[19:10]	N1, M3, M2, M1, L2, L1, K3, K2, K1, J3	I/O	Multifunction input-output interface
MFIO[9:0]	J2, J1, H2, H1, G3, G2, F2, F1, D3, C3	I/O	Multifunction input-output interface

SPECIAL POWER-SUPPLY REQUIREMENTS FOR VDDA1, VSSA1, VDDA2, VSSA2

The two PLLs require an analog supply. Each pair (VDDA1, VSSA1) requires a separate filter. These can be generated by filtering the core digital supply (VDD). A representative filter is shown in Figure 8. The filters should be located as close as reasonable to their respective pins (especially the bypass capacitors). The ferrite beads should be series 50R (similar to Murata P/N: BLM31P500SPT; description: IND FB BLM31P500SPT 50R 1206). In particular, supply VDDA1 must be less than or equal to VDD1 when VDD1 is at the low end of the required range. The series resistor assures this condition is met.

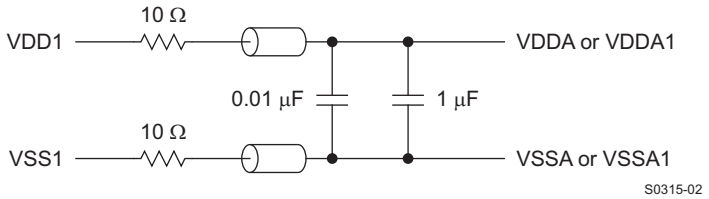


Figure 8. Recommended Filter for VDDA, VDDA1 Power

TX OUTPUT TO DAC5682Z AND DAC5688

The earlier figures show the GC5328 to DAC data, sync, and clock signals. These tables list the specific GC5328 to DAC TX connections.

Table 2. GC5328 TX (Single-Channel Single-Ended HSTL – DAC5688)

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
DACI[15:10]	TX15, TX14, TX11, TX10, TX7, TX6	O	DAC-I output
DACI[9:0]	TX3, TX2, TX1, TX0, TX4, TX5, TX8, TX9, TX12, TX13	O	DAC-I output
DACQ[15:10]	TX24, TX25, TX28, TX29, TX32, TX33	O	DAC-Q output
DACQ[9:0]	TX36, TX37, TX35, TX34, TX31, TX30, TX27, TX26, TX23, TX22	O	DAC-Q output
DACCLK	TX21	O	Clock to DAC
DACCLKC	TX20	O	Cmplementary clock to DAC
DACSYNC	TX18	O	Output data sync

Table 3. GC5328 TX (Single Channel Differential HSTL – DAC5682Z)

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
DAC[15:10]P	TX10, TX6, TX2, TX0, TX4, TX8	O	DAC positive output
DAC[9:0]N	TX12, TX16, TX23, TX27, TX31, TX35, TX32, TX36, TX29, TX25	O	DAC negative output
DAC[15:10]N	TX11, TX7, TX3, TX1, TX5, TX9,	O	DAC negative output
DAC[9:0]N	TX13, TX17, TX22, TX26, TX30, TX34, TX33, TX37, TX28, TX24	O	DAC negative output
DACCLK	TX21	O	Clock to DAC
DACCLKC	TX20	O	Complementary clock to DAC
DACSYNCP	TX14	O	Positive output data sync
DACSYNCN	TX15	O	Negative output data sync

FB INPUT FROM LVDS ADC

Figure 6 shows the ADC data and clock signals to the GC5328. These tables list the specific ADC-to-GC5328 FB connections. There are two feedback (FB) ports, A and B. Port A has faster timing and is preferred. There are several ADC styles:

- LVDS DDR – ADS5545 (ADS61x9, ADS5517)
- LVDS DDR – ADS62C17 – reversed data alignment (same connections as ADS5545)
- LVDS SDR – ADS5544

ADCs are typically connected to the GC5328 so the MSB of the ADC is connected to FB port A MSB. The lower bit numbers follow until the ADC bits are all connected. Any remaining lower-order bits on the FB port should be terminated with resistors, P connection to GND, N connection to 1.8 V as a logic 0. See the GC5325 schematic listed under *References* for an example.

NOTE

There are special connections for shared-feedback ADCs between GC5328s. See the GC5325 schematic diagram for the shared feedback connection to (2) GC5328.

Table 4. Single LVDS SDR ADC to FB Ports A and B

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
ADC[15:10]P	FB2, FB4, FB6, FB8, FB10, FB12	I	ADC positive feedback from PA output
DAC[9:0]P	FB14, FB16, FB20, FB22, FB24, FB26, FB28, FB30, FB32, FB34	I	ADC negative feedback from PA output
ADC[15:10]N	FB3, FB5, FB7, FB9, FB11, FB13	I	ADC negative feedback from PA output
ADC[9:0]N	FB15, FB17, FB21, FB23, FB25, FB27, FB29, FB31, FB33, FB35	I	ADC negative feedback from PA output
ADCCLK	FB0	I	Clock from ADC
ADCCLKC	FB1	I	Complementary clock from ADC

Table 5. Single LVDS DDR ADC to FB Port A (Preferred)

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
ADCA[7:0]P	FB2, FB4, FB6, FB8, FB10, FB12, FB14, FB16	I	ADC-A positive feedback from PA output
ADC[9:0]P	FB3, FB5, FB7, FB9, FB11, FB13, FB15, FB17	I	ADC-A negative feedback from PA output
ADCACLK	FB0	I	Clock from ADC-A
ADCACLKC	FB1	I	Complementary clock from ADC-A

Table 6. Single LVDS DDR ADC to FB Port B

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
ADCB[7:0]P	FB20, FB22, FB24, FB26, FB28, FB30, FB32, FB34	I	ADC-B positive feedback from PA output
ADCB[7:0]N	FB21, FB23, FB25, FB27, FB29, FB31, FB33, FB35	I	ADC-B negative feedback from PA output
ADCBCLK	FB18	I	Clock from ADC-B
ADCBCLKC	FB19	I	Complementary clock from ADC-B

MPU INTERFACE GUIDELINES

The following section describes the hardware interface between the recommended microprocessor, external memory, and the GC5328. Users may select a microprocessor that meets their specific system requirements. Although the hardware can support multiple options, the recommended TMS320C6727 DSP is also fully supported with host control and adaptation software. Figure 7 and Figure 9 illustrate the hardware interface between the DSP, GC5328, and SDRAM. The external memory is required to accommodate the computational efforts of the adaptation algorithm. Although the system evaluation kit suggests dual-parallel 64-Mb/PC133 (128-Mb) memory modules provided by Samsung (K4S641632H-TC(L)75), other memory alternatives are available.

The use of an external inverter with minimal propagation delay is required for OEB of the GC5328; this device is necessary when using a TMS320C6727 DSP. Additional documentation for the hardware interface is available in the *TMS320C672x Hardware Designer's Resource Guide* application report (SPRAA87) and *TMS320C672x DSP External Memory Interface (EMIF)* user's guide (SPRU711).

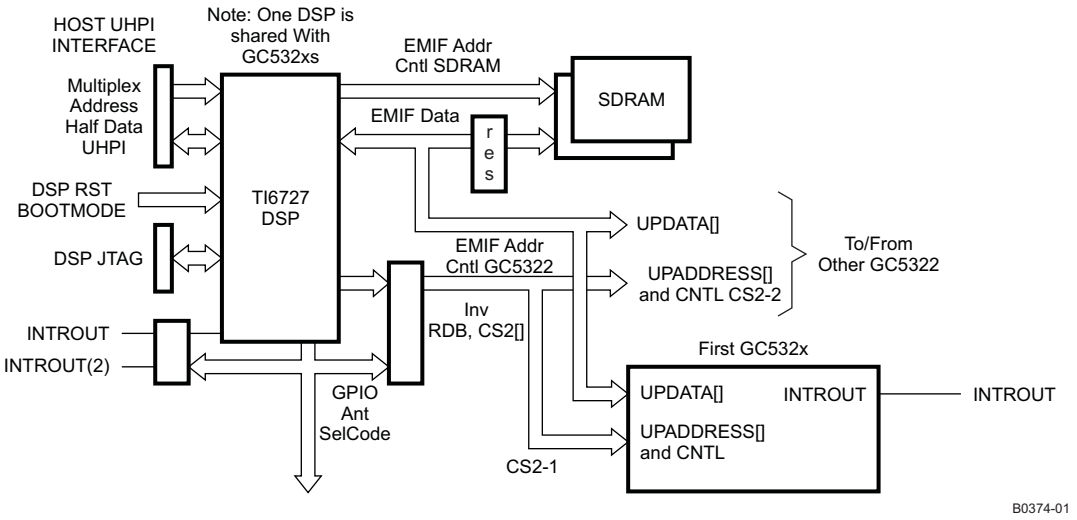


Figure 9. DSP-to-GC5328 EMIF Interface Specifications

ABSOLUTE MAXIMUM RATINGS

			VALUE	UNIT
V_{DD}, V_{DDA}	Core supply voltage		–0.3 to 1.32	V
V_{DDS}	Digital supply voltage for TX		–0.3 to 2	V
V_{DDSHV}	Digital supply voltage		–0.3 to 3.6	V
V_{IN}	Input voltage (under/overshoot)		–0.5 to VDDSHV + 0.5	V
	Clamp current for an input/output		–20 to 20	mA
T_{stg}	Storage temperature		–65 to 150	°C
	Lead soldering temperature, 10 seconds		300	°C
	ESD classification Class 2	(Required 2-kV HBM, 500-V CDM)		
		(Passed 2.5-kV HBM, 500-V CDM, 200-V MM)		
	Moisture sensitivity Class 3 (floor life at 30°C/60% H)		1	week
	Reflow conditions JEDEC standard		260	°C
Latchup	JEDEC Level 2 per JEDEC 78 standard (at 90°C and 1.5 × Vmax)		±100	mA

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{DD}, V_{DDA2}, V_{PP}	Core supply voltages. Note $V_{DDA2} \le V_{DD}$		1.14	1.2	1.26	V
V_{DDA1}	Analog supply for DPD PLL	See (1)	1	1.1	VDD	V
V_{DDS}	Digital supply voltage for TX		1.71	1.8	1.89	V
V_{DDSHV}	Digital supply voltage		3.15	3.3	3.45	V
I_{DD}, I_{DDA1}, I_{DDA2}, I_{PP}	Combined supply current for Vdd, Vdda1, Vdda2, and V_{PP}				3	A
I_{DDS}	Digital supply current for TX				0.25	A
I_{DDSHV}	Digital supply current				0.3	A
T_C	Case temperature	See (2)	–40	30	85	°C

(1) VDDA1 must be less than VDD1 when VDD1 is low. See recommended filtering circuit in Figure 1 Figure 1. Maximum observed current on VDDA1 is 8 mA.
(2) Chip specifications in are production tested to 90°C case temperature. QA tests are performed at 85°C.

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
T_J	Junction temperature	See (3)			105	°C

(3) Thermal management may be required for full-rate operation. Sustained operation at elevated temperatures reduces long-term reliability. Lifetime calculations based on maximum junction temperature of 105°C.

THERMAL CHARACTERISTICS (1)

PARAMETER		484 BGA AT 2.5 W	UNITS
$R_{\theta JA}$	Thermal resistance, junction-to-ambient (still air)	18	°C/W
$R_{\theta JMA1}$	Thermal resistance, junction-to-ambient (1 m/s)	14.3	°C/W
$R_{\theta JC}$	Thermal resistance, junction-to-case	6.8	°C/W
$R_{\theta JB}$	Thermal resistance, junction-to-board	8	°C/W

(1) Customer must check that heat removal is appropriate for the application to limit the junction temperature (T_J) aspecified in the Recommended Operating Conditions. Conducting heat through the ground and power balls, or adding a heat sink and airflow, may be needed to limit junction temperature.

ELECTRICAL CHARACTERISTICS

Describes the electrical characteristics for the baseband interface, multifunction I/O (MFIO), DPD clock and fast sync, MPU and JTAG interfaces over recommended operating conditions. Device is production tested at 90°C for the given specification and characterized at –40°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE						
V_{IL}	CMOS voltage input, low				0.8	V
V_{IH}	CMOS voltage input, high		2		V_{DDSHV}	V
V_{OL}	CMOS voltage output, low	I_{OL} = 2 mA			0.5	V
V_{OH}	CMOS voltage output, high	I_{OH} = –2 mA	2.4		VDDSHV	V
$\|I_{PU}\|$	Pullup current	V_{IN} = 0 V	40	100	200	µA
$\|I_{IN}\|$	Leakage current	V_{IN} = 0 or V_{IN} = V_{DDSHV}			5	µA
DAC INTERFACE (DACP/N[15:0])						
$V_{o(diff)}$	Output differential swing	$\| V_{OD} \| = \| V_{OH} - V_{OL} \|$ (1)	250			mV
V_{comm}	Common mode	$(V_{OH} + V_{OL}) / 2$ (1)	1000			mV
LVDS INTERFACE (FB[35:0], DPDCLK/C, SYNCD/C)						
V_I	Input voltage range			0	2000	mV
$V_{I(diff)}$	Input differential voltage, |Vpos – Vneg|	0 < Vi < 2000 mV		250		mV
		1000 mV < V_I < 1400 mV, FB[35:0] only	90			
R_{IN}	Input differential impedance			80	120	Ω
POWER SUPPLY						
I_{dyn}	Core current	See (2)			1.7	A

(1) HSTL output levels measured at 675 Mb/s delay and with 100-Ω load from P to N. Drive strength set to 0x360.
(2) 400-Mbps DAC signal, 200-Mhz DPD clock, maximum filtering, 70-Mhz BBPLL clock input

SWITCHING CHARACTERISTICS

Describes the electrical characteristics for the baseband interface, MFIO[19,18]. Sync A, B, C, and BB Clock over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
BASEBAND INTERFACE					
$f_{CLK(BB)}$	Baseband input clock frequency	GPP is ACTIVE	25	70	MHz
		GPP is BYPASSED	25	70	
$t_{su(BB)}$	Input data setup time before BBCLK↑	BB[15:0], BBFR, SYNCA, SYNCB, and SYNCC; MFIO18/19	1.3		ns
$t_{h(BB)}$	Input data hold time after BBCLK↑	BB[15:0], BBFR, MFIO18/19	1.5		ns
$t_{h(SYNCA, -B, -C)}$	Input data hold time after BBCLK↑	Valid for SYNCA, SYNCB, and SYNCC	2		ns
$Duty_{CLK(BB)}$	Duty cycle		30%	70%	

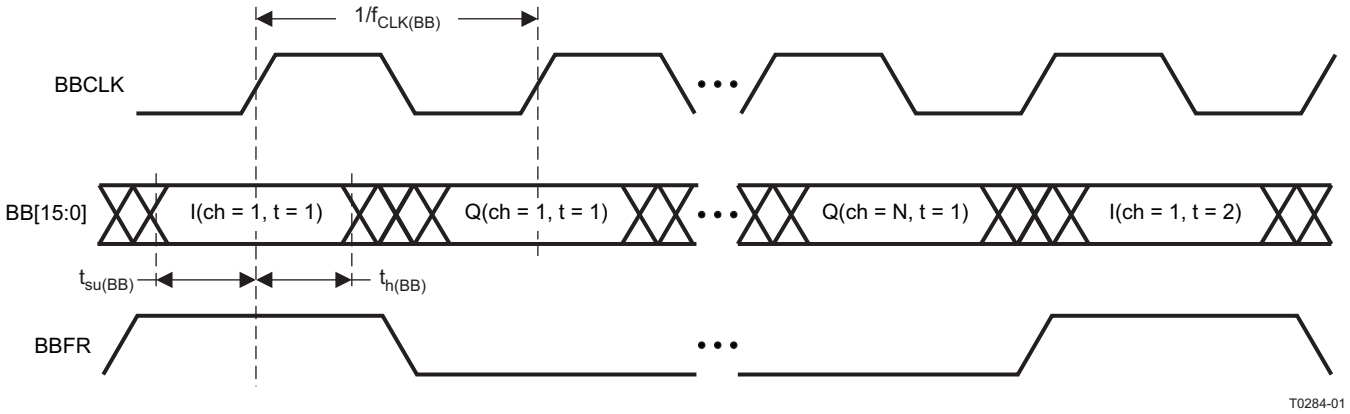


Figure 10. Baseband Timing Specifications

DPD CLOCK AND FAST SYNC SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{CLK(DPD)}$	DPD input clock frequency		100	200	MHz
$Duty_{CLK(DPD)}$	DPD input clock duty cycle		30%	70%	
$t_{h(SYNCD)}$	Input hold time after DPDCLK↑	See (1)	0.2		ns
$t_{su(SYNCD)}$	Input setup time after DPDCLK↑	See (1)	0.4		ns
$t_{h(SYNCA, -B, -C)}$	Input hold time after DPDCLK↑		2		ns
$t_{su(SYNCA, -B, -C)}$	Input setup time after DPDCLK↑		0.4		ns
$Jitter_{CLK(DPD)}$ (2)	Cycle-to cycle jitter		–2.5%	2.5%	

(1) Controlled by design and process
(2) Jitter is based on a period of (1/(DPDClk × 2)) (for BUC Interp 1 or 2); (1/(DPDClk × 3)) (for BUC Interp 1.5 or 3).

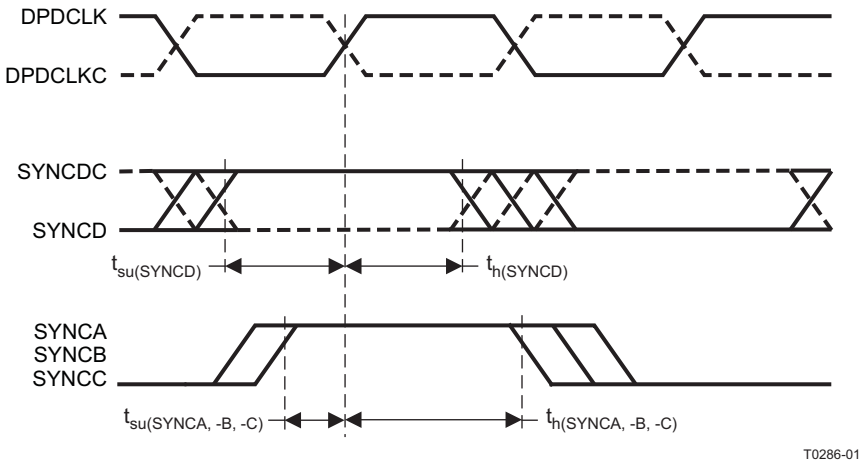


Figure 11. DPD Clock and Fast Sync Timing Specifications

MPU SWITCHING CHARACTERISTICS (READ)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{su(AD)}$	ADDR setup time to RDB↓	WRB is HIGH	5		ns
$t_{su(CEB)}$	CEB setup time to RDB↓	WRB is HIGH	7		ns
$t_{su(OEB)}$	OEB setup time to RDB↓	WRB is HIGH	2		ns
$t_{d(RD)}$	DATA valid time after RDB↓	WRB is HIGH		14	ns
$t_{h(RD)}$	ADDR hold time to RDB↑	WRB is HIGH	2		ns
	OEB, CEB hold time to RDB↑		0		
$t_{HIGH(RD)}$	Time RDB must remain HIGH between READs.	WRB is HIGH(1)	7		ns
$t_{Z(RD)}$	DATA goes high-impedance after OEB↑ or RDB↑	WRB is HIGH(1)		7	ns

(1) Controlled by design and process and not directly tested.

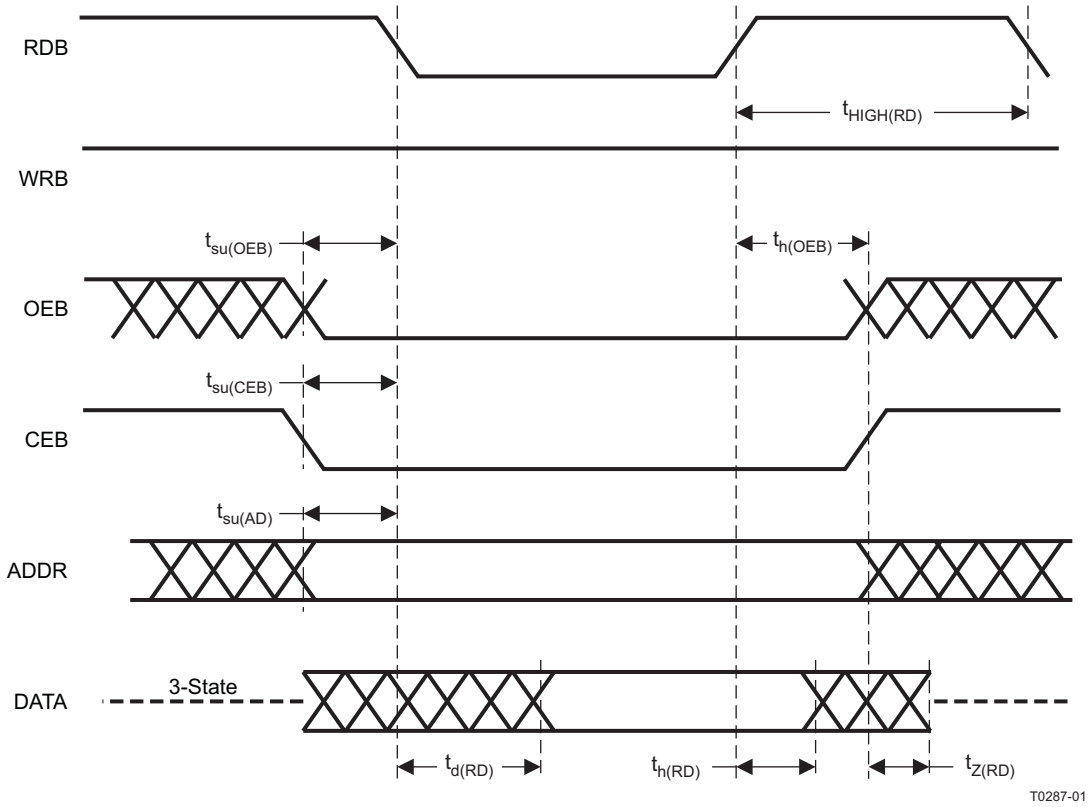


Figure 12. MPU READ Timing Specifications

MPU SWITCHING CHARACTERISTICS (WRITE)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{su(WR)}$	DATA and ADDR setup time to WRB↓		5		ns
	CEB setup time to WRB↓	OEB and RDB are HIGH	7		
	OEB setup time to WRB↓		2		
$t_{h(WR)}$	DATA and ADDR hold time after WRB↑	OEB and RDB are HIGH	2		ns
	OEB and CEB hold time after WRB↑		0		
$t_{low(WR)}$	Time WRB and CEB must remain simultaneously LOW	OEB and RDB are HIGH	15		ns
$t_{high(WR)}$	Time CEB or WRB must remain HIGH between WRITEs	OEB and RDB are HIGH	10		ns

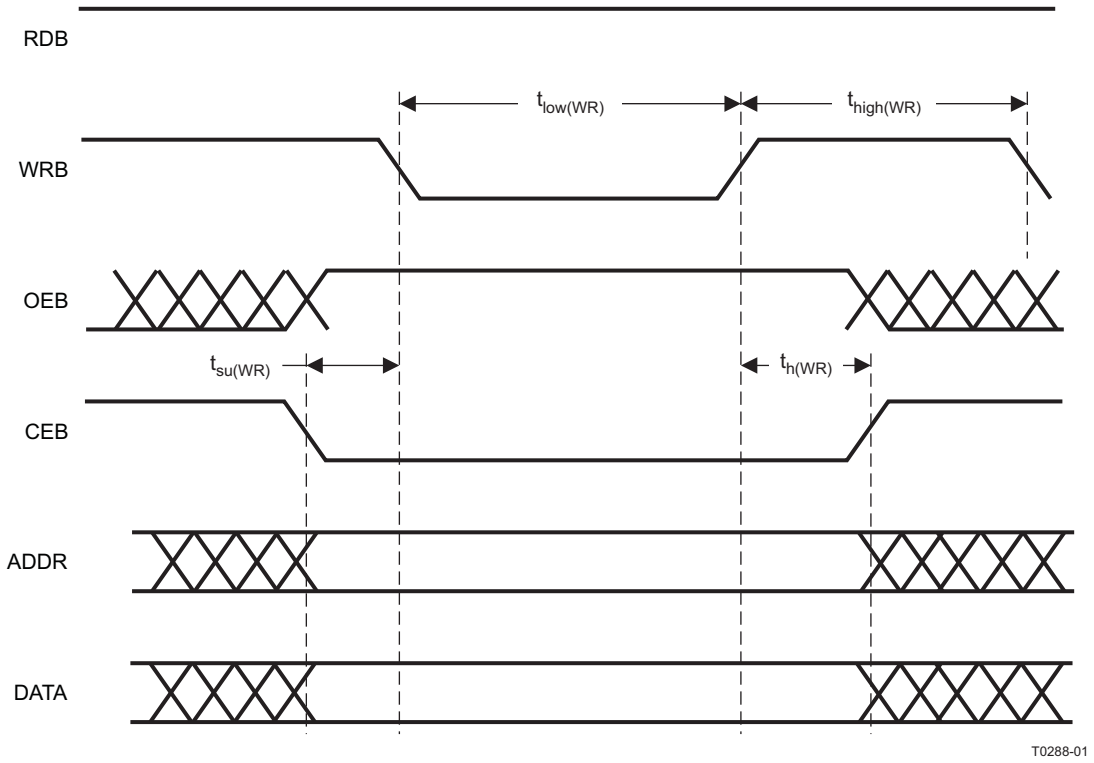


Figure 13. MPU WRITE Timing Specifications

JTAG SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

TEST CONDITIONS PARAMETER			MIN	MAX	UNIT
f_{TCK}	JTAG clock frequency			50	MHz
$t_{p(TCKL)}$	JTAG clock low period		10		ns
$t_{p(TCKH)}$	JTAG clock high period		10		ns
$t_{su(TDI)}$	Input data setup time before TCK↑	Valid for TDI and TMS	1		ns
$t_{h(TDI)}$	Input data hold time after TCK↑	Valid for TDI and TMS	6		ns
$t_{d(TDO)}$	Output data delay from TCK↓			8	ns

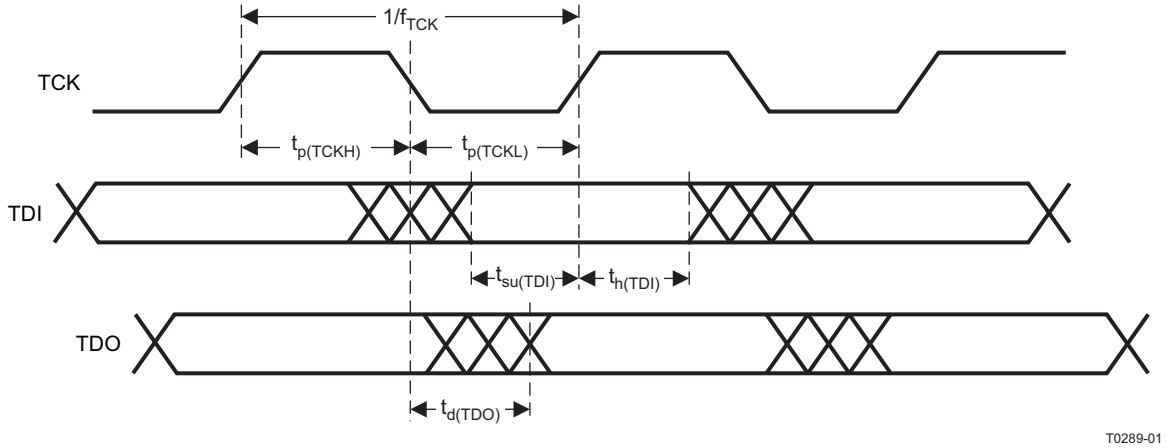


Figure 14. JTAG Timing Specifictions

TX SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HSTL MODE – DDR ex. DAC5682						
$f_{CLK(DAC)}$	DAC output clock frequency	R_L = 100 Ω (1)			300	MHz
$t_{SKW(DAC)}$	DACCLK to DAC data	R_L = 100 Ω (2)			TBD	ps

(1) Because the output clock is DDR, the data rate is 2× the f_{CLK} rate; $f_{CLK(DAC)}$ = (BUC Interp × DPDClk / 2).
(2) $t_{SKW(DAC)}$ data clock-to-data is measured during characterization.

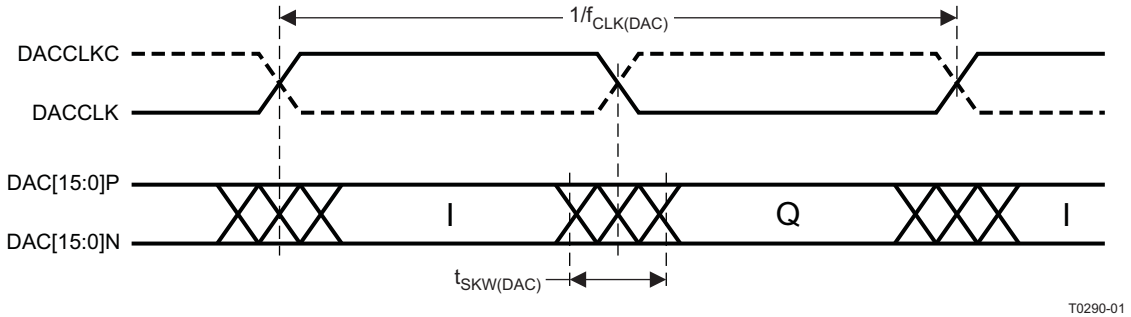


Figure 15. TX Timing Specifications (HSTL – DDR)

TX SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HSTL MODE – SDR ex. DAC5688						
$f_{CLK(DAC)}$	DAC output clock frequency	2-mA load (1)			200	MHz
t_d	DACCLK-to-DACData delay time	2-mA load (2)			1.5	ns
t_{ho}	DACCLK-to-DACData hold time	2-mA load (2)	1.5			ns

(1) Because the output clock is SDR, the positive edge of the clock is used to register the data at the DAC receiver. The clock rate is limited to 200 MHz.
(2) t_d and t_{ho} data clock-to-data is measured during characterization.

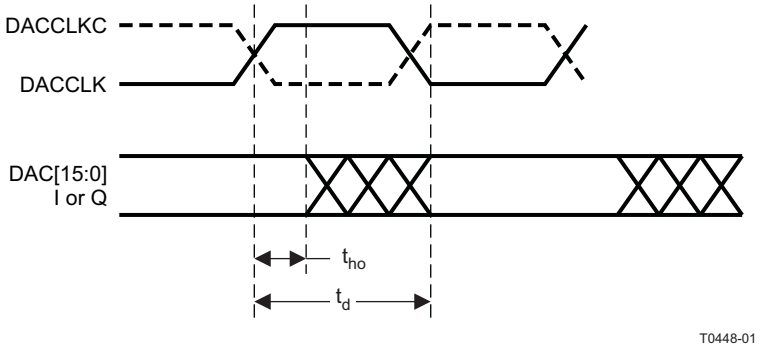


Figure 16. TX Timing Specifications (HSTL – SDR)

ENVELOPE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MFIO CMOS – SDR to Envelope Modulator						
$f_{CLK(ENV)}$	ENVELOPE data output clock frequency	2-mA load (1)			DPDClk/2	MHz
t_d	ENVCLK-to-ENVData delay time	2-mA load (2)			1.5	ns
t_{ho}	ENVCLK-to-ENVData hold time	2-mA load (2)	1.5			ns

(1) Envelope output is magnitude; this is a real output at a DPDClk/2 (100-MHz) rate.
(2) t_d and t_{ho} data clock-to-data is measured during characterization.

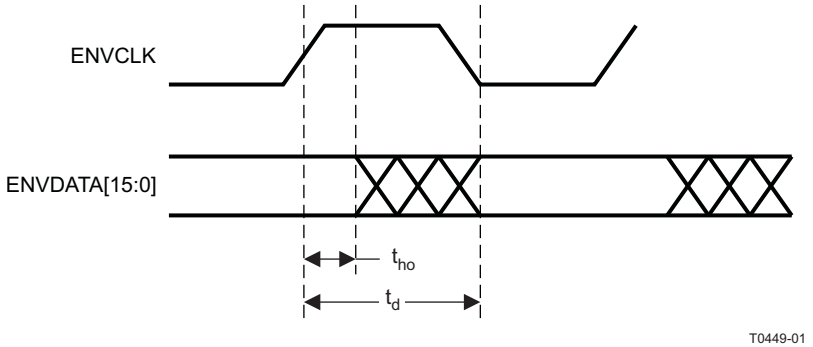


Figure 17. Envelope Timing (MFIO – CMOS 3.3 V)

LVDS SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). The following table uses a shorthand nomenclature, NxM. N means the number of differential pairs used to transmit data from one ADC, and M means the number of bits sent serially down each LVDS pair. Thus, 8x2 means eight LVDS pairs, each containing 2 bits of information sent serially. NOTE: The ADC clock rate must match the DPDClock rate for real feedback.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16x1 SDR LVDS MODE ex. ADS5444						
$f_{CLK(ADC)}$	ADC interface clock frequency	See(1)			200	MHz
$t_{su(ADC[\#]P)}$	Input data setup time before CLK↑	See(1) (2)	300			ps
$t_{h(ADC[\#]P)}$	Input data hold time after CLK↑	See(1) (2)	600			ps
8x2 DDR LVDS MODE ex. ADS5545, ADS6149						
$f_{CLK(ADCA)}$	ADCA interface clock frequency	See(1)			200	MHz
$t_{su(ADCA[\#/2]P)}$	Input data setup time before CLK↑↓	See(1) (3). For port A	430			ps
$t_{h(ADCA[\#/2]P)}$	Input data hold time after CLK↑↓	See(1) (3). For port A	260			ps
$f_{CLK(ADCB)}$	ADCB interface clock frequency	See(1)			200	MHz
$t_{su(ADCB[\#/2]P)}$	Input data setup time before CLK↑↓	See(1) (4). For port B	800			ps
$t_{h(ADCB[\#/2]P)}$	Input data hold time after CLK↑↓	See(1) (4). For port B	400			ps

(1) Specifications are limited by GC5328 performance and may exceed the example ADC capabilities for the given interface.
(2) Setup and hold measured for ADC[15:0]P, ADC[15:0]N valid for (VOD > 250 mV) to/from ADCCLK and ADCCLKC clock crossing (VOD = 0).
(3) Setup and hold measured for ADCA[7:0]P, ADCA[7:0]N valid for (VOD > 250 mV) to/from ADCACLK and ADCACLKC clock crossing (VOD = 0).
(4) Setup and hold measured for ADCB[7:0]P, ADCB[7:0]N valid for (VOD > 250 mV) to/from ADCBCLK and ADCBCLKC clock crossing (VOD = 0).

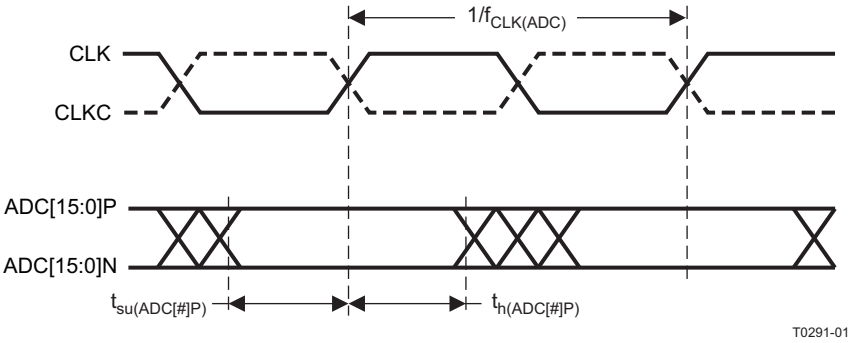


Figure 18. LVDS Timing Specification (16x1 SDR LVDS)

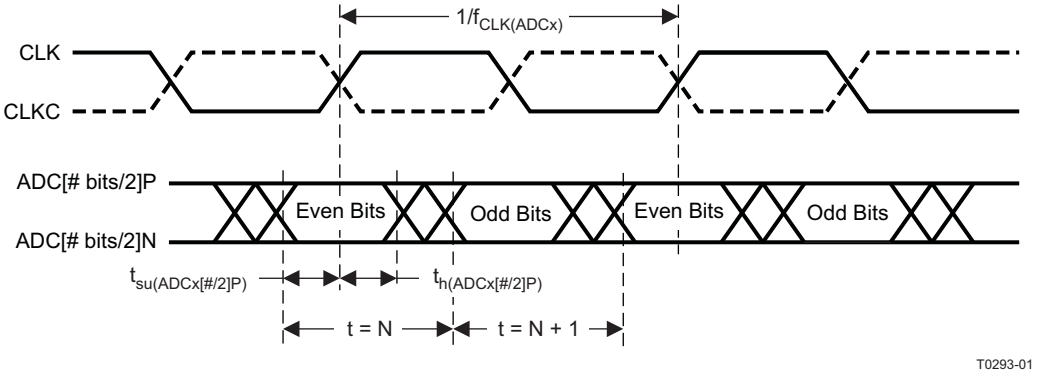


Figure 19. LVDS Timing Specification (8x2 DDR LVDS)

GLOSSARY OF TERMS

3G	Third-generation (refers to next-generation wideband cellular systems that use CDMA)
3GPP	Third-generation partnership project (W-CDMA specification, www.3gpp.org)
3GPP2	Third-generation partnership project 2 (cdma2000 specification, www.3gpp2.org)
ACLR	Adjacent channel leakage ratio (measure of out-of-band energy from one CDMA carrier)
ACPR	Adjacent channel power ratio
ADC	Analog-to-digital converter
BW	Bandwidth
CCDF	Complementary cumulative distribution function
CDMA	Code division multiple access (spread spectrum)
CEVM	Composite error vector magnitude
CFR	Crest factor reduction
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
dB	Decibels
dBm	Decibels relative to 1 mW (30 dBm = 1 W)
DDR	Dual data rate (ADC output format)
DSP	Digital signal processing or digital signal processor
DUC	Digital upconverter (usually provides the GC5328 input)
EVM	Error vector magnitude
FIR	Finite impulse response (type of digital filter)
I/Q	In-phase and quadrature (signal representation)
IF	Intermediate frequency
IIR	Infinite impulse response (type of digital filter)
JTAG	Joint Test Action Group (chip debug and test standard 1149.1)
LO	Local oscillator
LSB	Least-significant bit
Mb	Megabits (divide by 8 for megabytes MB)
MSB	Most-significant bit
MSPS	Megasamples per second (1×10^6 samples/s)
PA	Power amplifier
PAR	Peak-to-average ratio
PCDE	Peak code domain error
PDC	Peak detection and cancellation (stage)
PDF	Probability density function
RF	Radio frequency
RMS	Root mean square (method to quantify error)
SDR	Single data rate (ADC output format)
SEM	Spectrum emission mask
SNR	Signal-to-noise ratio (usually measured in dB or dBm)
UMTS	Universal mobile telephone service
W-CDMA	Wideband code division multiple access (synonymous with 3GPP)
WiBRO	Wireless broadband (Korean initiative IEEE 802.16e)
WiMAX	Worldwide Interoperability of Microwave Access (IEEE 802.16e)

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
GC5328IZER	ACTIVE	BGA	ZER	484	60	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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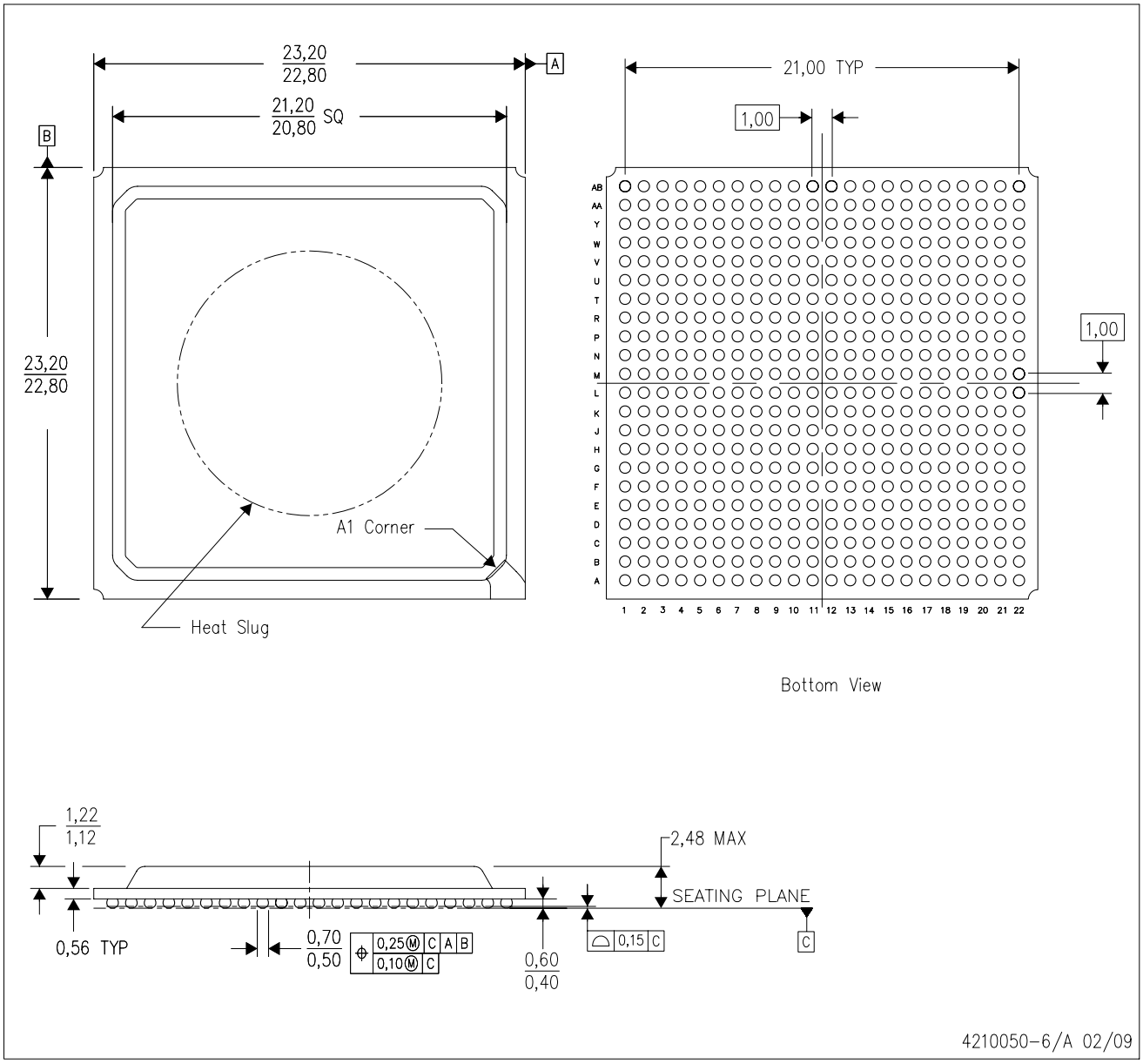
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZER (S–PBGA–N484) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–151
D. Thermally enhanced molded plastic package with heat slug (HSL).
E. This is a Pb–free solder ball design.

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