TEXAS INSTRUMENTS

DRV8320, DRV8320R
DRV8323, DRV8323R

SLVSDJ3A – FEBRUARY 2017 – REVISED APRIL 2017

DRV832x 6 to 60-V Three-Phase Smart Gate Driver

1 Features

- Triple Half-Bridge Gate Driver
  - Drives High-Side and Low-Side N-Channel MOSFETs
  - Supports 100% PWM Duty Cycle
- Smart Gate Drive Architecture
  - Adjustable Slew Rate Control
  - 10-mA to 1-A Peak Source Current
  - 20-mA to 2-A Peak Sink Current
- Integrated Gate Driver Power Supplies
  - High-Side Charge Pump
  - Low-Side Linear Regulator
- 6 to 60-V Operating Voltage Range
- Optional Integrated Buck Regulator
  - LMR16006X SIMPLE SWITCHER®
  - 4 to 60-V Operating Voltage Range
  - 0.8 to 60-V, 600-mA Output Capability
- Optional Integrated Triple Current Shunt Amplifiers
  - Adjustable Gain (5, 10, 20, 40 V/V)
  - Bidirectional or Unidirectional Support
- Selectable SPI or Hardware Interface
- 6x, 3x, 1x, and Independent PWM Modes
- Supports 1.8-V, 3.3-V, and 5-V Logic Inputs
- Low-Power Sleep Mode (20-µA)
- Linear Voltage Regulator, 3.3 V, 30 mA
- Compact QFN Packages and Footprints
- Efficient System Design With CSD88599Q5DC
- Integrated Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - MOSFET Overcurrent Protection (OCP)
  - Gate Driver Fault (GDF)
  - Thermal Warning and Shutdown (OTW/OTSD)
  - Fault Condition Indicator (nFAULT)

2 Applications

- BLDC Motor Modules
- CPAPs, Fans, and Pumps
- E-Bikes
- Power Tools and Lawn Appliances
- Drones, Robotics, and RC Toys
- ATM and Currency Counting

3 Description

The DRV832x family of devices are integrated gate drivers for three-phase applications. The devices provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV832x generates the proper gate drive voltages using an integrated charge pump for the high-side MOSFETs and a linear regulator for the low-side MOSFETs. The smart gate drive architecture supports up to 1-A source and 2-A sink peak gate drive current capability. The DRV832x can operate from a single power supply and supports a wide input supply range of 6 to 60-V for the gate driver and 4 to 60-V for the optional buck regulator.

The 6x, 3x, 1x, and independent input PWM modes allow for simple interfacing to controller circuits. Gate drive and device configuration settings are highly configurable through a SPI or hardware (H/W) interface. The DRV8323 and DRV8323R devices have three, integrated low-side shunt amplifiers that allow bidirectional current sensing on all three phases of the drive stage. The DRV8320R and DRV8323R devices integrate a 600-mA buck regulator.

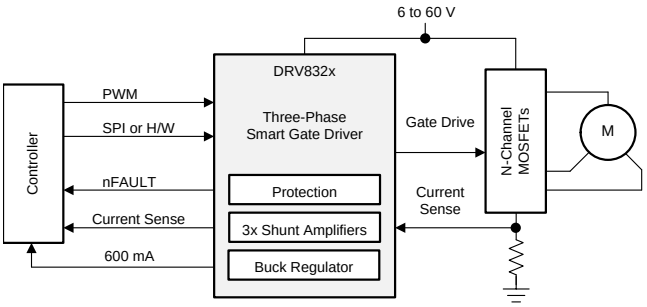
A low-power sleep mode is provided to achieve low quiescent current draw by shutting down most of the internal circuitry. Internal protection functions are provided for undervoltage lockout, charge pump fault, MOSFET overcurrent, MOSFET short circuit, gate driver fault, and overtemperature. Fault conditions are indicated on the nFAULT pin with details through the device registers for SPI device variants.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8320	WQFN (32)	5.00 mm × 5.00 mm
DRV8320R	VQFN (40)	6.00 mm × 6.00 mm
DRV8323	WQFN (40)	6.00 mm × 6.00 mm
DRV8323R	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2017) to Revision A **Page**

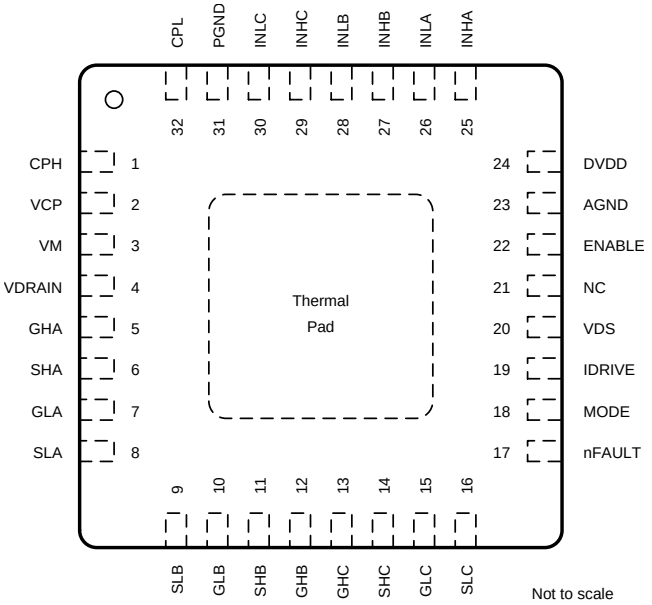
- Changed the test condition for the I_{BIAS} parameter in the *Electrical Characteristics* table ... 14
- Changed the GHx values in the *3x PWM Mode Truth Table* ... 29
- Changed the calibration description and added auto calibration feature description ... 42

5 Device Comparison Table

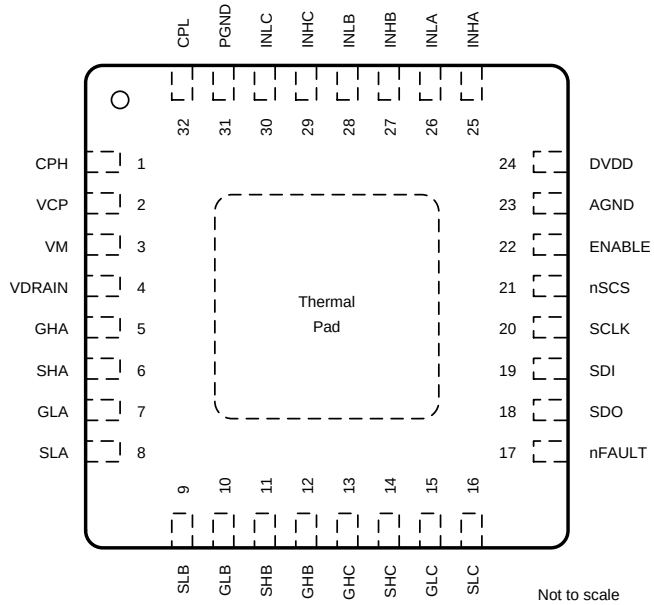
DEVICE	VARIANT	SHUNT AMPLIFIERS	BUCK REGULATOR	INTERFACE
DRV8320	DRV8320H	0	None	Hardware (H)
	DRV8320S			SPI (S)
DRV8320R	DRV8320RH		600 mA (R)	Hardware (H)
	DRV8320RS			SPI (S)
DRV8323	DRV8323H	3	None	Hardware (H)
	DRV8323S			SPI (S)
DRV8323R	DRV8323RH		600 mA (R)	Hardware (H)
	DRV8323RS			SPI (S)

6 Pin Configuration and Functions

DRV8320H RTV Package
32-Pin WQFN With Exposed Thermal Pad
Top View



DRV8320S RTV Package
32-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions—32-Pin DRV8320 Devices

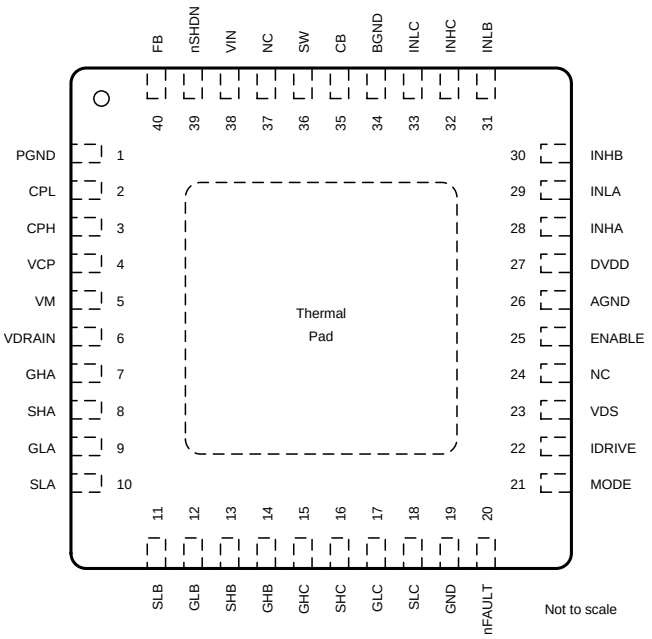
PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8320H	DRV8320S		
AGND	23	23	PWR	Device analog ground. Connect to system ground.
CPH	1	1	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	32	32	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DVDD	24	24	PWR	3.3-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	22	22	I	Gate driver enable. When this pin is logic low the device enters a low power sleep mode. An 8 to 40-µs pulse can be used to reset fault conditions.
GHA	5	5	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	12	12	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	7	7	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain

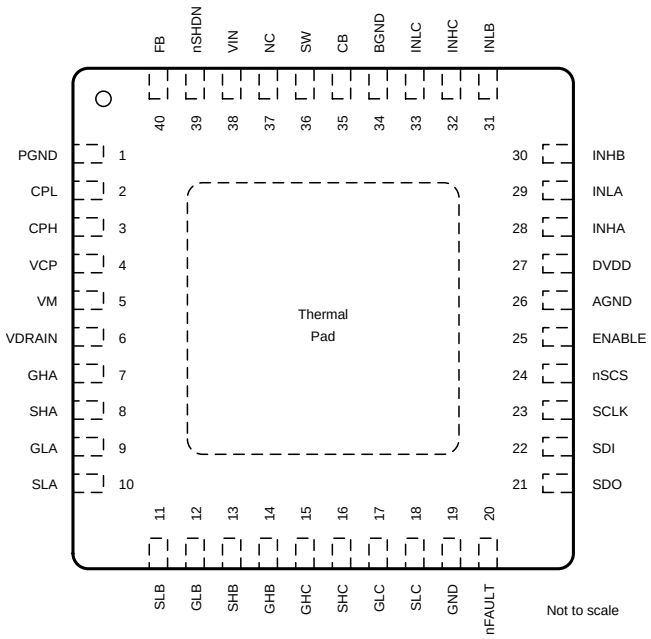
Pin Functions—32-Pin DRV8320 Devices (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8320H	DRV8320S		
GLC	15	15	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	19	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	25	25	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	27	27	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	29	29	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	26	26	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	28	28	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	30	30	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	18	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
NC	21	—	NC	No internal connection. This pin can be left floating or connected to system ground.
nFAULT	17	17	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
nSCS	—	21	I	Serial chip select. A logic low on this pin enables serial interface communication.
PGND	31	31	PWR	Device power ground. Connect to system ground.
SCLK	—	20	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	19	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	18	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor.
SHA	6	6	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	11	11	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	14	14	I	High-side source sense input. Connect to the high-side power MOSFET source.
SLA	8	8	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SLB	9	9	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SLC	16	16	I	Low-side source sense input. Connect to the low-side power MOSFET source.
VCP	2	2	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
VDRAIN	4	4	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains.
VDS	20	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VM	3	3	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.

DRV8320RH RHA Package
40-Pin VQFN With Exposed Thermal Pad
Top View



DRV8320RS RHA Package
40-Pin VQFN With Exposed Thermal Pad
Top View

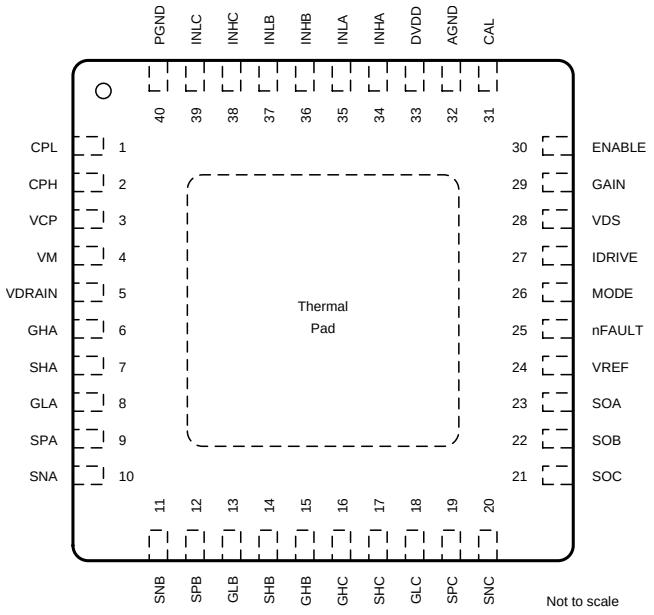


Pin Functions—40-Pin DRV8320R Devices

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8320RH	DRV8320RS		
AGND	26	26	PWR	Device analog ground. Connect to system ground.
BGND	34	34	PWR	Buck regulator ground. Connect to system ground.
CB	35	35	PWR	Buck regulator bootstrap input. Connect a X5R or X7R, 0.1-µF, 16-V, capacitor between the CB and SW pins.
CPH	3	3	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	2	2	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DVDD	27	27	PWR	3.3-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	25	25	I	Gate driver enable. When this pin is logic low the device enters a low power sleep mode. An 8 to 40-µs low pulse can be used to reset fault conditions.
FB	40	40	I	Buck feedback input. A resistor divider from the buck post inductor output to this pin sets the buck output voltage.
GHA	7	7	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	14	14	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	15	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	9	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	12	12	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	17	17	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GND	19	19	PWR	Device ground. Connect to system ground.
IDRIVE	22	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	28	28	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	30	30	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	32	32	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	29	29	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	31	31	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	33	33	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	21	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
NC	24	—	NC	No internal connection. This pin can be left floating or connected to system ground.
NC	37	37	NC	No internal connection. This pin can be left floating or connected to system ground.
nFAULT	20	20	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
nSCS	—	24	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSHDN	39	39	I	Buck shutdown input. Enable and disable input (high voltage tolerant). Internal pullup current source. Pull below 1.25 V to disable. Float to enable. Establish input undervoltage lockout with two resistor divider.
PGND	1	1	PWR	Device power ground. Connect to system ground.
SCLK	—	23	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	22	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	21	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor.
SHA	8	8	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	13	13	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	16	16	I	High-side source sense input. Connect to the high-side power MOSFET source.
SLA	10	10	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SLB	11	11	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SLC	18	18	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SW	36	36	O	Buck switch node. Connect this pin to an inductor, diode, and the CB bootstrap capacitor.
VCP	4	4	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
VDRAIN	6	6	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains.
VDS	23	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VIN	38	38	PWR	Buck regulator power supply input. Place an X5R or X7R, VM-rated ceramic capacitor between the VIN and BGND pins.
VM	5	5	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain

DRV8323H RTA Package
40-Pin WQFN With Exposed Thermal Pad
Top View



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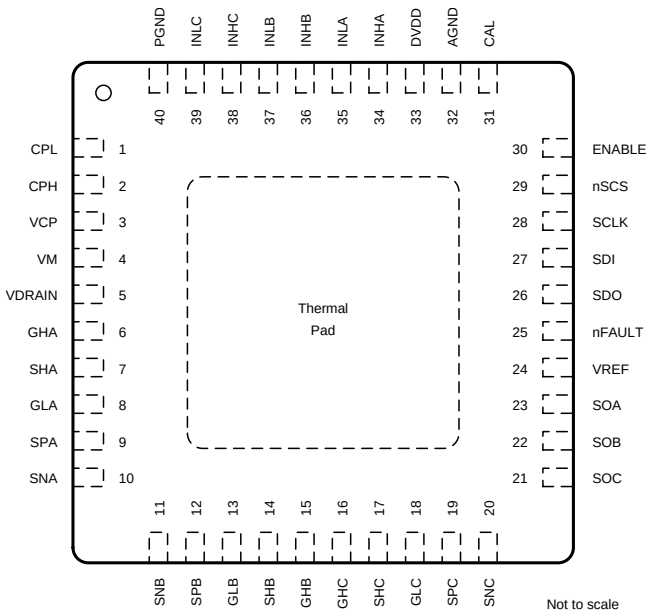
DRV8323S RTA Package
40-Pin WQFN With Exposed Thermal Pad
Top View



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Pin Functions—40-Pin DRV8323 Devices

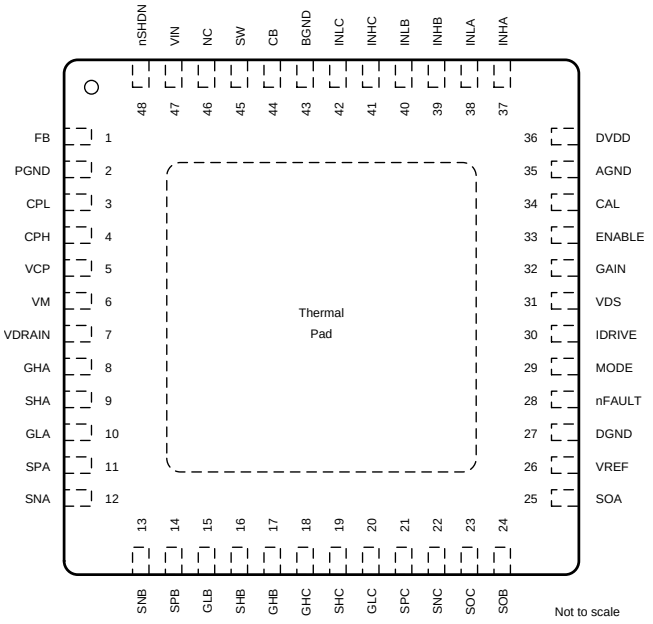
PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8323H	DRV8323S		
AGND	32	32	PWR	Device analog ground. Connect to system ground.
CAL	31	31	I	Amplifier calibration input. Set logic high to internally short amplifier inputs and perform auto offset calibration.
CPH	2	2	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	1	1	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DVDD	33	33	PWR	R 3.3-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	30	30	I	Gate driver enable. When this pin is logic low the device enters a low power sleep mode. An 8 to 40-µs low pulse can be used to reset fault conditions.
GAIN	29	—	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GHA	6	6	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	15	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	16	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	8	8	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	13	13	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	18	18	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	27	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	34	34	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	36	36	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	38	38	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	35	35	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	37	37	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	39	39	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	26	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
nFAULT	25	25	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
nSCS	—	29	I	Serial chip select. A logic low on this pin enables serial interface communication.
PGND	40	40	PWR	Device power ground. Connect to system ground.
SCLK	—	28	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	27	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	26	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor.

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain

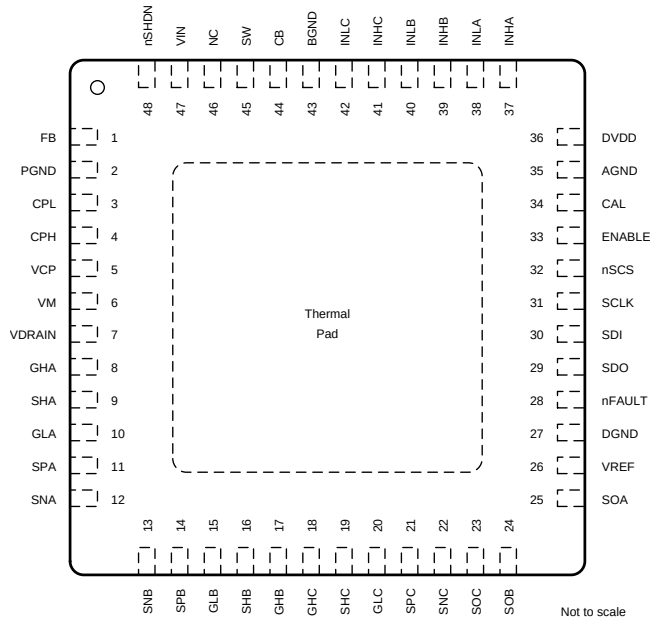
Pin Functions—40-Pin DRV8323 Devices (continued)

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8323H	DRV8323S		
SHA	7	7	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	14	14	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	17	17	I	High-side source sense input. Connect to the high-side power MOSFET source.
SNA	10	10	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNB	11	11	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNC	20	20	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SOA	23	23	O	Shunt amplifier output.
SOB	22	22	O	Shunt amplifier output.
SOC	21	21	O	Shunt amplifier output.
SPA	9	9	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPB	12	12	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPC	19	19	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
VCP	3	3	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
VDRAIN	5	5	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains.
VDS	28	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VM	4	4	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.
VREF	24	24	PWR	Shunt amplifier power supply input and reference. Connect a X5R or X7R, 0.1-µF, 6.3-V ceramic capacitor between the VREF and AGND pins.

DRV8323RH RGZ Package
48-Pin VQFN With Exposed Thermal Pad
Top View



DRV8323RS RGZ Package
48-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions—48-Pin DRV8323R Devices

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8323RH	DRV8323RS		
AGND	35	35	PWR	Device analog ground. Connect to system ground.
BGND	43	43	PWR	Buck regulator ground. Connect to system ground.
CAL	34	34	I	Amplifier calibration input. Set logic high to internally short amplifier inputs and perform auto offset calibration.

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain

Pin Functions—48-Pin DRV8323R Devices (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8323RH	DRV8323RS		
CB	44	44	PWR	Buck regulator bootstrap input. Connect a X5R or X7R, 0.1-µF, 16-V, capacitor between the CB and SW pins.
CPH	4	4	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	3	3	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DGND	27	27	PWR	Device ground. Connect to system ground.
DVDD	36	36	PWR	3.3-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	33	33	I	Gate driver enable. When this pin is logic low the device enters a low power sleep mode. An 8 to 40-µs low pulse can be used to reset fault conditions.
FB	1	1	I	Buck feedback input. A resistor divider from the buck post inductor output to this pin sets the buck output voltage.
GAIN	32	—	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GHA	8	8	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	17	17	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	18	18	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	10	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	15	15	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	20	20	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	30	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	37	37	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	39	39	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	41	41	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	38	38	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	40	40	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	42	42	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	29	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
NC	46	46	NC	No internal connection. This pin can be left floating or connected to system ground.
nFAULT	28	28	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
nSCS	—	32	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSHDN	48	48	I	Buck shutdown input. Enable and disable input (high voltage tolerant). Internal pullup current source. Pull below 1.25 V to disable. Float to enable. Establish input undervoltage lockout with two resistor divider.
PGND	2	2	PWR	Device power ground. Connect to system ground.
SCLK	—	31	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	30	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	29	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor.
SHA	9	9	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	16	16	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	19	19	I	High-side source sense input. Connect to the high-side power MOSFET source.
SNA	12	12	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNB	13	13	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNC	22	22	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SOA	25	25	O	Shunt amplifier output.
SOB	24	24	O	Shunt amplifier output.
SOC	23	23	O	Shunt amplifier output.
SPA	11	11	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPB	14	14	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPC	21	21	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SW	45	45	O	Buck switch node. Connect this pin to an inductor, diode, and the CB bootstrap capacitor.
VCP	5	5	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
VDRAIN	7	7	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains.
VDS	31	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VIN	47	47	PWR	Buck regulator power supply input. Place an X5R or X7R, VM-rated ceramic capacitor between the VIN and BGND pins.
VM	6	6	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.
VREF	26	26	PWR	Shunt amplifier power supply input and reference. Connect a X5R or X7R, 0.1-µF, 6.3-V ceramic capacitor between the VREF and AGND pins.

7 Specifications

7.1 Absolute Maximum Ratings

at T_A = –40°C to +125°C (unless otherwise noted)(1)

	MIN	MAX	UNIT
GATE DRIVER			
Power supply pin voltage (VM)	–0.3	65	V
Voltage differential between ground pins (AGND, BGND, DGND, PGND)	–0.3	0.3	V
MOSFET drain sense pin voltage (VDRAIN)	–0.3	65	V
Charge pump pin voltage (CPH, VCP)	–0.3	V_{VM} + 13.5	V
Charge-pump negative-switching pin voltage (CPL)	–0.3	V_{VM}	V
Internal logic regulator pin voltage (DVDD)	–0.3	3.8	V
Digital pin voltage (CAL, ENABLE, GAIN, IDRIVE, INHx, INLx, MODE, nFAULT, nSCS, SCLK, SDI, SDO, VDS)	–0.3	5.75	V
Continuous high-side gate drive pin voltage (GHx)	–5(2)	V_{VCP} + 0.5	V
Transient 200-ns high-side gate drive pin voltage (GHx)	–7	V_{VCP} + 0.5	V
High-side gate drive pin voltage with respect to SHx (GHx)	–0.3	13.5	V
Continuous high-side source sense pin voltage (SHx)	–5(2)	V_{VM} + 5	V
Transient 200-ns high-side source sense pin voltage (SHx)	–7	V_{VM} + 7	V
Continuous low-side gate drive pin voltage (GLx)	–0.5	13.5	V
Gate drive pin source current (GHx, GLx)	Internally limited		A
Gate drive pin sink current (GHx, GLx)	Internally limited		A
Continuous low-side source sense pin voltage (SLx)	–1	1	V
Transient 200-ns low-side source sense pin voltage (SLx)	–3	3	V
Continuous shunt amplifier input pin voltage (SNx, SPx)	–1	1	V
Transient 200-ns shunt amplifier input pin voltage (SNx, SPx)	–3	3	V
Reference input pin voltage (VREF)	–0.3	5.75	V
Shunt amplifier output pin voltage (SOx)	–0.3	V_{VREF} + 0.3	V
BUCK REGULATOR			
Power supply pin voltage (VIN)	–0.3	65	V
Shutdown control pin voltage (nSHDN)	–0.3	V_{VIN}	V
Voltage feedback pin voltage (FB)	–0.3	7	V
Bootstrap pin voltage with respect to SW (CB)	–0.3	7	V
Switching node pin voltage (SW)	–0.3	V_{VIN}	V
Switching node pin voltage less than 30-ns transients (SW)	–2	V_{VIN}	V
DRV832x			
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Continuous high-side gate pin (GHx) and phase node pin voltage (SHx) should be limited to –2 V minimum for an absolute maximum of 65 V on VM. At 60 V and below, the full specification of –5 V continuous on GHx and SHx is allowable.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

at T_A = –40°C to +125°C (unless otherwise noted)

		MIN	MAX	UNIT
GATE DRIVER				
V_{VM}	Power supply voltage (VM)	6	60	V
V_I	Input voltage (CAL, ENABLE, GAIN, IDRIVE, INHx, INLx, MODE, nSCS, SCLK, SDI, VDS)	0	5.5	V
f_{PWM}	Applied PWM signal (INHx, INLx)	0	200 (1)	kHz
I_{GATE_HS}	High-side average gate-drive current (GHx)	0	25 (1)	mA
I_{GATE_LS}	Low-side average gate-drive current (GLx)	0	25 (1)	mA
I_{DVDD}	External load current (DVDD)	0	30 (1)	mA
V_{VREF}	Reference voltage input (VREF)	3	5.5	V
I_{SO}	Shunt amplifier output current (SOx)	0	5	mA
V_{OD}	Open drain pullup voltage (nFAULT, SDO)	0	5.5	V
I_{OD}	Open drain output current (nFAULT, SDO)	0	5	mA
BUCK REGULATOR				
V_{VIN}	Power supply voltage (VIN)	4	60	V
V_{nSHDN}	Shutdown control input voltage (nSHDN)	0	60	V
DRV832x				
T_A	Operating ambient temperature	–40	125	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC (1)		DRV832x				UNIT
		RTV (WQFN)	RHA (VQFN)	RTA (WQFN)	RGZ (VQFN)	
		32 PINS	40 PINS	40 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	30.1	32.1	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.8	16.7	11	13.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	9.9	7.1	9.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.5	0.1	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.8	9.9	7.1	9.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	2.2	2.1	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = –40°C to +125°C, V_{VM} = 6 to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DVDD, VCP, VM)						
I_{VM}	VM operating supply current	V_{VM} = 24 V, ENABLE = 3.3 V, INHx/INLx = 0 V		10.5	14	mA
I_{VMQ}	VM sleep mode supply current	ENABLE = 0 V, V_{VM} = 24 V, T_A = 25°C		12	20	µA
		ENABLE = 0 V, V_{VM} = 24 V, T_A = 125°C (1)			50	
t_{RST} (1)	Reset pulse time	ENABLE = 0 V period to reset faults	8		40	µs
t_{WAKE}	Turnon time	V_{VM} > V_{UVLO}, ENABLE = 3.3 V to outputs ready			1	ms
t_{SLEEP}	Turnoff time	ENABLE = 0 V to device sleep mode			1	ms
V_{DVDD}	DVDD regulator voltage	I_{DVDD} = 0 to 30 mA	3	3.3	3.6	V
V_{VCP}	VCP operating voltage w.r.t VM	V_{VM} = 13 V, I_{VCP} = 0 to 25 mA	8.4	11	12.5	V
		V_{VM} = 10 V, I_{VCP} = 0 to 20 mA	6.3	9	10	
		V_{VM} = 8 V, I_{VCP} = 0 to 15 mA	5.4	7	8	
		V_{VM} = 6 V, I_{VCP} = 0 to 10 mA	4	5	6	
LOGIC-LEVEL INPUTS (CAL, ENABLE, INHx, INLx, nSCS, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			100		mV
I_{IL}	Input logic low current	V_{VIN} = 0 V	–5		5	µA
I_{IH}	Input logic high current	V_{VIN} = 5 V		50	70	µA
R_{PD}	Pulldown resistance	To AGND		100		kΩ
t_{PD}	Propagation delay	INHx/INLx transition to GHx/GLx transition		150		ns
FOUR-LEVEL H/W INPUTS (GAIN, MODE)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	45 kΩ ± 5% to tied AGND		1.2		V
V_{I3}	Input mode 3 voltage	Hi-Z		2		V
V_{I4}	Input mode 4 voltage	Tied to DVDD		3.3		V
R_{PU}	Pullup resistance	Internal pullup to DVDD		50		kΩ
R_{PD}	Pulldown resistance	Internal pulldown to AGND		84		kΩ
SEVEN-LEVEL H/W INPUTS (IDRIVE, VDS)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	18 kΩ ± 5% tied to AGND		0.5		V
V_{I3}	Input mode 3 voltage	75 kΩ ± 5% tied to AGND		1.1		V
V_{I4}	Input mode 4 voltage	Hi-Z		1.65		V
V_{I5}	Input mode 5 voltage	75 kΩ ± 5% tied to DVDD		2.2		V
V_{I6}	Input mode 6 voltage	18 kΩ ± 5% tied to DVDD		2.8		V
V_{I7}	Input mode 7 voltage	Tied to DVDD		3.3		V
R_{PU}	Pullup resistance	Internal pullup to DVDD		73		kΩ
R_{PD}	Pulldown resistance	Internal pulldown to AGND		73		kΩ
OPEN DRAIN OUTPUTS (nFAULT, SDO)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.1	V
I_{OZ}	Output high impedance leakage	V_O = 5 V	–2		2	µA

(1) Specified by design and characterization data

Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVERS (GHx, GLx)							
V_{GSH} (1)	High-side gate drive voltage w.r.t SHx		V_{VM} = 13 V, I_{VCP} = 0 to 25 mA	8.4	11	12.5	V
			V_{VM} = 10 , I_{VCP} = 0 to 20 mA	6.3	9	10	
			V_{VM} = 8 V, I_{VCP} = 0 to 15 mA	5.4	7	8	
			V_{VM} = 6 V, I_{VCP} = 0 to 10 mA	4	5	6	
V_{GSL} (1)	Low-side gate drive voltage w.r.t PGND		V_{VM} = 12 V, I_{VGLS} = 0 to 25 mA	9	11	12	V
			V_{VM} = 10 V, I_{VGLS} = 0 to 20 mA	7.5	9	10	
			V_{VM} = 8 V, I_{VGLS} = 0 to 15 mA	5.5	7	8	
			V_{VM} = 6 V, I_{VGLS} = 0 to 10 mA	4	5	6	
t_{DEAD}	Gate drive dead time	SPI Device	DEAD_TIME = 00b		50		ns
			DEAD_TIME = 01b		100		
			DEAD_TIME = 10b		200		
			DEAD_TIME = 11b		400		
		H/W Device			100		
t_{DRIVE}	Peak current gate drive time	SPI Device	TDRIVE = 00b		500		ns
			TDRIVE = 01b		1000		
			TDRIVE = 10b		2000		
			TDRIVE = 11b		4000		
		H/W Device			4000		
I_{DRIVEP}	Peak source gate current	SPI Device	IDRIVEP_HS or IDRIVEP_LS = 0000b		10		mA
			IDRIVEP_HS or IDRIVEP_LS = 0001b		30		
			IDRIVEP_HS or IDRIVEP_LS = 0010b		60		
			IDRIVEP_HS or IDRIVEP_LS = 0011b		80		
			IDRIVEP_HS or IDRIVEP_LS = 0100b		120		
			IDRIVEP_HS or IDRIVEP_LS = 0101b		140		
			IDRIVEP_HS or IDRIVEP_LS = 0110b		170		
			IDRIVEP_HS or IDRIVEP_LS = 0111b		190		
			IDRIVEP_HS or IDRIVEP_LS = 1000b		260		
			IDRIVEP_HS or IDRIVEP_LS = 1001b		330		
			IDRIVEP_HS or IDRIVEP_LS = 1010b		370		
			IDRIVEP_HS or IDRIVEP_LS = 1011b		440		
			IDRIVEP_HS or IDRIVEP_LS = 1100b		570		
			IDRIVEP_HS or IDRIVEP_LS = 1101b		680		
			IDRIVEP_HS or IDRIVEP_LS = 1110b		820		
			IDRIVEP_HS or IDRIVEP_LS = 1111b		1000		
		H/W Device	IDRIVE = Tied to AGND		10		
			IDRIVE = 18 kΩ ± 5% tied to AGND		30		
			IDRIVE = 75 kΩ ± 5% tied to AGND		60		
			IDRIVE = Hi-Z		120		
			IDRIVE = 75 kΩ ± 5% tied to DVDD		260		
			IDRIVE = 18 kΩ ± 5% tied to DVDD		570		
			IDRIVE = Tied to DVDD		1000		

Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEN}	Peak sink gate current	SPI Device	IDRIVEN_HS or IDRIVEN_LS = 0000b		20		mA
			IDRIVEN_HS or IDRIVEN_LS = 0001b		60		
			IDRIVEN_HS or IDRIVEN_LS = 0010b		120		
			IDRIVEN_HS or IDRIVEN_LS = 0011b		160		
			IDRIVEN_HS or IDRIVEN_LS = 0100b		240		
			IDRIVEN_HS or IDRIVEN_LS = 0101b		280		
			IDRIVEN_HS or IDRIVEN_LS = 0110b		340		
			IDRIVEN_HS or IDRIVEN_LS = 0111b		380		
			IDRIVEN_HS or IDRIVEN_LS = 1000b		520		
			IDRIVEN_HS or IDRIVEN_LS = 1001b		660		
			IDRIVEN_HS or IDRIVEN_LS = 1010b		740		
			IDRIVEN_HS or IDRIVEN_LS = 1011b		880		
			IDRIVEN_HS or IDRIVEN_LS = 1100b		1140		
			IDRIVEN_HS or IDRIVEN_LS = 1101b		1360		
			IDRIVEN_HS or IDRIVEN_LS = 1110b		1640		
			IDRIVEN_HS or IDRIVEN_LS = 1111b		2000		
		H/W Device	IDRIVE = Tied to AGND		20		
			IDRIVE = 18 kΩ ± 5% tied to AGND		60		
			IDRIVE = 75 kΩ ± 5% tied to AGND		120		
			IDRIVE = Hi-Z		240		
			IDRIVE = 75 kΩ ± 5% tied to DVDD		520		
			IDRIVE = 18 kΩ ± 5% tied to DVDD		1140		
			IDRIVE = Tied to DVDD		2000		
I_{HOLD}	Gate holding current		Source current after t_{DRIVE}		10		mA
			Sink current after t_{DRIVE}		50		
I_{STRONG}	Gate strong pulldown current		GHx to SHx and GLx to PGND		2		A
R_{OFF}	Gate hold off resistor		GHx to SHx and GLx to PGND		150		kΩ
CURRENT SHUNT AMPLIFIER (SNx, SOx, SPx, VREF)							
G_{CSA}	Amplifier gain	SPI Device	CSA_GAIN = 00b	4.85	5	5.15	V/V
			CSA_GAIN = 01b	9.7	10	10.3	
			CSA_GAIN = 10b	19.4	20	20.6	
			CSA_GAIN = 11b	38.8	40	41.2	
		H/W Device	GAIN = Tied to AGND	4.85	5	5.15	
			GAIN = 45 kΩ ± 5% tied to AGND	9.7	10	10.3	
			GAIN = Hi-Z	19.4	20	20.6	
			GAIN = Tied to DVDD	38.8	40	41.2	
t_{SET} (1)	Settling time to ±1%		V_{O_STEP} = 0.5 V, G_{CSA} = 5 V/V		150		ns
			V_{O_STEP} = 0.5 V, G_{CSA} = 10 V/V		300		
			V_{O_STEP} = 0.5 V, G_{VSA} = 20 V/V		600		
			V_{O_STEP} = 0.5 V, G_{CSA} = 40 V/V		1200		
V_{COM}	Common mode input range			–0.15		0.15	V
V_{DIFF}	Differential mode input range			–0.3		0.3	V
V_{OFF}	Input offset error		V_{SP} = V_{SN} = 0 V, CAL = 3.3 V, VREF = 3.3 V	–4		4	mV
V_{DRIFT} (1)	Drift offset		V_{SP} = V_{SN} = 0 V		10		µV/°C
V_{LINEAR}	SOx output voltage linear range			0.25		V_{VREF} – 0.25	V

Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BIAS}	SOx output voltage bias	SPI Device	V_{SP} = V_{SN} = 0 V, CAL = 3.3 V, VREF_DIV = 0b		V_{VREF} – 0.3		V
			V_{SP} = V_{SN} = 0 V, CAL = 3.3 V, VREF_DIV = 1b		V_{VREF} / 2		
		H/W Device	V_{SP} = V_{SN} = 0 V, CAL = 3.3 V		V_{VREF} / 2		
I_{BIAS}	SPx/SNx input bias current		VREF_DIV = 1b			100	µA
V_{SLEW} (1)	SOx output slew rate		60-pF load		10		V/µs
I_{VREF}	VREF input current		V_{VREF} = 5 V		2	3	mA
UGB (1)	Unity gain bandwidth		60-pF load		1		MHz
PROTECTION CIRCUITS							
V_{UVLO}	VM undervoltage lockout		VM falling, UVLO report	5.4	5.6	5.8	V
			VM rising, UVLO recovery	5.6	5.8	6	
V_{UVLO_HYS}	VM undervoltage hysteresis		Rising to falling threshold		200		mV
t_{UVLO_DEG}	VM undervoltage deglitch time		VM falling, UVLO report		10		µs
V_{CPUV}	Charge pump undervoltage lockout		VCP falling, CPUV report		V_{VM} + 2.8		V
V_{GS_CLAMP}	High-side gate clamp		Positive clamping voltage	15	16.5	18	V
			Negative clamping voltage		–0.7		
V_{VDS_OCP}	V_{DS} overcurrent trip voltage	SPI Device	VDS_LVL = 0000b		0.06		V
			VDS_LVL = 0001b		0.13		
			VDS_LVL = 0010b		0.2		
			VDS_LVL = 0011b		0.26		
			VDS_LVL = 0100b		0.31		
			VDS_LVL = 0101b		0.45		
			VDS_LVL = 0110b		0.53		
			VDS_LVL = 0111b		0.6		
			VDS_LVL = 1000b		0.68		
			VDS_LVL = 1001b		0.75		
			VDS_LVL = 1010b		0.94		
			VDS_LVL = 1011b		1.13		
			VDS_LVL = 1100b		1.3		
			VDS_LVL = 1101b		1.5		
			VDS_LVL = 1110b		1.7		
			VDS_LVL = 1111b		1.88		
		H/W Device	VDS = Tied to AGND		0.06		
			VDS = 18 kΩ ± 5% tied to AGND		0.13		
			VDS = 75 kΩ ± 5% tied to AGND		0.26		
			VDS = Hi-Z		0.6		
			VDS = 75 kΩ ± 5% tied to DVDD		1.13		
			VDS = 18 kΩ ± 5% tied to DVDD		1.88		
			VDS = Tied to DVDD		Disabled		
t_{OCP_DEG}	V_{DS} and V_{SENSE} overcurrent deglitch time	SPI Device	OCP_DEG = 00b		2		µs
			OCP_DEG = 01b		4		
			OCP_DEG = 10b		6		
			OCP_DEG = 11b		8		
		H/W Device			4		

Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SEN_OCP}	V_{SENSE} overcurrent trip voltage	SPI Device	SEN_LVL = 00b		0.25		V
			SEN_LVL = 01b		0.5		
			SEN_LVL = 10b		0.75		
			SEN_LVL = 11b		1		
		H/W Device			1		
t_{RETRY}	Overcurrent retry time	SPI Device	TRETRY = 0b		4		ms
			TRETRY = 1b		50		µs
		H/W Device			4		ms
T_{OTW} (1)	Thermal warning temperature		Die temperature, T_J	130	150	165	°C
T_{OTSD} (1)	Thermal shutdown temperature		Die temperature, T_J	150	170	185	°C
T_{HYS} (1)	Thermal hysteresis		Die temperature, T_J		20		°C
BUCK REGULATOR SUPPLY (VIN)							
I_{nSHDN}	Shutdown supply current		V_{nSHDN} = 0 V		1	3	µA
I_Q	Operating quiescent current		V_{VIN} = 12 V, no load; non-switching		28		µA
V_{VIN_UVLO}	VIN undervoltage lockout threshold		VIN Rising			4	V
			VIN Falling	3			
BUCK REGULATOR SHUTDOWN (nSHDN)							
V_{nSHDN_TH}	Rising nSHDN threshold			1.05	1.25	1.38	V
I_{nSHDN}	Input current		V_{nSHDN} = 2.3 V		–4.2		µA
			V_{nSHDN} = 0.9 V		–1		
I_{nSHDN_HYS}	Hysteresis current				–3		µA
BUCK REGULATOR HIGH-SIDE MOSFET							
R_{DS_ON}	MOSFET on resistance		V_{VIN} = 12 V, V_{CB} to V_{SW} = 5.8 V, T_A = 25°C		900		mΩ
BUCK REGULATOR VOLTAGE REFERENCE (FB)							
V_{FB}	Feedback voltage			0.747	0.765	0.782	V
BUCK REGULATOR CURRENT LIMIT							
I_{LIMIT}	Peak current limit		V_{VIN} = 12 V, T_A = 25°C		1200		mA
						1700	
BUCK REGULATOR SWITCHING (SW)							
f_{SW}	Switching frequency			595	700	805	kHz
D_{MAX}	Maximum duty cycle				96%		
BUCK REGULATOR THERMAL SHUTDOWN							
T_{SHDN} (1)	Thermal shutdown threshold				170		°C
T_{HYS} (1)	Thermal shutdown hysteresis				10		°C

7.6 SPI Timing Requirements(1)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SPI (nSCS, SCLK, SDI, SDO)						
t_{READY}	SPI ready after enable	VM > UVLO, ENABLE = 3.3 V			1	ms
t_{CLK}	SCLK minimum period		100			ns
t_{CLKH}	SCLK minimum high time		50			ns
t_{CLKL}	SCLK minimum low time		50			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{H_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time	SCLK high to SDO valid			30	ns
t_{SU_nSCS}	nSCS input setup time		50			ns
t_{H_nSCS}	nSCS input hold time		50			ns
t_{HI_nSCS}	nSCS minimum high time before active low		400			ns
t_{DIS_nSCS}	nSCS disable time	nSCS high to SDO high impedance		10		ns

(1) Specified by design and characterization data

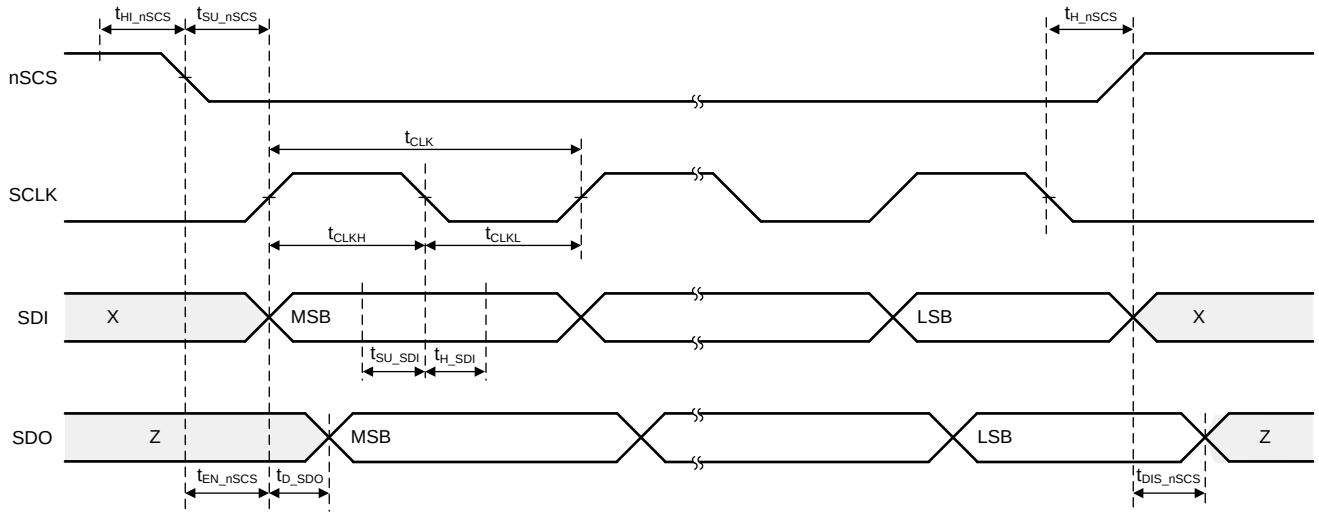


Figure 1. SPI Slave Mode Timing Diagram

7.7 Typical Characteristics

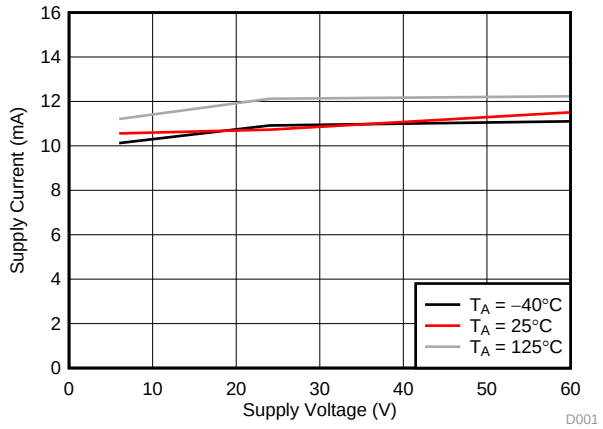


Figure 2. Supply Current Over VM

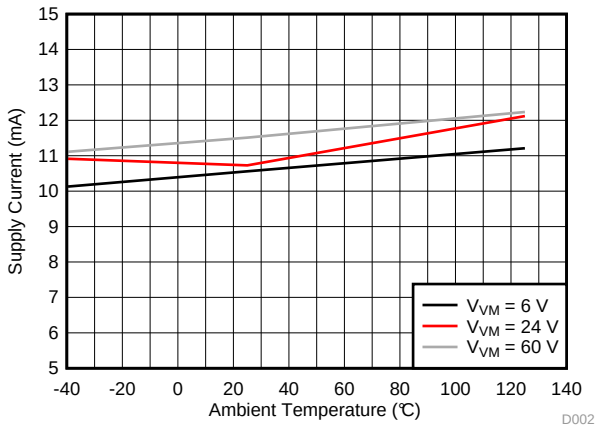


Figure 3. Supply Current Over Temperature

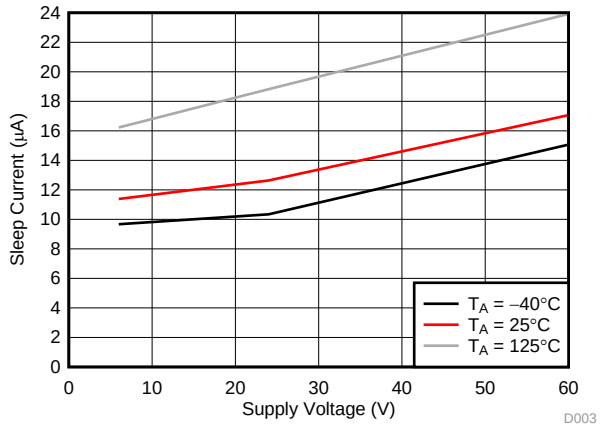


Figure 4. Sleep Current Over VM

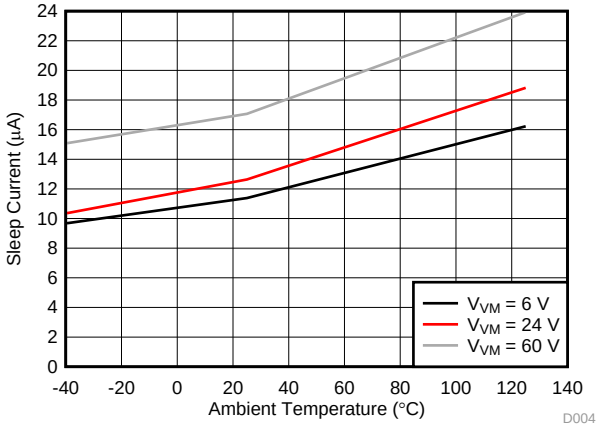


Figure 5. Sleep Current Over Temperature

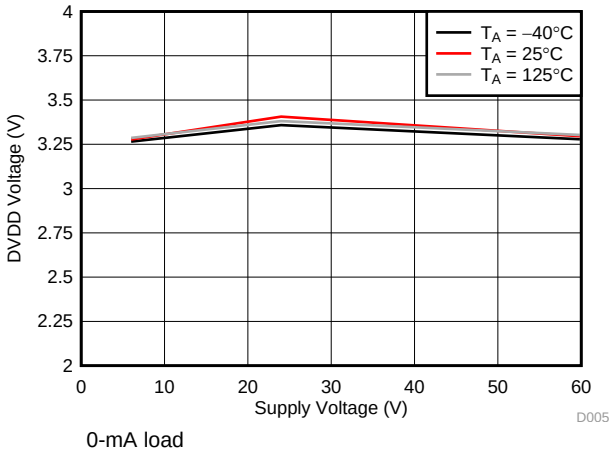


Figure 6. DVDD Voltage Over VM

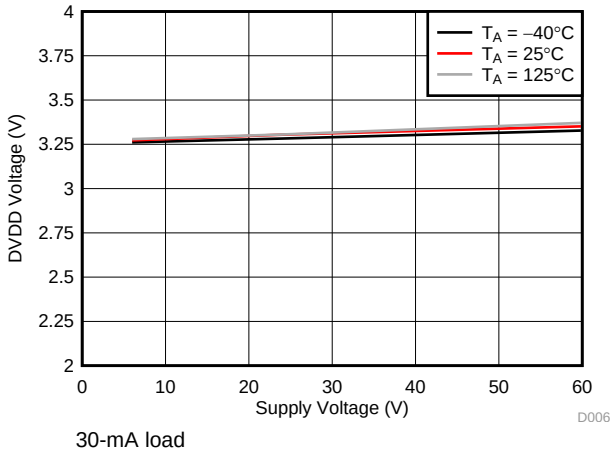


Figure 7. DVDD Voltage Over VM

Typical Characteristics (continued)

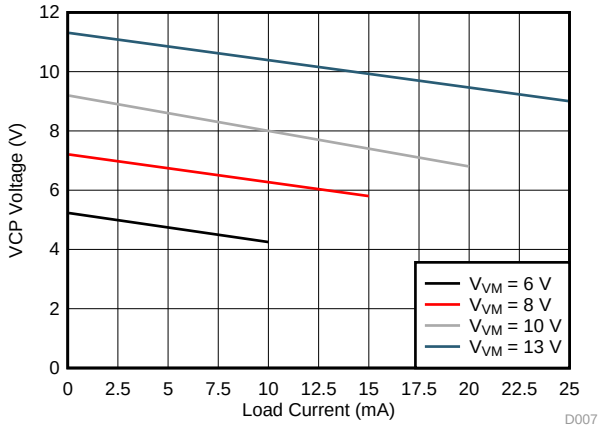
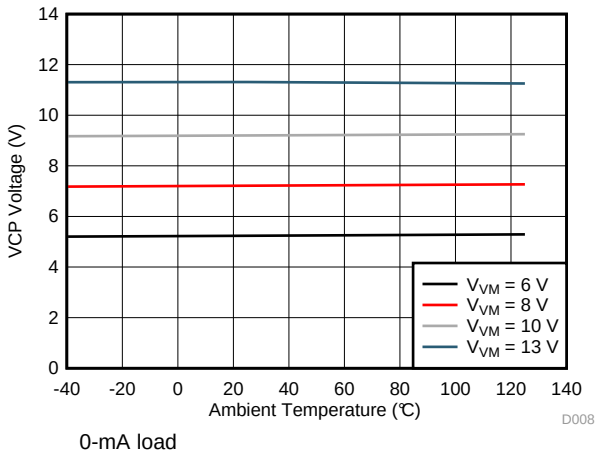


Figure 8. VCP Voltage Over Load



0-mA load

Figure 9. VCP Voltage Over Temperature

8 Detailed Description

8.1 Overview

The DRV832x family of devices are integrated 6 to 60-V gate drivers for three-phase motor drive applications. These devices reduce system component count, cost, and complexity by integrating three independent half-bridge gate drivers, charge pump and linear regulator for the high-side and low-side gate driver supply voltages, optional triple current shunt amplifiers, and an optional 600-mA buck regulator. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1-A source, 2-A sink peak currents with a 25-mA average output current. The high-side gate drive supply voltage is generated using a doubler charge-pump architecture that regulates the VCP output to V_{VM} + 11 V. The low-side gate drive supply voltage is generated using a linear regulator from the VM power supply that regulates to 11 V. A smart gate-drive architecture provides the ability to dynamically adjust the output gate-drive current strength allowing for the gate driver to control the power MOSFET V_{DS} switching speed. This allows for the removal of external gate drive resistors and diodes reducing BOM component count, cost, and PCB area. The architecture also uses an internal state machine to protect against gate-drive short-circuit events, control the half-bridge dead time, and protect against dV/dt parasitic turnon of the external power MOSFET.

The DRV8323 and DRV8323R devices integrate three, bidirectional current-shunt amplifiers for monitoring the current level through each of the external half-bridges using a low-side shunt resistor. The gain setting of the shunt amplifier can be adjusted through the SPI or hardware interface with the SPI providing additional flexibility to adjust the output bias point.

The DRV8320R and DRV8323R devices integrate a 600-mA buck regulator that can be used to power an external controller or other logic circuits. The buck regulator is implemented as a separate internal die that can use either the same or a different power supply from the gate driver.

In addition to the high level of device integration, the DRV832x family of devices provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), V_{DS} overcurrent monitoring (OCP), gate-driver short-circuit detection (GDF), and overtemperature shutdown (OTW/OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The DRV832x family of devices are available in 0.5-mm pin pitch, QFN surface-mount packages. The QFN sizes are 5 × 5 mm for the 32-pin package, 6 × 6 mm for the 40-pin package, and 7 × 7 mm for the 48-pin package.

8.2 Functional Block Diagram

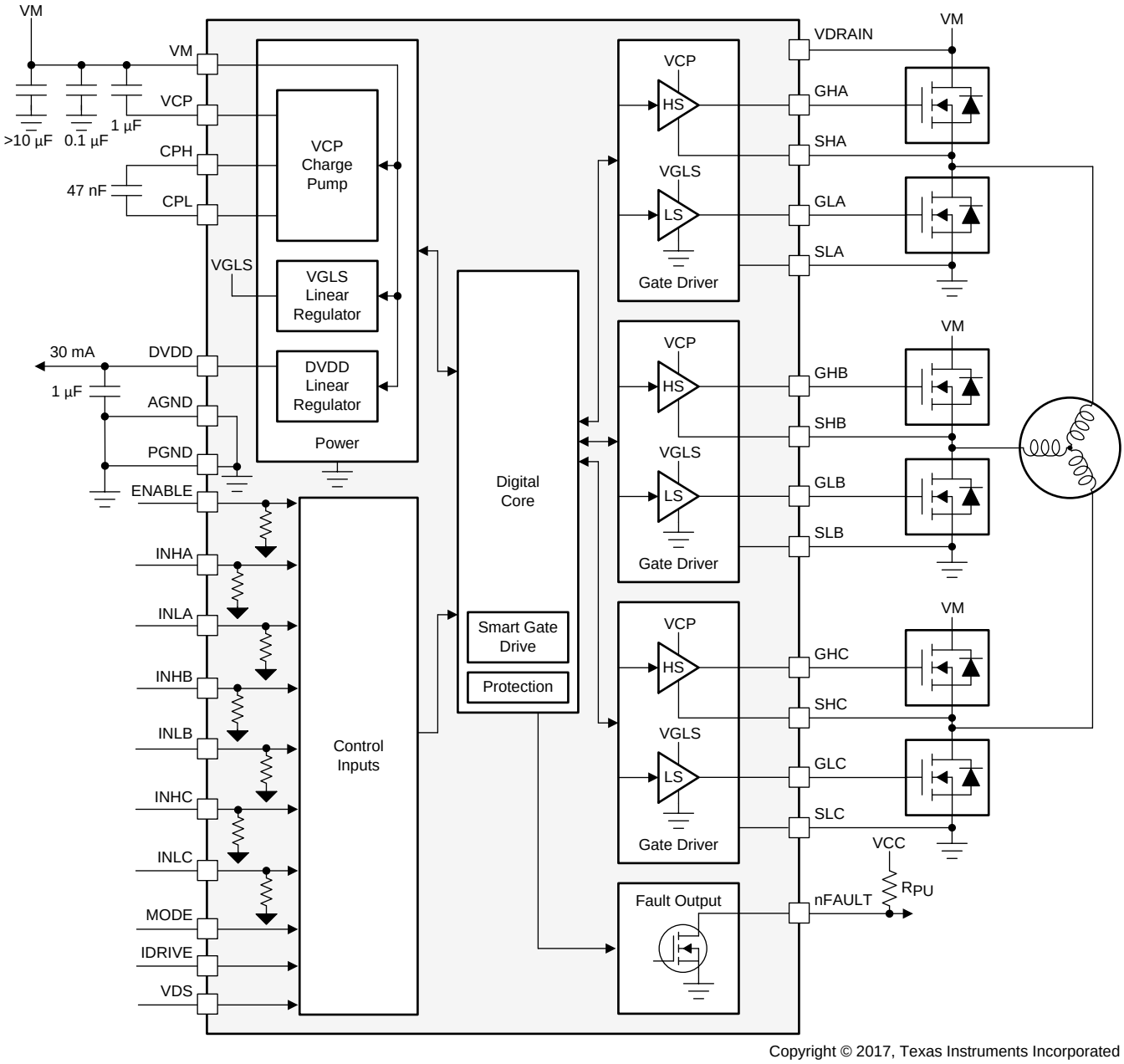


Figure 10. Block Diagram for DRV8320H

Functional Block Diagram (continued)

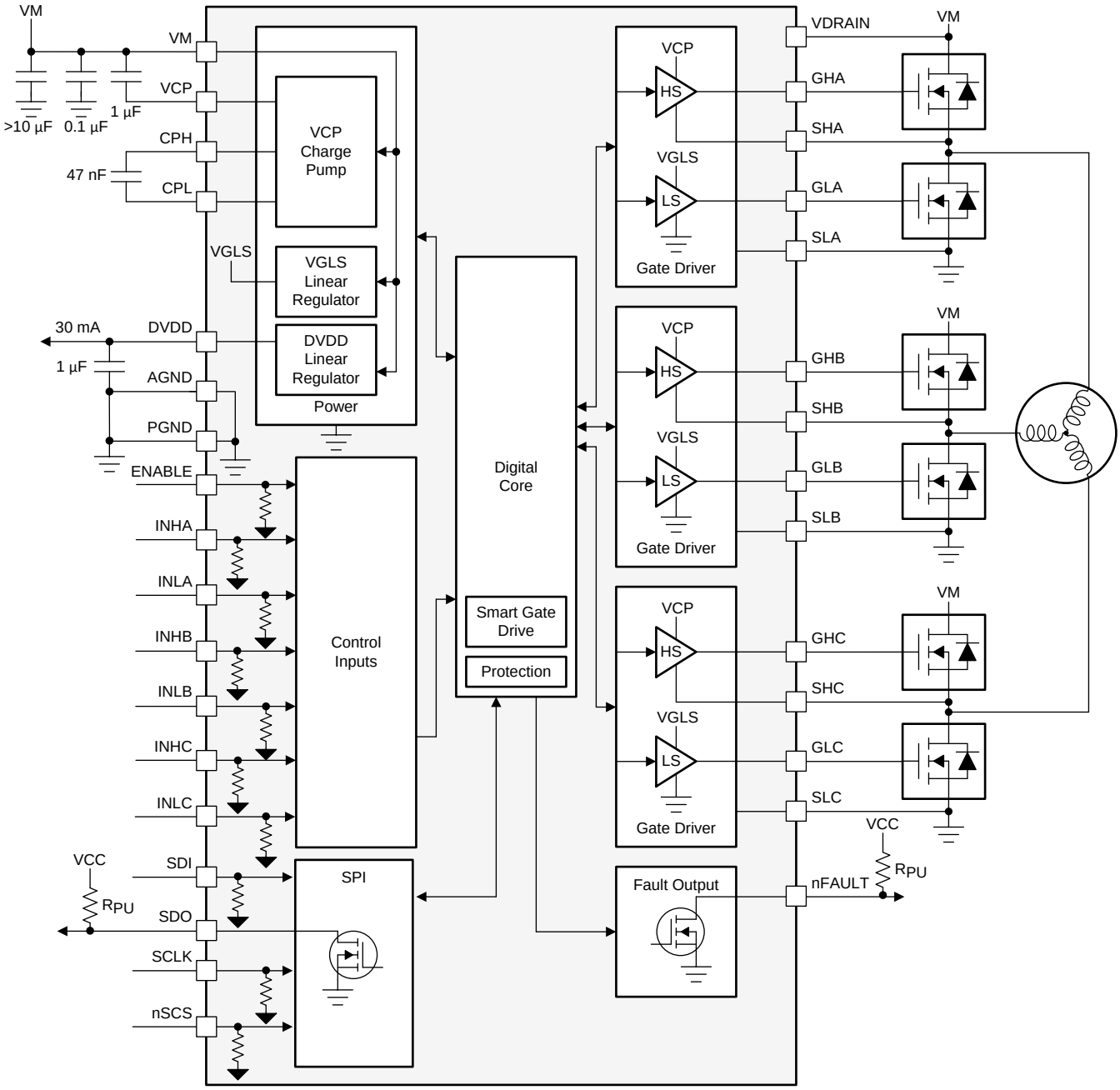


Figure 11. Block Diagram for DRV8320S

Functional Block Diagram (continued)

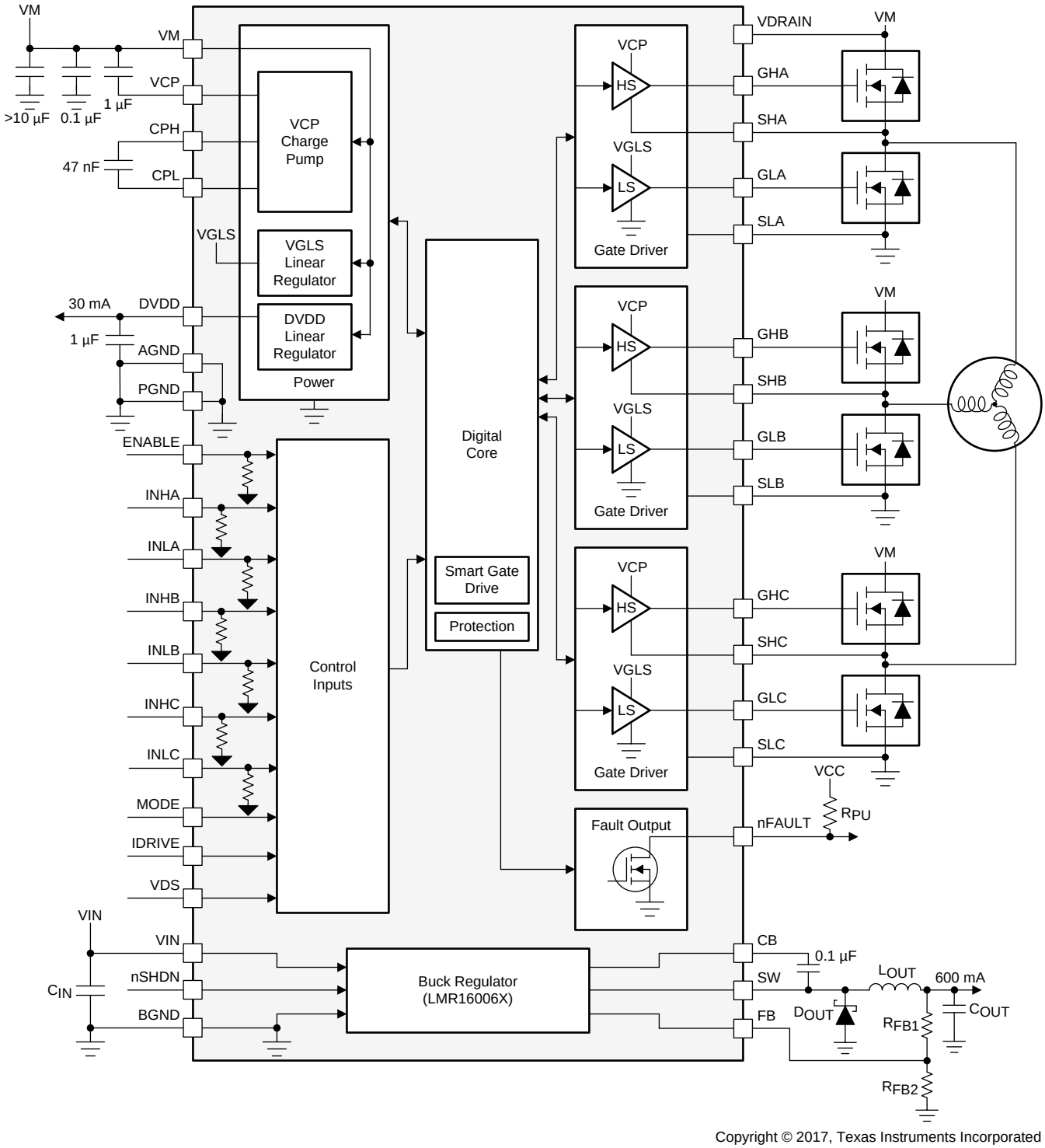


Figure 12. Block Diagram for DRV8320RH

Functional Block Diagram (continued)

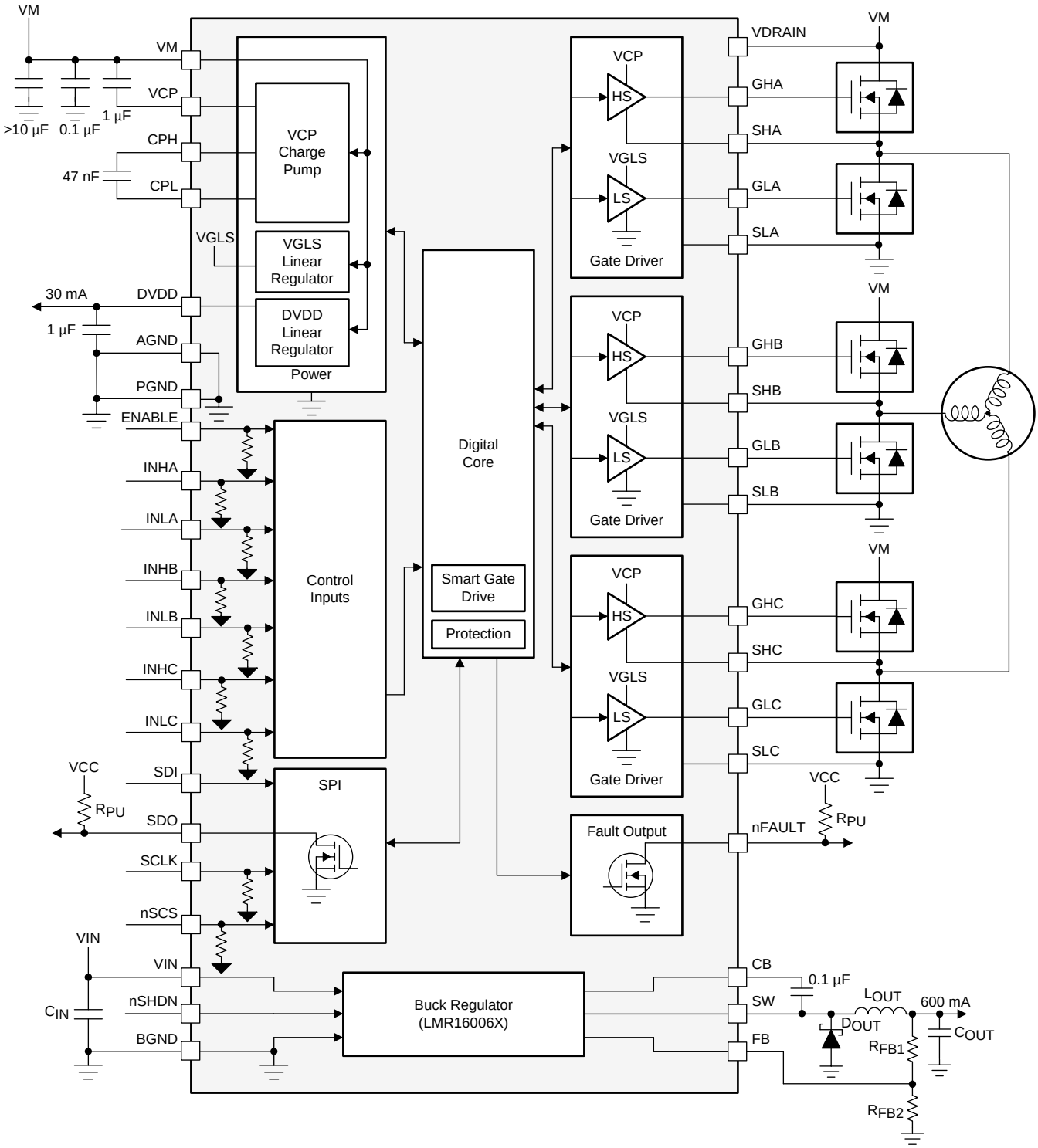


Figure 13. Block Diagram for DRV8320RS

Functional Block Diagram (continued)

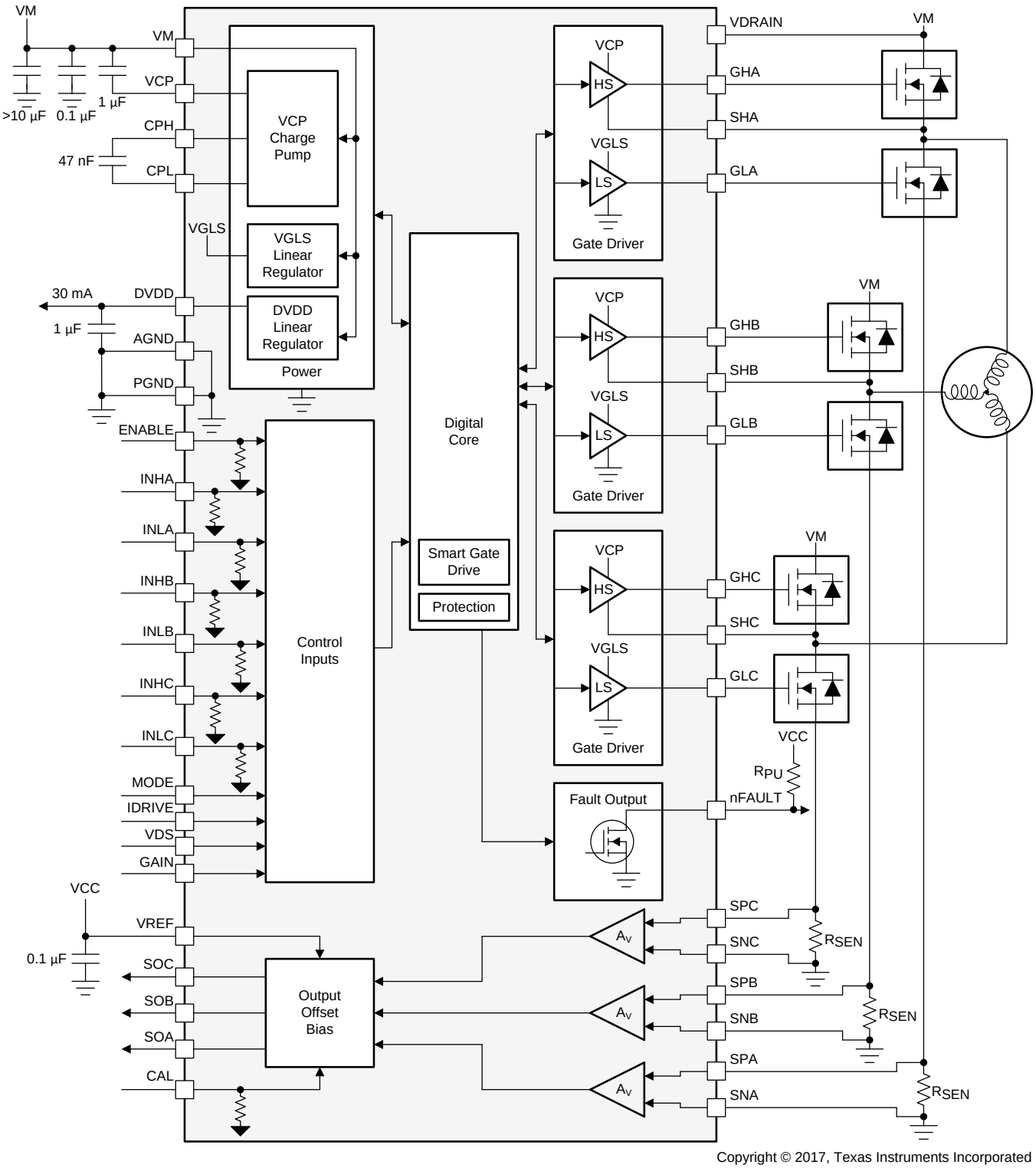


Figure 14. Block Diagram for DRV8323H

Functional Block Diagram (continued)

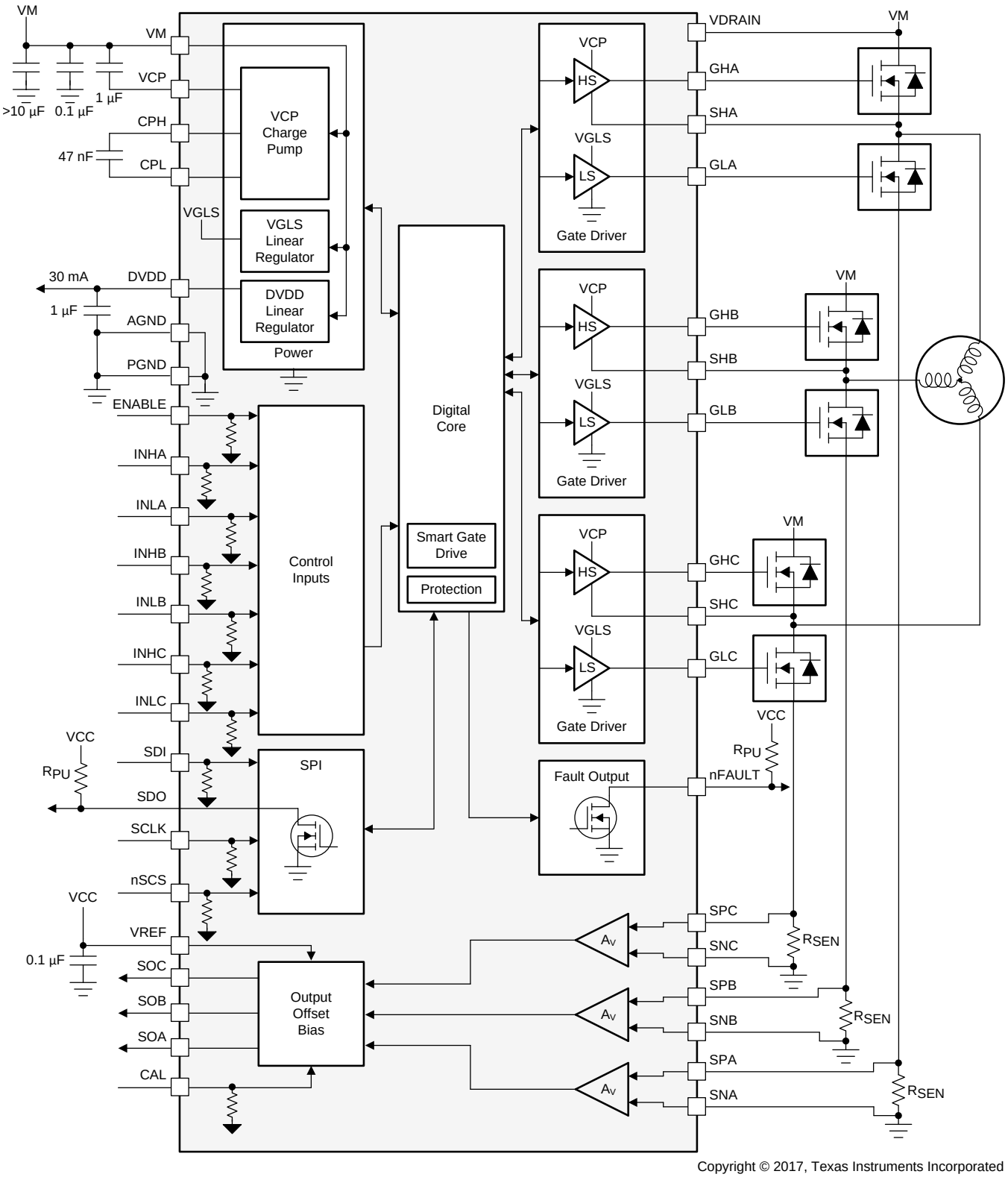


Figure 15. Block Diagram for DRV8323S

Functional Block Diagram (continued)

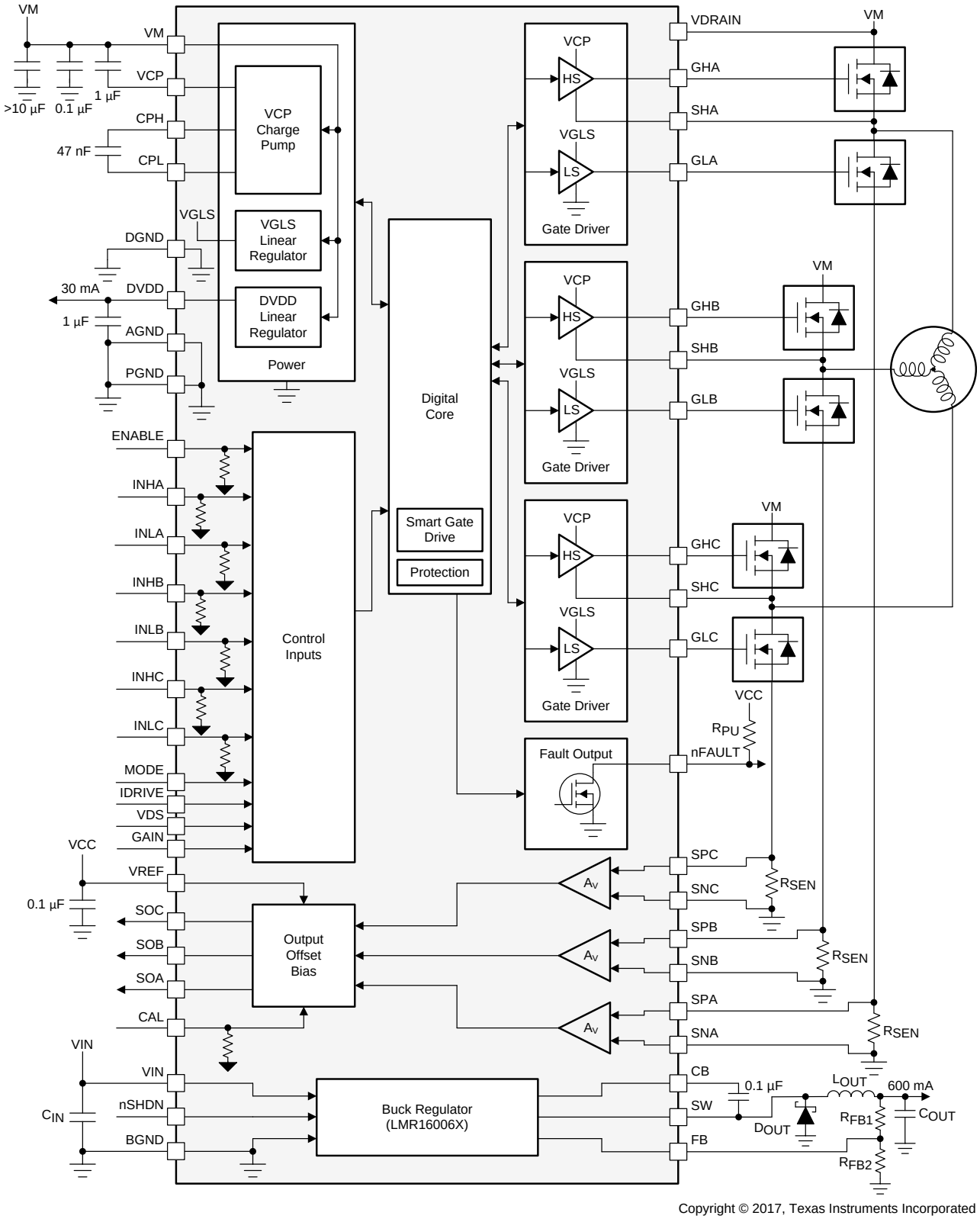


Figure 16. Block Diagram for DRV8323RH

Functional Block Diagram (continued)

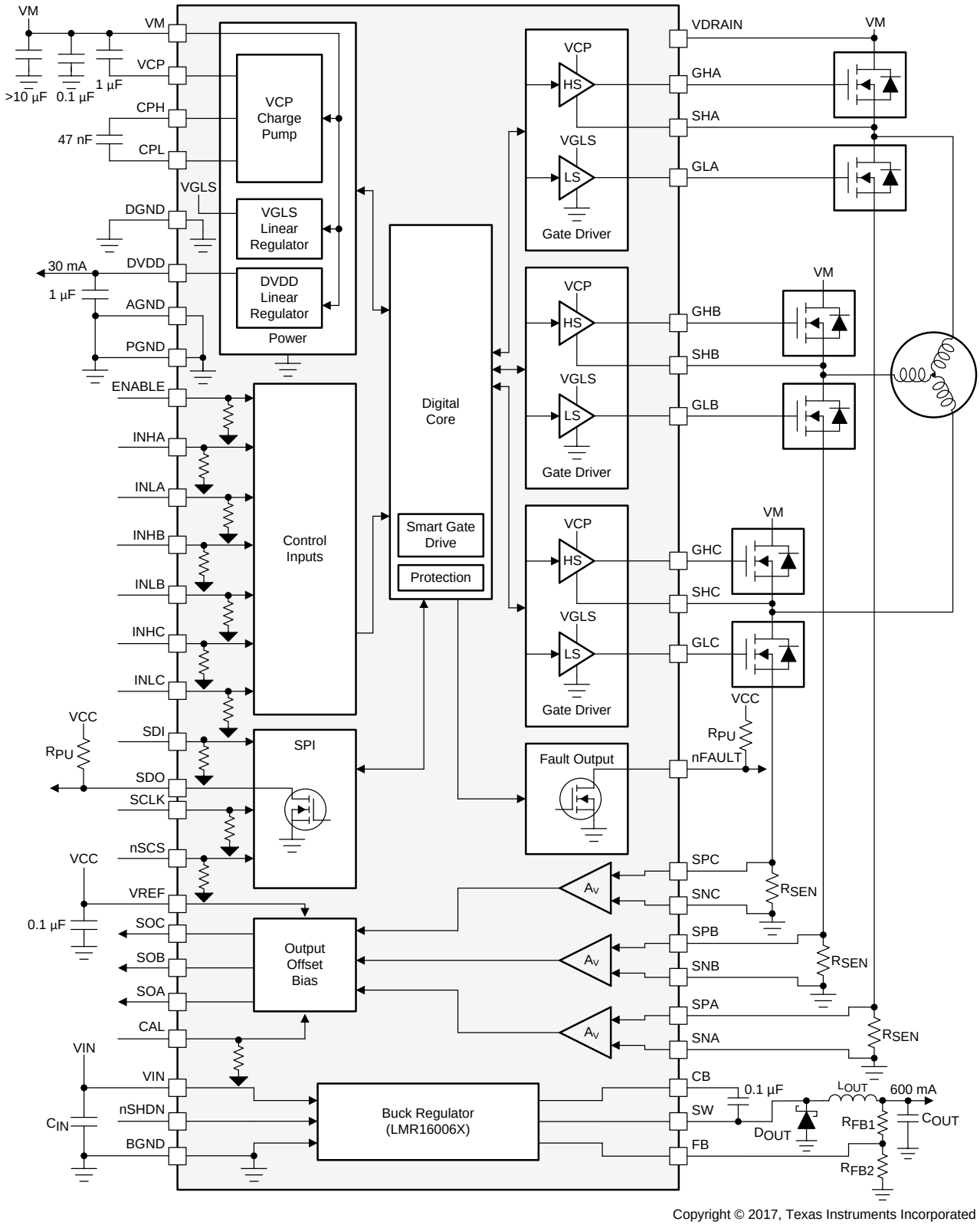


Figure 17. Block Diagram for DRV8323RS

8.3 Feature Description

Table 1 lists the recommended values of the external components for the gate driver. Table 2 lists the recommended values of the external components for the buck regulator.

Table 1. DRV832x Gate-Driver External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, VM-rated capacitor
C_{VM2}	VM	PGND	≥ 10 µF, VM-rated capacitor
C_{VCP}	VCP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{SW}	CPH	CPL	X5R or X7R, 47-nF, VM-rated capacitor
C_{DVDD}	DVDD	AGND	X5R or X7R, 1-µF, 6.3-V capacitor
R_{nFAULT}	VCC(1)	nFAULT	Pullup resistor
R_{SDO}	VCC(1)	SDO	Pullup resistor
R_{IDRIVE}	IDRIVE	AGND or DVDD	DRV832x hardware interface
R_{VDS}	VDS	AGND or DVDD	DRV832x hardware interface
R_{MODE}	MODE	AGND or DVDD	DRV832x hardware interface
R_{GAIN}	GAIN	AGND or DVDD	DRV832x hardware interface
C_{VREF}	VREF	AGND or DGND	Optional capacitor rated for VREF
R_{ASENSE}	SPA	SNA and PGND	Sense shunt resistor
R_{BSENSE}	SPB	SNB and PGND	Sense shunt resistor
R_{CSENSE}	SPC	SNC and PGND	Sense shunt resistor

(1) The VCC pin is not a pin on the DRV832x family of devices, but a VCC supply voltage pullup is required for the open-drain output nFAULT and SDO. These pins can also be pulled up to DVDD.

Table 2. DRV832xR Buck Regulator External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VIN}	VIN	BGND	X5R or X7R, 1 to 10 µF, VM-rated capacitor
C_{BOOT}	SW	CB	X5R or X7R, 0.1-µF, 16-V capacitor
D_{SW}	SW	BGND	Schottky diode
L_{SW}	SW	OUT(1)	Output inductor
C_{OUT}	OUT(1)	BGND	X5R or X7R, OUT rated capacitor
R_{FB1}	OUT(1)	FB	Resistor divider to set buck output voltage
R_{FB2}	FB	BGND	

(1) The OUT pin is not a pin on the DRV8320R and DRV8323R devices, but is the regulated output voltage of the buck regulator after the output inductor.

8.3.1 Three Phase Smart Gate Drivers

The DRV832x family of devices integrates three, half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A doubler charge pump provides the proper gate bias voltage to the high-side MOSFET across a wide operating voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

The DRV832x family of devices implements a smart gate-drive architecture which allows the user to dynamically adjust the gate drive current without requiring external gate current limiting resistors. Additionally, this architecture provides a variety of protection features for the external MOSFETs including automatic dead-time insertion, parasitic dV/dt gate turnon prevention, and gate-fault detection.

8.3.1.1 PWM Control Modes

The DRV832x family of devices provides four different PWM control modes to support various commutation and control methods. Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs. Set all INHx and INLx pins to logic low before making a MODE or PWM_MODE change.

8.3.1.1.1 6x PWM Mode (PWM_MODE = 00b or MODE Pin Tied to AGND)

In this mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in Table 3.

Table 3. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

8.3.1.1.2 3x PWM Mode (PWM_MODE = 01b or MODE Pin = 47 kΩ to AGND)

In this mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to change the half-bridge to high impedance. If the high-impedance (Hi-Z) sate is not required, tie all INLx pins logic high. The corresponding INHx and INLx signals control the output state as listed in Table 4.

Table 4. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

8.3.1.1.3 1x PWM Mode (PWM_MODE = 10b or MODE Pin = Hi-Z)

In this mode, the DRV832x family of devices uses 6-step block commutation tables that are stored internally. This feature allows for a three-phase BLDC motor to be controlled using a single PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to hall sensor digital outputs from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode normally operates with synchronous rectification, however it can be configured to use asynchronous diode freewheeling rectification on SPI devices. This configuration is set using the 1PWM_COM bit through the SPI registers.

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when hall sensors are directly controlling the INLA, INHB, and INLB state inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled low. This brake is independent of the states of the other input pins. Tie the INLC pin high if this feature is not required.

Table 5. Synchronous 1x PWM Mode

LOGIC AND HALL INPUTS							GATE-DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

Table 6. Asynchronous 1x PWM Mode 1PWM_COM = 1 (SPI Only)

LOGIC AND HALL INPUTS							GATE-DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

Figure 18 and Figure 19 show the different possible configurations in 1x PWM mode.

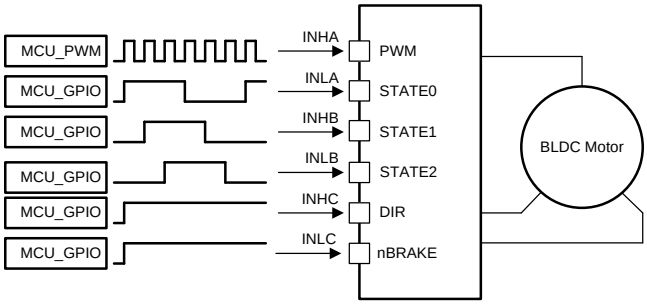


Figure 18. 1x PWM—Simple Controller

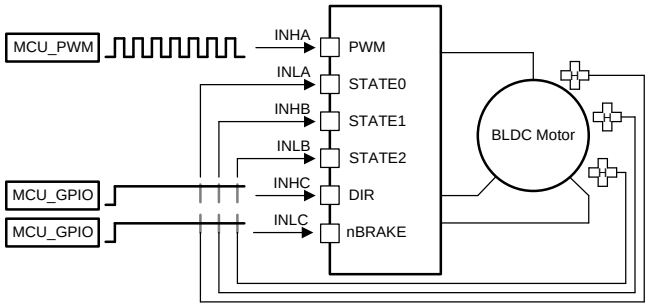


Figure 19. 1x PWM—Hall Sensor

8.3.1.1.4 Independent PWM Mode (PWM_MODE = 11b or MODE Pin Tied to DVDD)

In this mode, the corresponding input pin independently controls each high-side and low-side gate driver. This control mode allows for the DRV832x family of devices to drive separate high-side and low-side loads with each half-bridge. These types of loads include unidirectional brushed DC motors, solenoids, and low-side and high-side switches. In this mode, if the system is configured in a half-bridge configuration, simultaneously turning on both the high-side and low-side MOSFETs causes shoot-through.

Table 7. Independent PWM Mode Truth Table

INLx	INHx	GLx	GHx
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

Because the high-side and low-side V_{DS} overcurrent monitors share the SHx sense line, using the monitors if both the high-side and low-side gate drivers of one half-bridge are split and being used is not possible. In this case, connect the SHx pin to the high-side driver and disable the V_{DS} overcurrent monitors as shown in Figure 20.

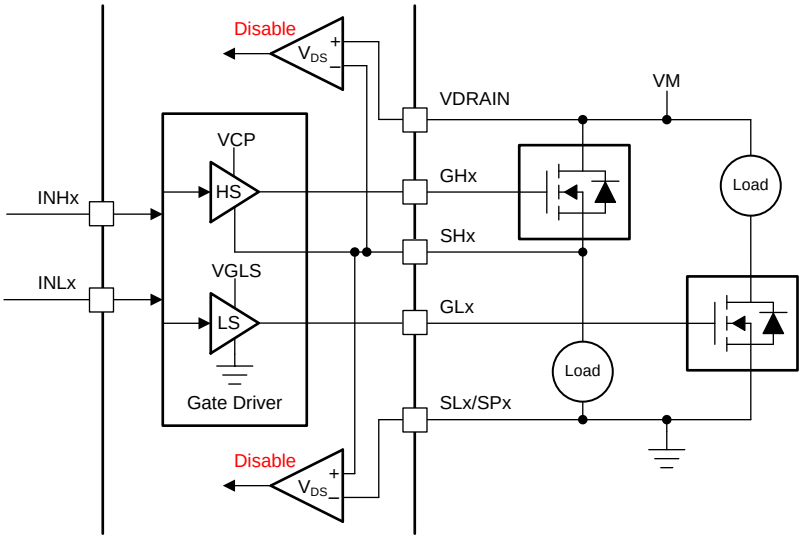


Figure 20. Independent PWM High-Side and Low-Side Drivers

If the half-bridge is used to implement only a high-side or low-side driver, using the V_{DS} overcurrent monitors is still possible. Connect the SHx pin as shown in Figure 21 or Figure 22. The unused gate driver and the corresponding input can be left disconnected.

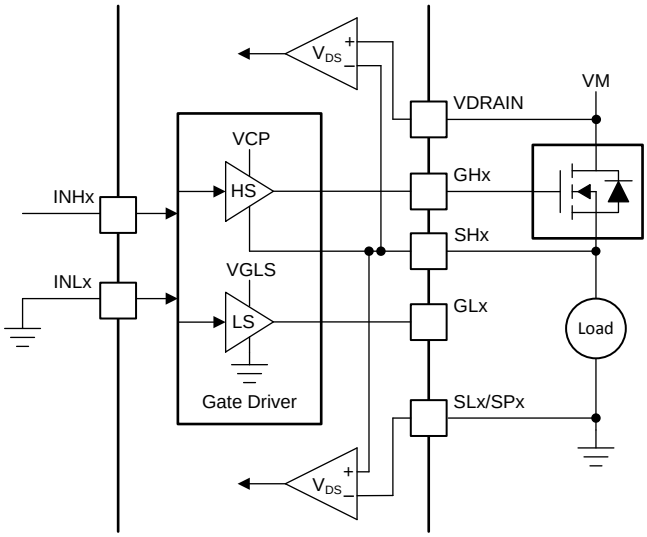


Figure 21. Single High-Side Driver

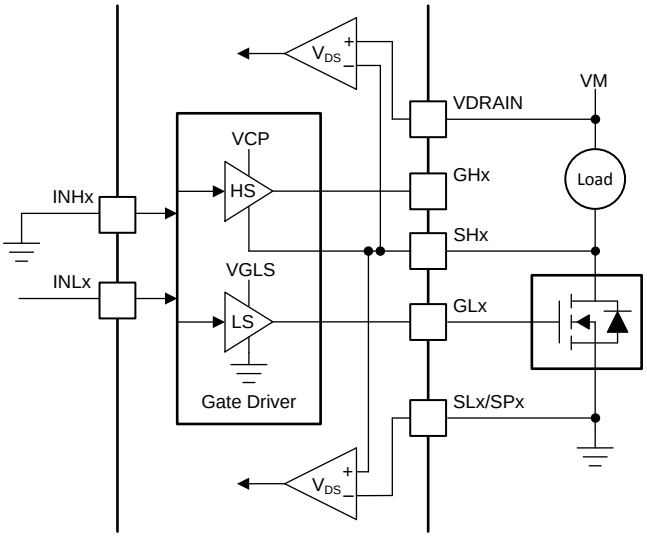


Figure 22. Single Low-Side Driver

8.3.1.2 Device Interface Modes

The DRV832x family of devices supports two different interface modes (SPI and hardware) to allow the end application to design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin to pin compatible. This allows for application designers to evaluate with one interface version and potentially switch to another with minimal modifications to their design.

8.3.1.2.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that allows for an external controller to send and receive data with the DRV832x. This allows for the external controller to configure device settings and read detailed fault information. The interface is a four wire interface utilizing the SCLK, SDI, SDO, and nSCS pins.

- The SCLK pin is an input which accepts a clock signal to determine when data is captured and propagated on SDI and SDO.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin uses an open-drain structure and requires an external pullup resistor.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV832x.

For more information on the SPI, see the *SPI Communication* section.

8.3.1.2.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor configurable inputs, GAIN, IDRIVE, MODE, and VDS. This allows for the application designer to configure the most commonly used device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The GAIN pin configures the current shunt amplifier gain.
- The IDRIVE pin configures the gate drive current strength.
- The MODE pin configures the PWM control mode.
- The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.

For more information on the hardware interface, see the *Pin Diagrams* section.

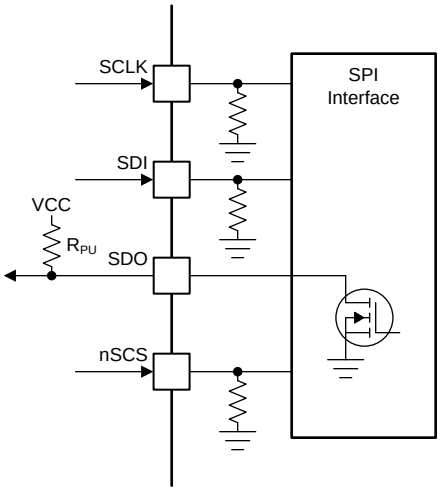


Figure 23. SPI

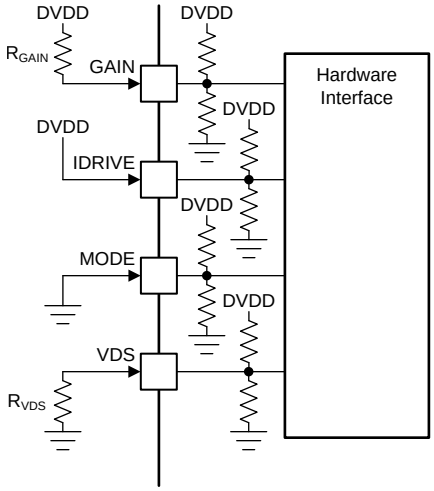


Figure 24. Hardware Interface

8.3.1.3 Gate Driver Voltage Supplies

The high-side gate-drive voltage supply is created using a doubler charge pump that operates from the VM voltage supply input. The charge pump allows the gate driver to properly bias the high-side MOSFET gate with respect to the source across a wide input supply voltage range. The charge pump is regulated to maintain a fixed output voltage of V_{VM} + 11 V and supports an average output current of 25 mA. When V_{VM} is less than 12 V, the charge pump operates in full doubler mode and generates $V_{VCP} = 2 \times V_{VM} – 1.5$ V when unloaded. The charge pump is continuously monitored for undervoltage to prevent under-driven MOSFET conditions. The charge pump requires a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VM and VCP pins to act as the storage capacitor. Additionally, a X5R or X7R, 47-nF, VM-rated ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

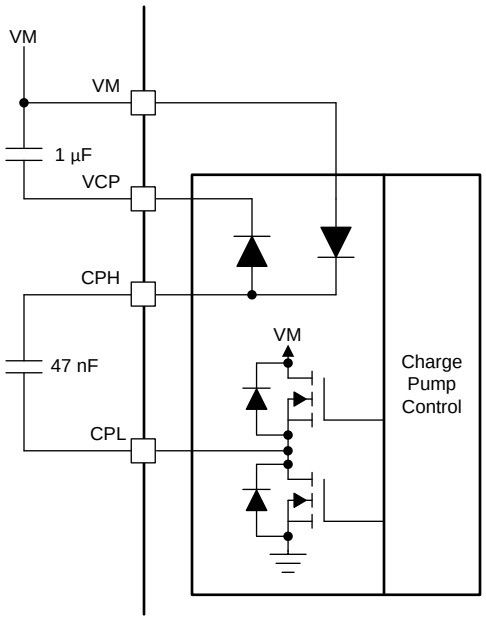


Figure 25. Charge Pump Architecture

The low-side gate drive voltage is created using a linear regulator that operates from the VM voltage supply input. The linear regulator allows the gate driver to properly bias the low-side MOSFET gate with respect to ground. The linear regulator output is fixed at 11 V and supports an output current of 25 mA.

8.3.1.4 Smart Gate Drive Architecture

The DRV832x gate drivers use an adjustable, complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates.

Additionally, the gate drivers use a smart gate-drive architecture to provide additional control of the external power MOSFETs, take additional steps to protect the MOSFETs, and allow for optimal tradeoffs between efficiency and robustness. This architecture is implemented through two components called IDRIVE and TDRIVE which are detailed in the *IDRIVE: MOSFET Slew-Rate Control* section and *TDRIVE: MOSFET Gate Drive Control* section. Figure 26 shows the high-level functional block diagram of the gate driver.

The IDRIVE gate-drive current and TDRIVE gate-drive time should be initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times (see the *Application and Implementation* section).

The high-side gate driver also implements a Zener clamp diode to help protect the external MOSFET gate from overvoltage conditions in the case of external short-circuit events on the MOSFET.

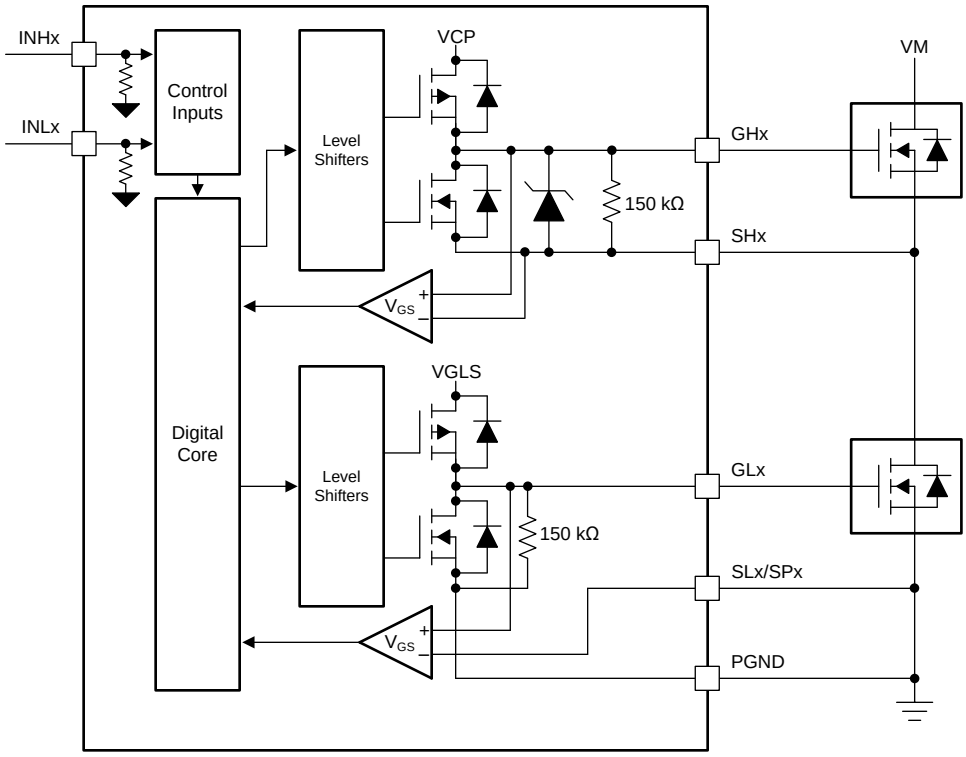


Figure 26. Gate Driver Block Diagram

8.3.1.4.1 IDRIVE: MOSFET Slew-Rate Control

The IDRIVE component implements adjustable gate-drive current to control the MOSFET V_{DS} slew rates. The MOSFET V_{DS} slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, dV/dt gate turnon leading to shoot-through, and switching voltage transients related to parasitics in the external half-bridge. IDRIVE operates on the principal that the MOSFET V_{DS} slew rates are predominately determined by the rate of gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By allowing the gate driver to adjust the gate current, it can effectively control the slew rate of the external power MOSFETs.

IDRIVE allows the DRV832x family of devices to dynamically switch between gate drive currents either through a register setting on SPI devices or the IDRIVE pin on hardware interface devices. The SPI devices provide 16 I_{DRIVE} settings ranging between 10-mA to 1-A source and 20-mA to 2-A sink. Hardware interface devices provides 7 I_{DRIVE} settings between the same ranges. The gate drive current setting is delivered to the gate during the turnon and turnoff of the external power MOSFET for the t_{DRIVE} duration. After the MOSFET turnon or turnoff, the gate driver switches to a smaller hold I_{HOLD} current to improve the gate driver efficiency. Additional details on the IDRIVE settings are described in the *Register Maps* section for the SPI devices and in the *Pin Diagrams* section for the hardware interface devices.

8.3.1.4.2 TDRIVE: MOSFET Gate Drive Control

The TDRIVE component is an integrated gate-drive state machine that provides automatic dead time insertion through switching handshaking, parasitic dV/dt gate turnon prevention, and MOSFET gate-fault detection.

The first component of the TDRIVE state machine is automatic dead-time insertion. Dead time is period of time between the switching of the external high-side and low-side MOSFETs to ensure that they do not cross conduct and cause shoot-through. The DRV832x family of devices uses V_{GS} voltage monitors to measure the MOSFET gate-to-source voltage and determine the proper time to switch instead of relying on a fixed time value. This feature allows the gate-driver dead time to adjust for variation in the system such a temperature drift and variation in the MOSFET parameters. An additional digital dead time (t_{DEAD}) can be inserted and is adjustable through the registers on SPI devices.

The second component focuses on parasitic dV/dt gate turnon prevention. To implement this, the TDRIVE state machine enables a strong pulldown I_{STRONG} current on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown last for the TDRIVE duration. This feature helps remove parasitic charge that couples into the MOSFET gate when the half-bridge switch-node voltage slews rapidly.

The third component implements a gate-fault detection scheme to detect pin-to-pin solder defects, a MOSFET gate failure, or a MOSFET gate stuck-high or stuck-low voltage condition. This implementation is done with a pair of V_{GS} gate-to-source voltage monitors for each half-bridge gate driver. When the gate driver receives a command to change the state of the half-bridge it begins to monitor the gate voltage of the external MOSFET. If at the end of the t_{DRIVE} period the V_{GS} voltage has not reached the proper threshold the gate driver will report a fault. To ensure that a false fault is not detected, a t_{DRIVE} time should be selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not increase the PWM time and will terminate if another PWM command is received while active. Additional details on the TDRIVE settings are described in the *Register Maps* section for SPI devices and in the *Pin Diagrams* section for hardware interface devices.

Figure 27 shows an example of the TDRIVE state machine in operation.

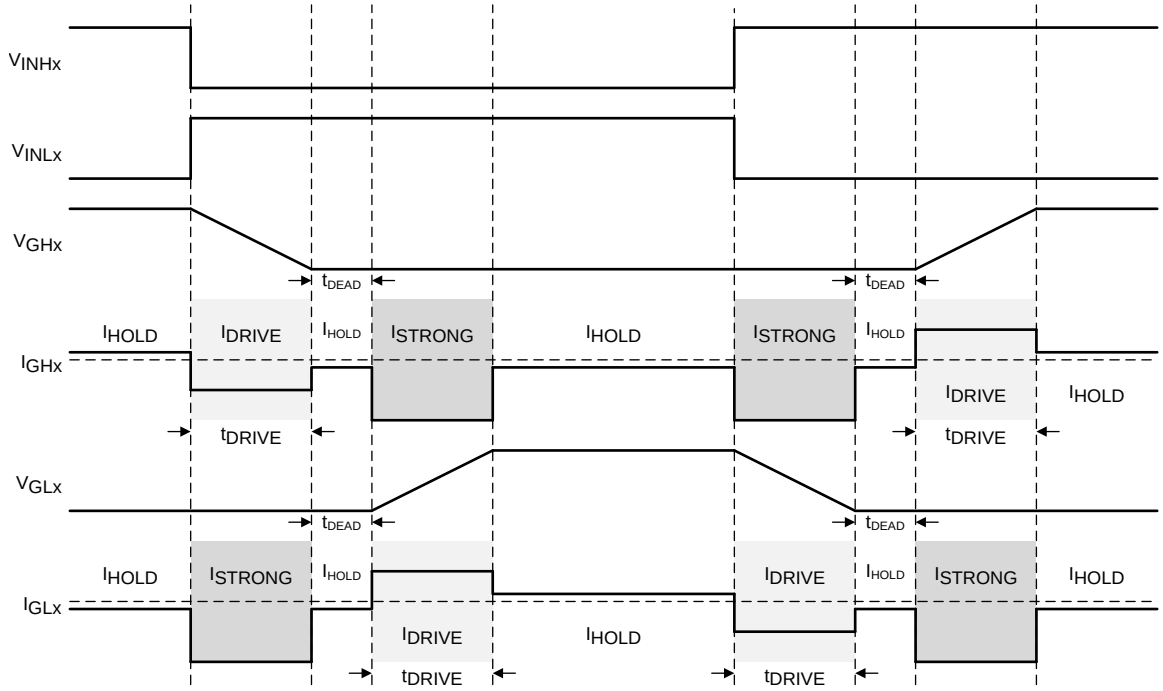


Figure 27. TDRIVE State Machine

8.3.1.4.3 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time comprises three parts consisting of the digital input deglitcher delay, the digital propagation delay, and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

8.3.1.4.4 MOSFET V_{DS} Monitors

The gate drivers implement adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. When the monitored voltage is greater than the V_{DS} trip point (V_{VDS_OCP}) for longer than the deglitch time (t_{OCP}), an overcurrent condition is detected and action is taken according to the device V_{DS} fault mode.

The high-side V_{DS} monitors measure the voltage between the VDRAIN and SHx pins. In devices with three current-shunt amplifiers (DRV8323 and DRV8323R), the low-side V_{DS} monitors measure the voltage between the SHx and SPx pins. If the current shunt amplifier is unused, tie the SP pins to the common ground point of the external half-bridges. On device options without the current shunt amplifiers (DRV8320 and DRV8320R) the low-side V_{DS} monitor measures between the SHx and SLx pins.

For the SPI devices, the low-side V_{DS} monitor reference point can be changed between the SPx and SNx pins if desired with the LS_REF register setting.

The V_{VDS_OCP} threshold is programmable between 0.06 V and 1.88 V. Additional information on the V_{DS} monitor levels are described in the *Register Maps* section for SPI devices and in the *Pin Diagrams* section hardware interface device.

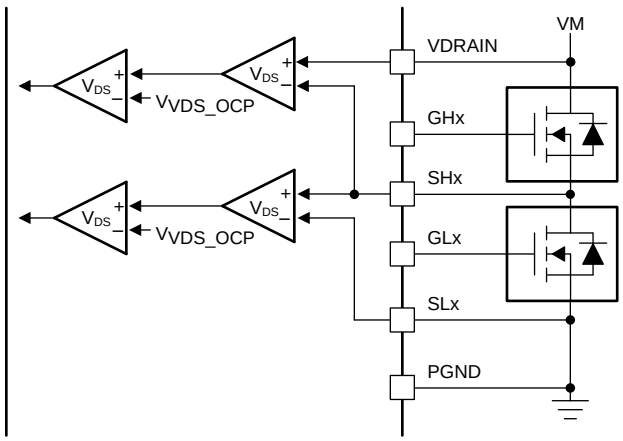


Figure 28. DRV8320 and DRV8320R V_{DS} Monitors

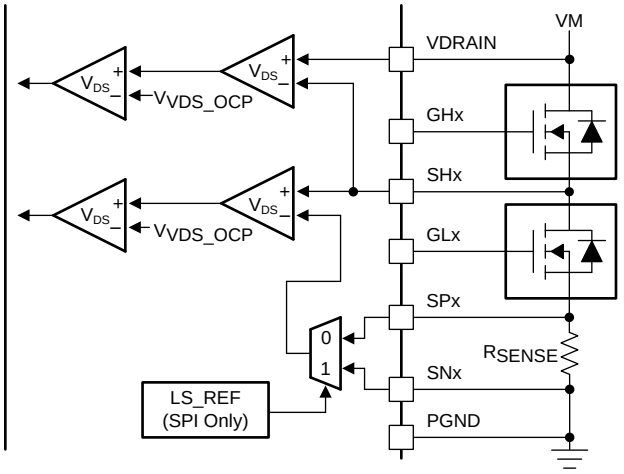


Figure 29. DRV8323 and DRV8323R V_{DS} Monitors

8.3.1.4.5 VDRAIN Sense Pin

The DRV832x family of devices provides a separate sense pin for the common point of the high-side MOSFET drain. This pin is called VDRAIN. This pin allows the sense line for the overcurrent monitors (VDRAIN) and the power supply (VM) to remain separate and prevent noise on the VDRAIN sense line. This separation also allows for a small filter to be implemented on the gate driver supply (VM) or to insert a boost converter to support lower voltage operation if desired. Care must still be taken when the filter or separate supply is designed because VM is still the reference point for the VCP charge pump that supplies the high-side gate drive voltage (V_{GSH}). The VM supply must not drift to far from the VDRAIN supply to avoid violating the V_{GS} voltage specification of the external power MOSFETs.

8.3.2 DVDD Linear Voltage Regulator

A 3.3-V, 30-mA linear regulator is integrated into the DRV832x family of devices and is available for use by external circuitry. This regulator can provide the supply voltage for a low-power microcontroller or other low-current supporting circuitry. The output of the DVDD regulator should be bypassed near the DVDD pin with a X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The DVDD nominal, no-load output voltage is 3.3 V. When the DVDD load current exceeds 30 mA, the regulator functions like a constant-current source. The output voltage drops significantly with a current load greater than 30 mA.

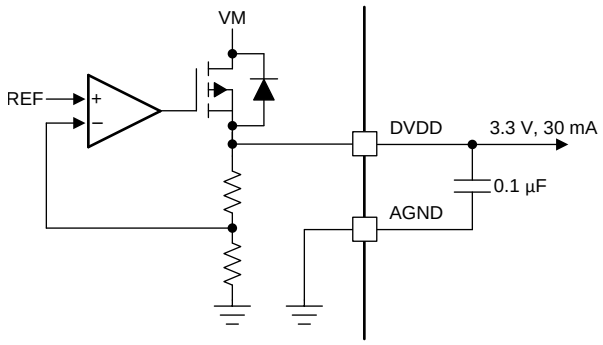


Figure 30. DVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device because of the DVDD linear regulator.

$$P = \left(V_{VM} - V_{DVDD}\right) \times I_{DVDD} \quad (1)$$

For example, at V_{VM} = 24 V, drawing 20 mA out of DVDD results in a power dissipation as shown in Equation 2.

$$P = \left(24\ V - 3.3\ V\right) \times 20\ mA = 414\ mW \quad (2)$$

8.3.3 Pin Diagrams

Figure 31 shows the input structure for the logic-level pins, INHx, INLx, CAL, ENABLE, nSCS, SCLK, and SDI. The input can be driven with a voltage or external resistor.

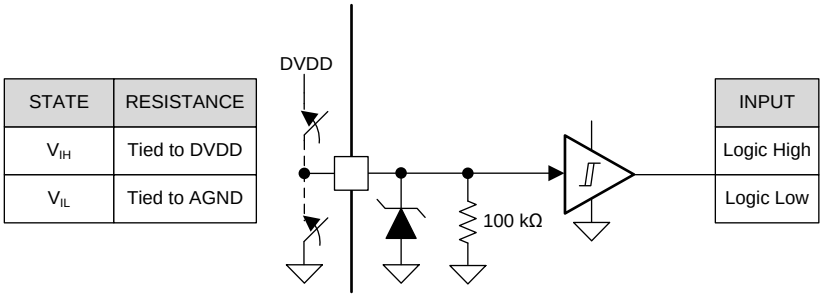
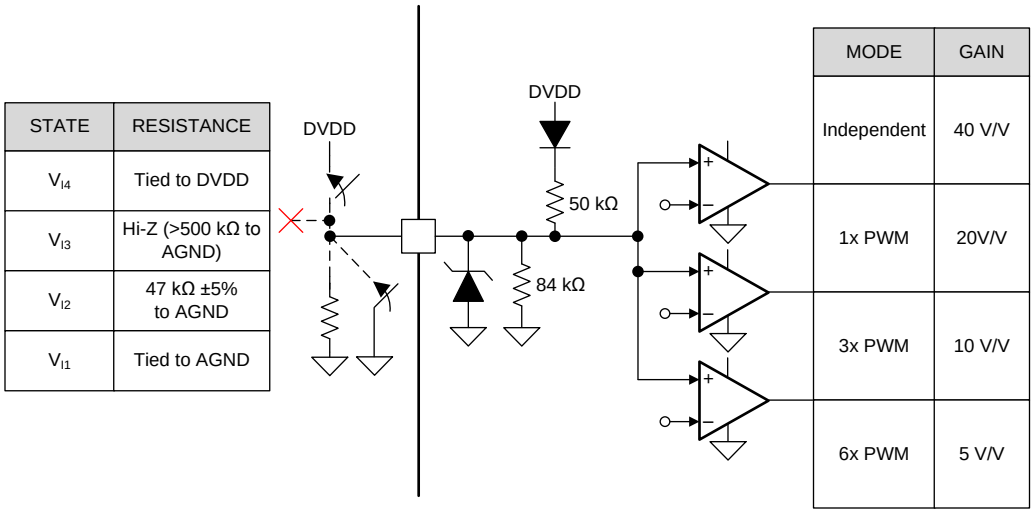


Figure 31. Logic-Level Input Pin Structure

Figure 32 shows the structure of the four level input pins, MODE and GAIN, on hardware interface devices. The input can be set with an external resistor.

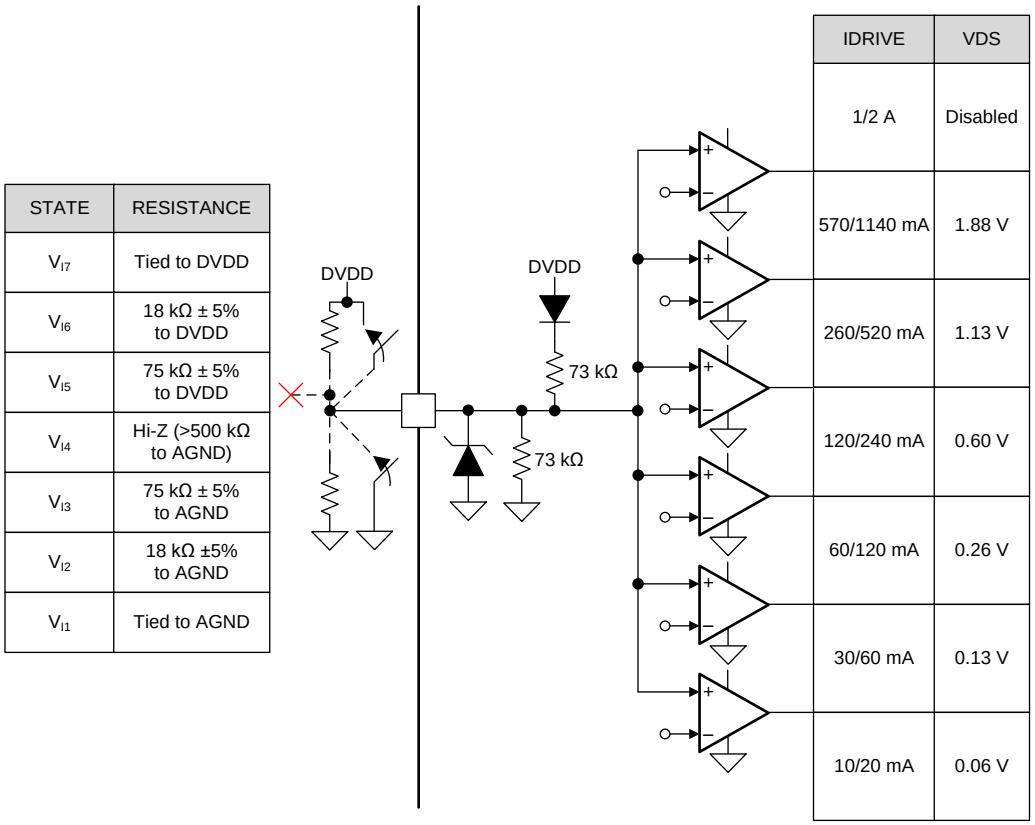


STATE	RESISTANCE
V_{I4}	Tied to DVDD
V_{I3}	Hi-Z (>500 kΩ to AGND)
V_{I2}	47 kΩ ±5% to AGND
V_{I1}	Tied to AGND

MODE	GAIN
Independent	40 V/V
1x PWM	20V/V
3x PWM	10 V/V
6x PWM	5 V/V

Figure 32. Four Level Input Pin Structure

Figure 33 shows the structure of the seven level input pins, IDRIVE and VDS, on hardware interface devices. The input can be set with an external resistor.



STATE	RESISTANCE
V_{I7}	Tied to DVDD
V_{I6}	18 kΩ ± 5% to DVDD
V_{I5}	75 kΩ ± 5% to DVDD
V_{I4}	Hi-Z (>500 kΩ to AGND)
V_{I3}	75 kΩ ± 5% to AGND
V_{I2}	18 kΩ ±5% to AGND
V_{I1}	Tied to AGND

IDRIVE	VDS
1/2 A	Disabled
570/1140 mA	1.88 V
260/520 mA	1.13 V
120/240 mA	0.60 V
60/120 mA	0.26 V
30/60 mA	0.13 V
10/20 mA	0.06 V

Figure 33. Seven Level Input Pin Structure

Figure 34 shows the structure of the open-drain output pins nFAULT and SDO. The open-drain output requires an external pullup resistor to function properly.

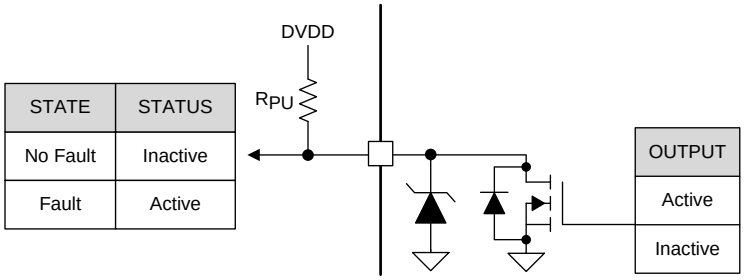


Figure 34. Open-Drain Output Pin Structure

8.3.4 Low-Side Current-Shunt Amplifiers (DRV8323 and DRV8323R Only)

The DRV8323 and DRV8323R integrate three, high-performance low-side current-shunt amplifiers for current measurements using low-side shunt resistors in the external half-bridges. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs or one amplifier can be used to sense the sum of the half-bridge legs. The current shunt amplifiers include features such as programmable gain, offset calibration, unidirectional and bidirectional support, and a voltage reference pin (VREF).

8.3.4.1 Bidirectional Current Sense Operation

The SOx pin on the DRV8323 and DRV8323R outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}). The gain setting is adjustable between four different levels (5 V/V, 10 V/V, 20 V/V, and 40 V/V). Use Equation 3 to calculate the current through the shunt resistor.

$$I = \frac{\frac{V_{VREF}}{2} - V_{SOx}}{G_{CSA} \times R_{SENSE}} \quad (3)$$

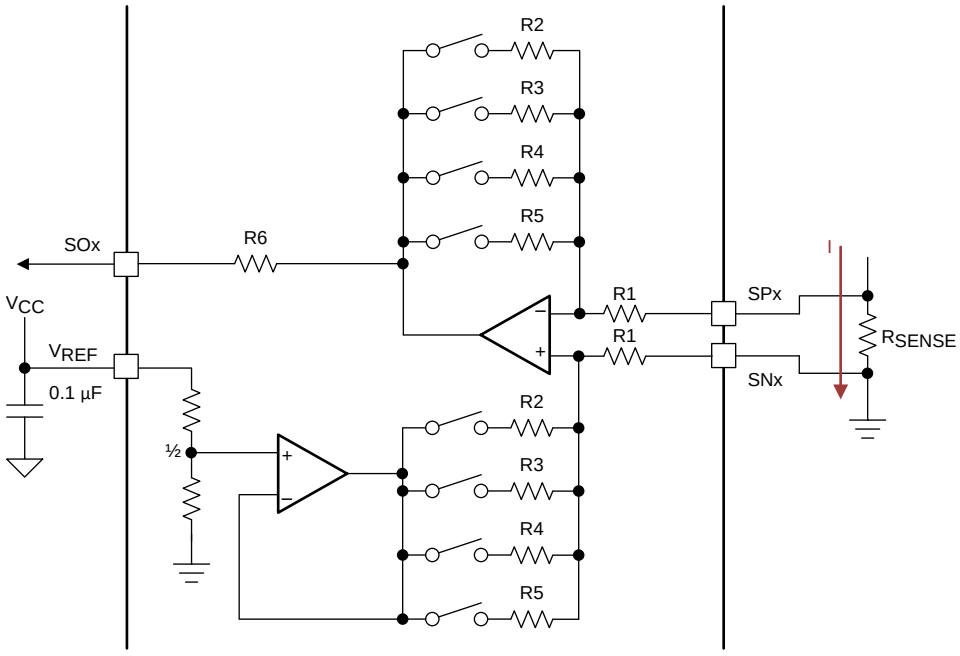


Figure 35. Bidirectional Current-Sense Configuration

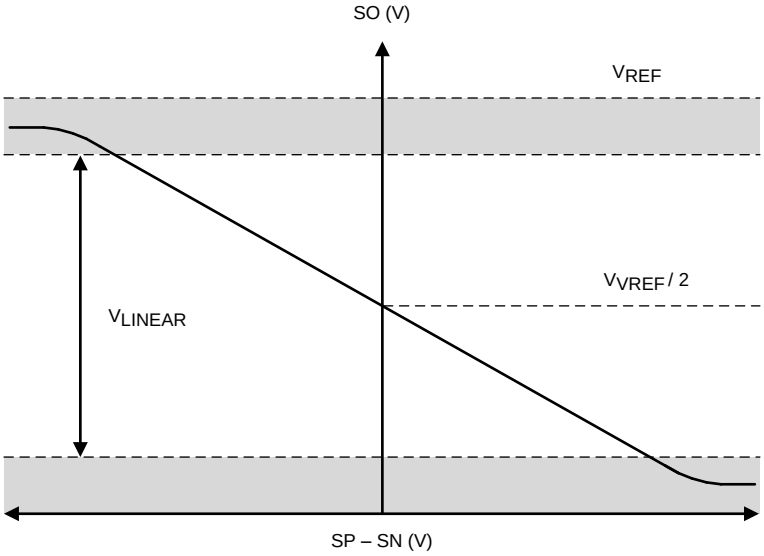


Figure 36. Bidirectional Current-Sense Output

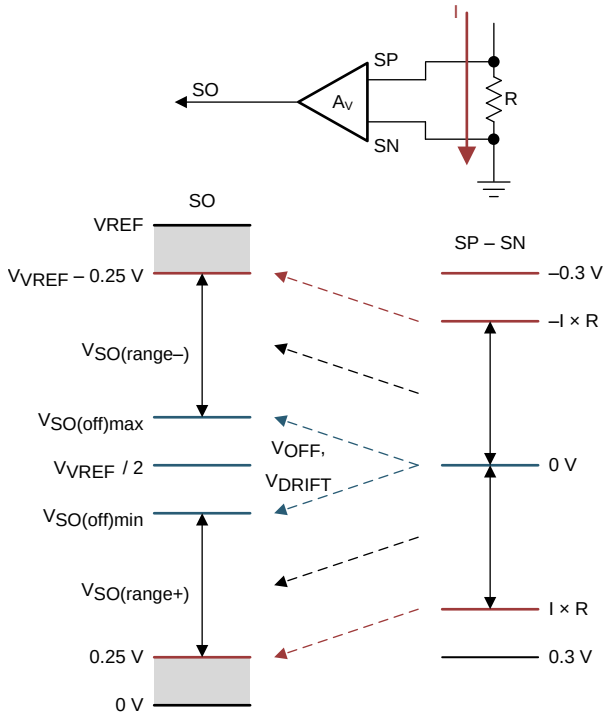


Figure 37. Bidirectional Current Sense Regions

8.3.4.2 Unidirectional Current Sense Operation (SPI only)

On the DRV8323 and DRV8323R SPI devices, use the VREF_DIV bit to remove the VREF divider. In this case the shunt amplifier operates unidirectionally and SOx outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}). Use Equation 4 to calculate the current through the shunt resistor.

$$I = \frac{V_{VREF} - V_{SOx}}{G_{CSA} \times R_{SENSE}} \quad (4)$$

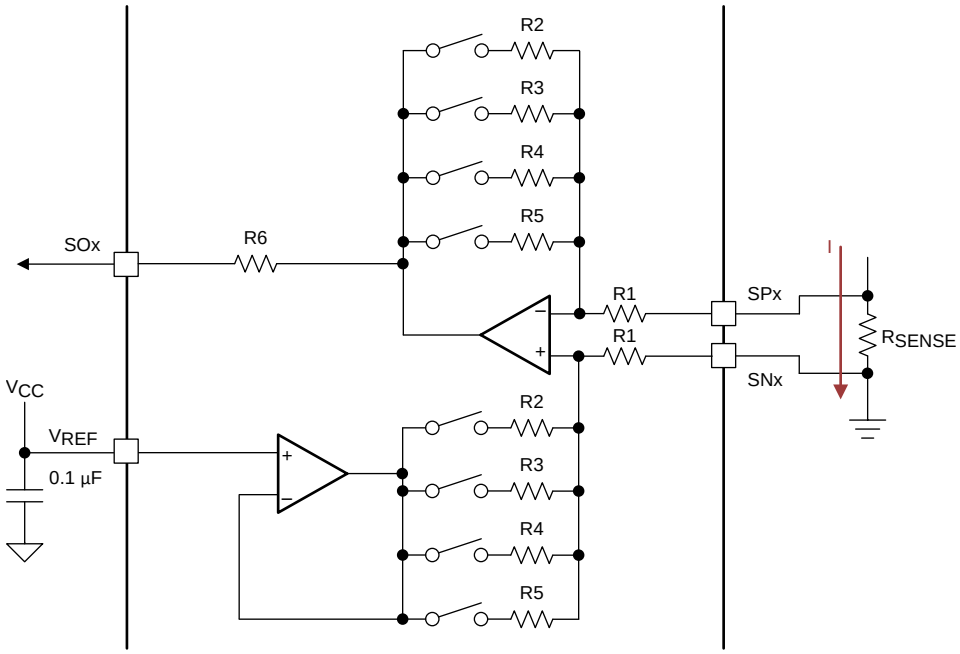


Figure 38. Unidirectional Current-Sense Configuration

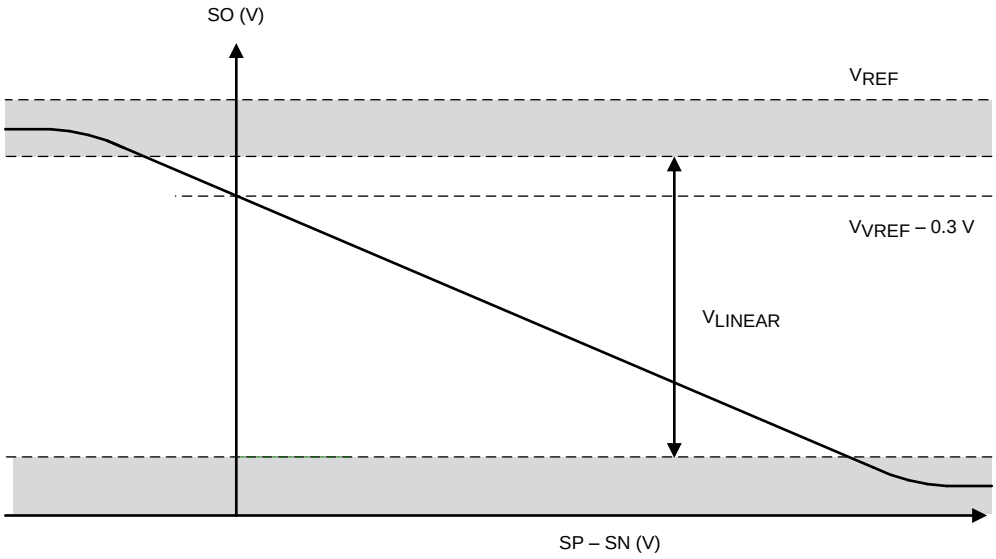


Figure 39. Unidirectional Current-Sense Output

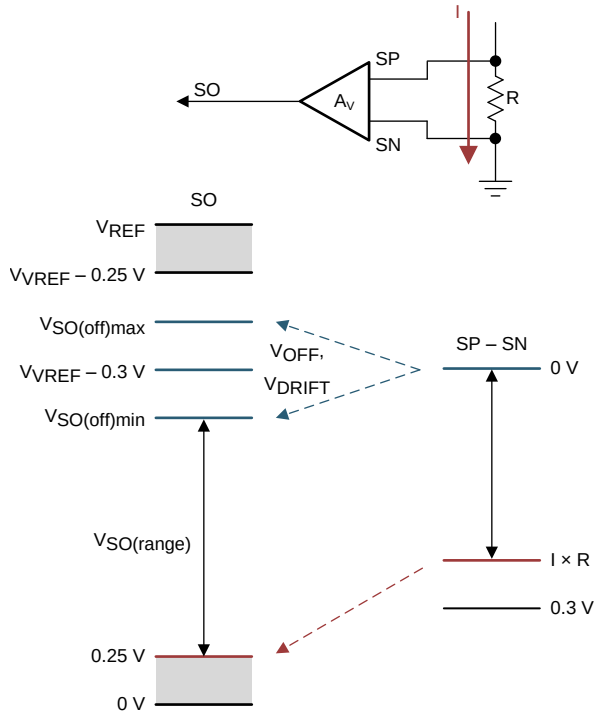


Figure 40. Unidirectional Current-Sense Regions

8.3.4.3 Auto Offset Calibration

To minimize DC offset, the DRV8323 and DRV8323R devices can perform an automatic offset calibration through the SPI registers (CSA_CAL_X) or CAL pin. When the calibration is enabled, the inputs to the amplifier are shorted, the load disconnected, and the gain (G_{CSA}) of the amplifier changed to the 40 V/V setting. The amplifier then goes through an automatic trim routine to minimize the input offset. The automatic trim routine requires 100 µs to complete after the calibration is enabled. After this time, the inputs of the amplifier remain shorted, the load disconnected, and the gain at 40 V/V if further offset calibration is desired to be done by the external controller. To complete the offset calibration, the CSA_CAL_X registers or CAL pin should be taken back low. For the best results, perform offset calibration when the external MOSFETS are not switching to reduce the potential noise impact to the amplifier.

8.3.4.4 MOSFET V_{DS} Sense Mode (SPI Only)

The current-sense amplifiers on the DRV8323 and DRV8323R SPI devices can be configured to amplify the voltage across the external low-side MOSFET V_{DS}. This allows for the external controller to measure the voltage drop across the MOSFET $R_{DS(on)}$ without the shunt resistor and then calculate the half-bridge current level.

To enable this mode set the CSA_FET bit to 1. The positive input of the amplifier is then internally connected to the SHx pin with an internal clamp to prevent high voltage on the SHx pin from damaging the sense amplifier inputs. During this mode of operation, the SPx pins should be left disconnected. When the CSA_FET bit is set to 1, the negative reference for the low-side V_{DS} monitor is automatically set to SNx, regardless of the state of the LS_REF bit state. This setting is implemented to prevent disabling of the low-side V_{DS} monitor.

If the system operates in MOSFET V_{DS} sensing mode, route the SHx and SNx pins with Kelvin connections across the drain and source of the external low-side MOSFETs.

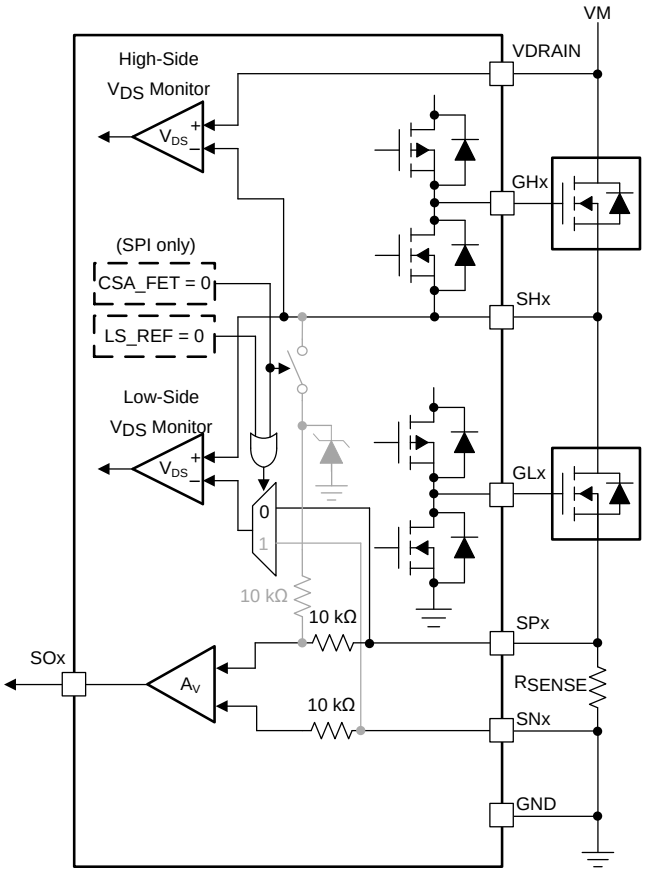


Figure 41. Resistor Sense Configuration

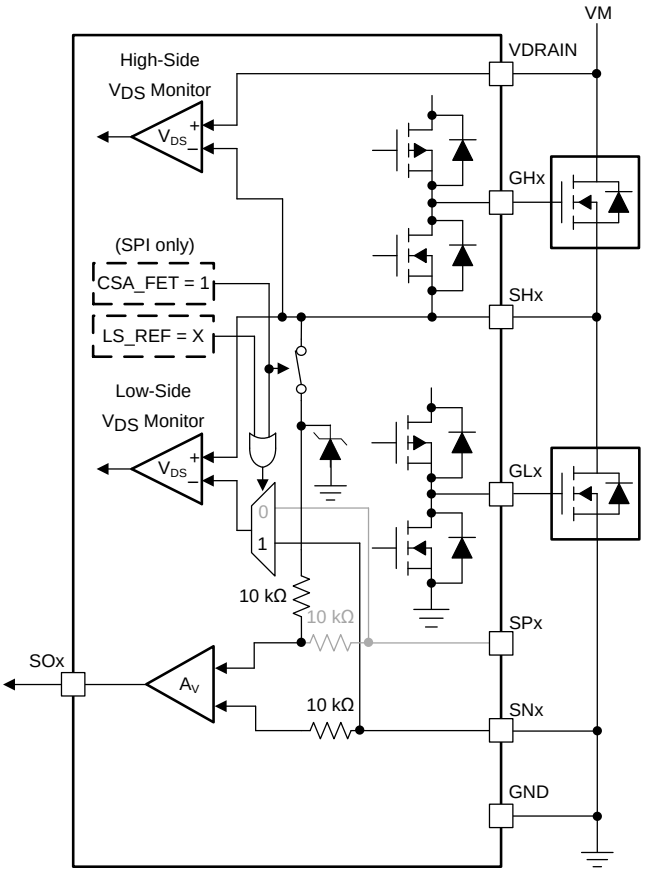


Figure 42. V_{DS} Sense Configuration

When operating in MOSFET V_{DS} sense mode, the amplifier is enabled at the end of the t_{DRIVE} time. At this time, the amplifier input is connected to the SHx pin, and the SOx output is valid. When the low-side MOSFET receives a signal to turn off, the amplifier inputs, SPx and SNx, are shorted together internally.

8.3.5 Step-Down Buck Regulator

The DRV8320R and DRV8323R have an integrated buck regulator (LMR16006) to supply power for an external controller or system voltage rail. The LMR16006 device is a 60-V, 600-mA, buck (step-down) regulator.

The buck regulator has a very-low quiescent current during light loads to prolong battery life. The LMR16006 device improves performance during line and load transients by implementing a constant-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design. The LMR160006 is the LMR16006X device version that uses a 0.7-MHz switching frequency.

The LMR16006 device reduces the external component count by integrating the bootstrap recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the CB to SW pin. The bootstrap capacitor voltage is monitored by a UVLO circuit and turns off the high-side MOSFET when the boot voltage falls below a preset threshold.

The LMR16006 device can operate at high duty cycles because of the boot UVLO and then refreshs the wimp MOSFET. The output voltage can be stepped down to as low as the 0.8-V reference. The internal soft-start feature minimizes inrush currents.

For additional details and design information refer to *LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency Eco-mode*.

8.3.5.1 Fixed Frequency PWM Control

The LMR16006 device has a fixed switching frequency and implements peak current-mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch turns off. The internal COMP node voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

8.3.5.2 Bootstrap Voltage (CB)

The LMR16006 device has an integrated bootstrap regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high-side MOSFET. The CB capacitor is refreshed when the high-side MOSFET is off and the low-side diode conducts. To improve dropout, the LMR16006 device is designed to operate at 100% duty cycle as long as the CB to SW pin voltage is greater than 3 V. When the voltage from the CB to SW pin drops below 3 V, the high-side MOSFET turns off using a UVLO circuit which allows the low-side diode to conduct and refresh the charge on the CB capacitor. Because the supply current sourced from the CB capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high. Attention must be taken in maximum duty-cycle applications with a light load. To ensure the SW pin can be pulled to ground to refresh the CB capacitor, an internal circuit charges the CB capacitor when the load is light or the device is working in dropout condition.

8.3.5.3 Output Voltage Setting

The output voltage is set using the feedback pin (FB) and a resistor divider connected to the output as shown in the Figure 51 section. The voltage of the feedback pin is 0.765 V, so the ratio of the feedback resistors sets the output voltage according to Equation 5.

$$V_O = 0.765\ V \times \left(1 + \left[\frac{R1}{R2}\right]\right) \tag{5}$$

Typically the starting value of R2 is from 1 kΩ to 100 kΩ. Use Equation 6 to calculate the value of R1.

$$R1 = R2 \times \left(\left[\frac{V_O}{0.765\ V}\right] - 1\right) \tag{6}$$

8.3.5.4 Enable nSHDN and VIN Undervoltage Lockout

The nSHDN pin of the LMR16006 device is a high-voltage tolerant input with an internal pullup circuit. The device can be enabled even if the nSHDN pin is floating. The regulator can also be turned on using 1.23-V or higher logic signals. If the use of a higher voltage is desired because of system or other constraints, a 100-kΩ or larger value resistor is recommended between the applied voltage and the nSHDN pin to help protect the device. When the nSHDN pin is pulled down to 0 V, the device turns off and enters the lowest shutdown current mode. In shutdown mode the supply current decreases to approximately 1 µA. If the shutdown function is unused, the nSHDN pin can be tied to the VIN pin with a 100-kΩ resistor. The maximum voltage to the nSHDN pin should not exceed 60 V. The LMR16006 device has an internal UVLO circuit to shut down the output if the input voltage falls below an internally-fixed UVLO-threshold level which ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator powers up when the input voltage exceeds the voltage level. If the UVLO voltage must be higher, use the nSHDN pin to adjust the system UVLO by using external resistors.

8.3.5.5 Current Limit

The LMR16006 device implements current mode control which uses the internal COMP voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. Each cycle, the switch current and internal COMP voltage are compared. When the peak switch current intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

8.3.5.6 Overvoltage Transient Protection

The LMR16006 device incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low-value output capacitance. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the voltage of the FB pin is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error amplifier output to a high voltage, therefore requesting the maximum output current. When the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state duty cycle. In some applications, the power-supply output voltage can respond faster than the error amplifier output can respond which leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot when using a low-value output capacitor by implementing a circuit to compare the FB pin voltage to the OVTP threshold which is 108% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.5.7 Thermal Shutdown

The device implements an internal thermal shutdown to help protect the device if the junction temperature exceeds 170°C (typical). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the junction temperature decreases below 160°C (typical), the device reinitiates the power up sequence.

8.3.6 Gate-Driver Protective Circuits

The DRV832x family of devices is fully protected against VM undervoltage, charge pump undervoltage, MOSFET V_{DS} overcurrent, gate driver shorts, and overtemperature events.

Table 8. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
VM undervoltage (UVLO)	$V_{VM} < V_{UVLO}$	—	nFAULT	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$
Charge pump undervoltage (CPUV)	$V_{VCP} < V_{CPUV}$	DIS_CPUV = 0b	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$
		DIS_CPUV = 1b	None	Active	Active	
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{VDS\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b	None	Active	Active	No action
V_{SENSE} overcurrent (SEN_OCP)	$V_{SP} > V_{SEN\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b or DIS_SEN = 1b	None	Active	Active	No action
Gate driver fault (GDF)	Gate voltage stuck > t_{DRIVE}	DIS_GDF = 0b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		DIS_GDF = 1b	None	Active	Active	No action
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$
		OTW_REP = 0b	None	Active	Active	No action
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$

8.3.6.1 VM Supply Undervoltage Lockout (UVLO)

If at any time the input supply voltage on the VM pin falls below the V_{UVLO} threshold, all of the external MOSFETs are disabled, the charge pump is disabled, and the nFAULT pin is driven low. The FAULT and VM_UVLO bits are also latched high in the registers on SPI devices. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the VM undervoltage condition is removed. The VM_UVLO bit remains set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}).

8.3.6.2 VCP Charge-Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls below the V_{CPUV} threshold voltage of the charge pump, all of the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and CPUV bits are also latched high in the registers on SPI devices. Normal operation resumes (gate-driver operation and the nFAULT pin is released) when the VCP undervoltage condition is removed. The CPUV bit remains set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}). Setting the DIS_CPUV bit high on the SPI devices disables this protection feature. On hardware interface devices, the CPUV protection is always enabled.

8.3.6.3 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. If the voltage across an enabled MOSFET exceeds the V_{VDS_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a VDS_OCP event is recognized and action is done according to the OCP_MODE. On hardware interface devices, the V_{VDS_OCP} threshold is set with the VDS pin, the t_{OCP_DEG} is fixed at 4 µs, and the OCP_MODE is configured for 4-ms automatic retry but can be disabled by tying the VDS pin to DVDD. On SPI devices, the V_{VDS_OCP} threshold is set through the VDS_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: V_{DS} latched shutdown, V_{DS} automatic retry, V_{DS} report only, and V_{DS} disabled.

8.3.6.3.1 V_{DS} Latched Shutdown (OCP_MODE = 00b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the VDS_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.3.2 V_{DS} Automatic Retry (OCP_MODE = 01b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, VDS_OCP, and MOSFET OCP bits remain latched until the t_{RETRY} period expires.

8.3.6.3.3 V_{DS} Report Only (OCP_MODE = 10b)

No protective action occurs after a VDS_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, VDS_OCP, and corresponding MOSFET OCP bits high in the SPI registers. The gate drivers continue to operate normally. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the VDS_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.3.4 V_{DS} Disabled (OCP_MODE = 11b)

No action occurs after a VDS_OCP event in this mode.

8.3.6.4 V_{SENSE} Overcurrent Protection (SEN_OCP)

Half-bridge overcurrent is also monitored by sensing the voltage drop across the external current-sense resistor with the SP pin. If at any time, the voltage on the SP input of the current-sense amplifier exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized and action is done according to the OCP_MODE. On hardware interface devices, the V_{SENSE} threshold is fixed at 1 V, t_{OCP_DEG} is fixed at 4 µs, and the OCP_MODE for V_{SENSE} is fixed for 4-ms automatic retry. On SPI devices, the V_{SENSE} threshold is set through the SEN_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: V_{SENSE} latched shutdown, V_{SENSE} automatic retry, V_{SENSE} report only, and V_{SENSE} disabled.

8.3.6.4.1 V_{SENSE} Latched Shutdown (OCP_MODE = 00b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and SEN_OCP bits are latched high in the SPI registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the SEN_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.4.2 V_{SENSE} Automatic Retry (OCP_MODE = 01b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, SEN_OCP, and corresponding sense OCP bits are latched high in the SPI registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT , SEN_OCP, and sense OCP bits remain latched until the t_{RETRY} period expires.

8.3.6.4.3 V_{SENSE} Report Only (OCP_MODE = 10b)

No protective action occurs after a SEN_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT and SEN_OCP bits high in the SPI registers. The gate drivers continue to operate. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT released) when the SEN_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.4.4 V_{SENSE} Disabled (OCP_MODE = 11b or DIS_SEN = 1b)

No action occurs after a SEN_OCP event in this mode. The SEN_OCP bit can be disabled independently of the VDS_OCP bit by using the DIS_SEN SPI register.

8.3.6.5 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault may be encountered if the GHx or GLx pins are shorted to the PGND, SHx, or VM pins. Additionally, a gate driver fault may be encountered if the selected I_{DRIVE} setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin driven low. In addition, the FAULT, GDF, and corresponding VGS bits are latched high in the SPI registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the gate driver fault condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). On SPI devices, setting the DIS_GDF_UVLO bit high disables this protection feature.

Gate driver faults can indicate that the selected I_{DRIVE} or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the I_{DRIVE} or t_{DRIVE} setting can resolve gate driver faults in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on.

8.3.6.6 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. When the die temperature falls below the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin by setting the OTW_REP bit to 1 through the SPI registers.

8.3.6.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the external MOSFETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and TSD bits are latched high. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the overtemperature condition is removed. The TSD bit remains latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). This protection feature cannot be disabled.

8.4 Device Functional Modes

8.4.1 Gate Driver Functional Modes

8.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV832x family of devices. When the ENABLE pin is low, the device enters a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the charge pump is disabled, the DVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the ENABLE pin before the device enters sleep mode. The device comes out of sleep mode automatically if the ENABLE pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all external MOSFETs are disabled. The high-side gate pins, GHx, are pulled to the SHx pin by an internal resistor and the low-side gate pins, GLx, are pulled to the PGND pin by an internal resistor.

It should be noted that during power up and power down of the device through the ENABLE pin, the nFAULT pin will be held low as the internal regulators enable or disable. After the regulators have enabled or disabled, the nFAULT pin will be automatically released. The duration that nFAULT is low will not exceed the t_{SLEEP} or t_{WAKE} time.

8.4.1.2 Operating Mode

When the ENABLE pin is high and $V_{VM} > V_{UVLO}$, the device enters operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, low-side gate regulator, DVDD regulator, and SPI bus are active

8.4.1.3 Fault Reset (CLR_FLT or ENABLE Reset Pulse)

In the case of device latched faults, the DRV832x family of devices enters a partial shutdown state to help protect the external power MOSFETs and system.

When the fault condition has been removed the device can reenter the operating state by either setting the CLR_FLT SPI bit on SPI devices or issuing a result pulse to the ENABLE pin on either interface variant. The ENABLE reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the ENABLE pin. The low period of the sequence should fall with the t_{RST} time window or else the device will begin the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks

8.4.2 Buck Regulator Functional Modes

8.4.2.1 Continuous Conduction Mode (CCM)

The LMR16006 integrated buck regulator steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at CCM), the buck regulator operates in two cycles. The power switch is connected between the VIN and SW pins. During the first cycle of operation, the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by the C_{OUT} capacitor and the rising current through the inductor. During the second cycle of operation, the transistor is open and the diode is forward biased because the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. Equation 7 and Equation 8 define the approximate output voltage.

$$D = \frac{V_O}{V_{VIN}} \tag{7}$$

where

- D is the duty cycle of the switch

$$D' = (1 - D) \tag{8}$$

The value of D and D' will be required for design calculations.

Device Functional Modes (continued)

8.4.2.2 Eco-mode™ Control Scheme

The LMR16006 device operates with the Eco-mode control scheme at light load currents to improve efficiency by reducing switching and gate-drive losses. The LMR16006 device is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the sleep-current threshold, $I_{INDUCTOR}$ ≤ 80 mA, the device enters Eco-mode. For Eco-mode operation, the LMR16006 device senses peak current, not average or load current, so the load current when the device enters Eco-mode is dependent on the input voltage, the output voltage, and the value of the output inductor. When the load current is low and the output voltage is within regulation, the device enters Eco-mode and draws only 28-µA input quiescent current.

8.5 Programming

This section applies only to the DRV832x SPI devices.

8.5.1 SPI Communication

8.5.1.1 SPI

On DRV832x SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16 bit word, with a 5 bit command and 11 bits of data. The SPI output data (SDO) word consists of 11-bit register data. The first 5 bits are don't care bits.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 5 bit command data.

8.5.1.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 4 address bits, A (bits B14 through B11)
- 11 data bits, D (bits B11 through B0)

The SDO output data word is 16 bits long and the first 5 bits are don't care bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 9. SDI Input Data Word Format

R/W	ADDRESS				DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 10. SDO Output Data Word Format

DON'T CARE BITS					DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

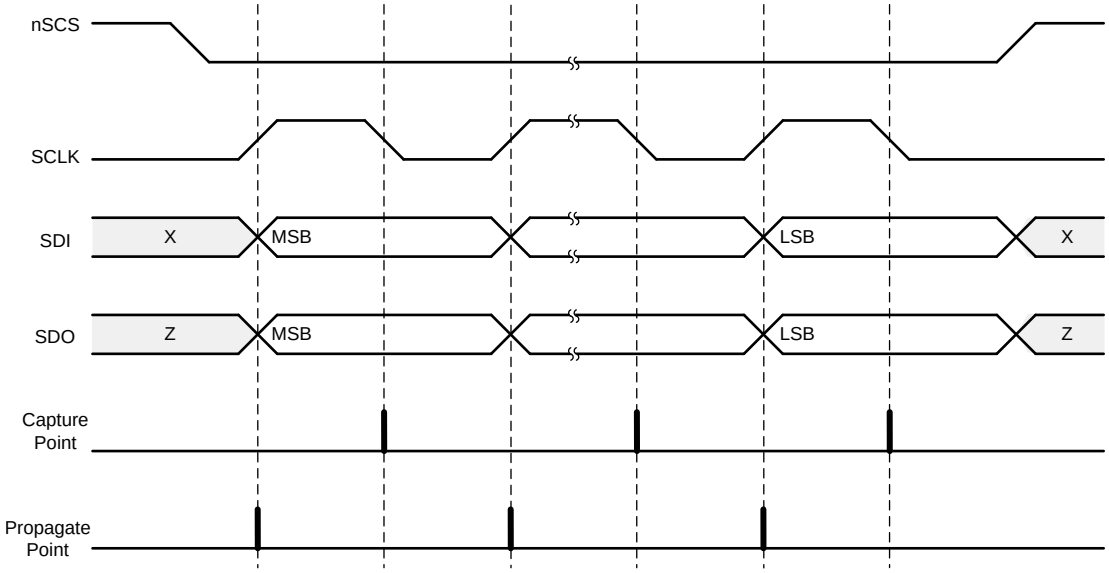


Figure 43. SPI Slave Timing Diagram

8.6 Register Maps

This section applies only to the DRV832x SPI devices.

NOTE

Do not modify reserved registers or addresses not listed in the register map (Table 11). Writing to these registers may have unintended effects. For all reserved bits, the default value is 0. To help prevent erroneous SPI writes from the master controller, set the LOCK bits to lock the SPI registers.

Table 11. DRV832xS and DRV832xRS Register Map

Name	10	9	8	7	6	5	4	3	2	1	0	Type	Address
DRV8320S and DRV8320RS													
Fault Status 1	FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R	0h
VGS Status 2	SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R	1h
Driver Control	Reserved	DIS_CPUV	DIS_GDF	OTW_REP	PWM_MODE		1PWM_COM	1PWM_DIR	COAST	BRAKE	CLR_FLT	RW	2h
Gate Drive HS	LOCK			IDRIVEP_HS				IDRIVEN_HS				RW	3h
Gate Drive LS	CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS				RW	4h
OCP Control	TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL				RW	5h
Reserved	Reserved											RW	6h
Reserved	Reserved											RW	7h
DRV8323S and DRV8323RS													
Fault Status 1	FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R	0h
VGS Status 2	SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R	1h
Driver Control	Reserved	DIS_CPUV	DIS_GDF	OTW_REP	PWM_MODE		1PWM_COM	1PWM_DIR	COAST	BRAKE	CLR_FLT	RW	2h
Gate Drive HS	LOCK			IDRIVEP_HS				IDRIVEN_HS				RW	3h
Gate Drive LS	CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS				RW	4h
OCP Control	TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL				RW	5h
CSA Control	CSA_FET	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	CSA_CAL_A	CSA_CAL_B	CSA_CAL_C	SEN_LVL		RW	6h
Reserved	Reserved											RW	7h

8.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. The status registers are read-only registers

Complex bit access types are encoded to fit into small table cells. Table 12 shows the codes that are used for access types in this section.

Table 12. Status Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 Fault Status Register 1 (address = 0x00h)

The fault status register 1 is shown in Figure 44 and described in Table 13.

Register access type: Read only

Figure 44. Fault Status Register 1

10	9	8	7	6	5	4	3	2	1	0
FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 13. Fault Status Register 1 Field Descriptions

Bit	Field	Type	Default	Description
10	FAULT	R	0b	Logic OR of FAULT status registers. Mirrors nFAULT pin.
9	VDS_OCP	R	0b	Indicates VDS monitor overcurrent fault condition
8	GDF	R	0b	Indicates gate drive fault condition
7	UVLO	R	0b	Indicates undervoltage lockout fault condition
6	OTSD	R	0b	Indicates overtemperature shutdown
5	VDS_HA	R	0b	Indicates VDS overcurrent fault on the A high-side MOSFET
4	VDS_LA	R	0b	Indicates VDS overcurrent fault on the A low-side MOSFET
3	VDS_HB	R	0b	Indicates VDS overcurrent fault on the B high-side MOSFET
2	VDS_LB	R	0b	Indicates VDS overcurrent fault on the B low-side MOSFET
1	VDS_HC	R	0b	Indicates VDS overcurrent fault on the C high-side MOSFET
0	VDS_LC	R	0b	Indicates VDS overcurrent fault on the C low-side MOSFET

8.6.1.2 Fault Status Register 2 (address = 0x01h)

The fault status register 2 is shown in Figure 45 and described in Table 14.

Register access type: Read only

Figure 45. Fault Status Register 2

10	9	8	7	6	5	4	3	2	1	0
SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 14. Fault Status Register 2 Field Descriptions

Bit	Field	Type	Default	Description
10	SA_OC	R	0b	Indicates overcurrent on phase A sense amplifier (DRV8323xS)
9	SB_OC	R	0b	Indicates overcurrent on phase B sense amplifier (DRV8323xS)
8	SC_OC	R	0b	Indicates overcurrent on phase C sense amplifier (DRV8323xS)
7	OTW	R	0b	Indicates overtemperature warning
6	CPUV	R	0b	Indicates charge pump undervoltage fault condition
5	VGS_HA	R	0b	Indicates gate drive fault on the A high-side MOSFET
4	VGS_LA	R	0b	Indicates gate drive fault on the A low-side MOSFET
3	VGS_HB	R	0b	Indicates gate drive fault on the B high-side MOSFET
2	VGS_LB	R	0b	Indicates gate drive fault on the B low-side MOSFET
1	VGS_HC	R	0b	Indicates gate drive fault on the C high-side MOSFET
0	VGS_LC	R	0b	Indicates gate drive fault on the C low-side MOSFET

8.6.2 Control Registers

The control registers are used to configure the device. The control registers are read and write capable

Complex bit access types are encoded to fit into small table cells. Table 15 shows the codes that are used for access types in this section.

Table 15. Control Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1 Driver Control Register (address = 0x02h)

The driver control register is shown in Figure 46 and described in Table 16.

Register access type: Read/Write

Figure 46. Driver Control Register

10	9	8	7	6	5	4	3	2	1	0
Reserved	DIS _CPUV	DIS _GDF	OTW _REP	PWM_MODE		1PWM _COM	1PWM _DIR	COAST	BRAKE	CLR _FLT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 16. Driver Control Field Descriptions

Bit	Field	Type	Default	Description
10	Reserved	R/W	0b	Reserved
9	DIS_CPUV	R/W	0b	**0b = Charge-pump undervoltage lockout fault is enabled** 1b = Charge-pump undervoltage lockout fault is disabled
8	DIS_GDF	R/W	0b	**0b = Gate drive fault is enabled** 1b = Gate drive fault is disabled
7	OTW_REP	R/W	0b	**0b = OTW is not reported on nFAULT or the FAULT bit** 1b = OTW is reported on nFAULT and the FAULT bit
6-5	PWM_MODE	R/W	00b	**00b = 6x PWM Mode** 01b = 3x PWM mode 10b = 1x PWM mode 11b = Independent PWM mode
4	1PWM_COM	R/W	0b	**0b = 1x PWM mode uses synchronous rectification** 1b = 1x PWM mode uses asynchronous rectification (diode freewheeling)
3	1PWM_DIR	R/W	0b	In 1x PWM mode this bit is ORed with the INHC (DIR) input
2	COAST	R/W	0b	Write a 1 to this bit to put all MOSFETs in the Hi-Z state
1	BRAKE	R/W	0b	Write a 1 to this bit to turn on all three low-side MOSFETs in 1x PWM mode. This bit is ORed with the INLC (BRAKE) input.
0	CLR_FLT	R/W	0b	Write a 1 to this bit to clear latched fault bits. This bit automatically resets after being writen.

8.6.2.2 Gate Drive HS Register (address = 0x03h)

The gate drive HS register is shown in Figure 47 and described in Table 17.

Register access type: Read/Write

Figure 47. Gate Drive HS Register

10	9	8	7	6	5	4	3	2	1	0
LOCK			IDRIVEP_HS				IDRIVEn_HS			
R/W-011b			R/W-1111b				R/W-1111b			

Table 17. Gate Drive HS Field Descriptions

Bit	Field	Type	Default	Description
10-8	LOCK	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x02h bits 0-2. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
7-4	IDRIVEP_HS	R/W	1111b	0000b = 10 mA 0001b = 30 mA 0010b = 60 mA 0011b = 80 mA 0100b = 120 mA 0101b = 140 mA 0110b = 170 mA 0111b = 190 mA 1000b = 260 mA 1001b = 330 mA 1010b = 370 mA 1011b = 440 mA 1100b = 570 mA 1101b = 680 mA 1110b = 820 mA **1111b = 1000 mA**
3-0	IDRIVEN_HS	R/W	1111b	0000b = 20 mA 0001b = 60 mA 0010b = 120 mA 0011b = 160 mA 0100b = 240 mA 0101b = 280 mA 0110b = 340 mA 0111b = 380 mA 1000b = 520 mA 1001b = 660 mA 1010b = 740 mA 1011b = 880 mA 1100b = 1140 mA 1101b = 1360 mA 1110b = 1640 mA **1111b = 2000 mA**

8.6.2.3 Gate Drive LS Register (address = 0x03h)

The gate drive LS register is shown in Figure 48 and described in Table 18.

Register access type: Read/Write

Figure 48. Gate Drive LS Register

10	9	8	7	6	5	4	3	2	1	0
CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS			
R/W-1b	R/W-11b		R/W-1111b				R/W-1111b			

Table 18. Gate Drive LS Register Field Descriptions

Bit	Field	Type	Default	Description
10	CBC	R/W	1b	In retry OCP_MODE, for both VDS_OCP and SEN_OCP, the fault is automatically cleared when a PWM input is given
9-8	TDRIVE	R/W	11b	00b = 500-ns peak gate-current drive time 01b = 1000-ns peak gate-current drive time 10b = 2000-ns peak gate-current drive time **11b = 4000-ns peak gate-current drive time**
7-4	IDRIVEP_LS	R/W	1111b	0000b = 10 mA 0001b = 30 mA 0010b = 60 mA 0011b = 80 mA 0100b = 120 mA 0101b = 140 mA 0110b = 170 mA 0111b = 190 mA 1000b = 260 mA 1001b = 330 mA 1010b = 370 mA 1011b = 440 mA 1100b = 570 mA 1101b = 680 mA 1110b = 820 mA **1111b = 1000 mA**
3-0	IDRIVEN_LS	R/W	1111b	0000b = 20 mA 0001b = 60 mA 0010b = 120 mA 0011b = 160 mA 0100b = 240 mA 0101b = 280 mA 0110b = 340 mA 0111b = 380 mA 1000b = 520 mA 1001b = 660 mA 1010b = 740 mA 1011b = 880 mA 1100b = 1140 mA 1101b = 1360 mA 1110b = 1640 mA **1111b = 2000 mA**

8.6.2.4 OCP Control Register (address = 0x05h)

The OCP control register is shown in Figure 49 and described in Table 19.

Register access type: Read/Write

Figure 49. OCP Control Register

10	9	8	7	6	5	4	3	2	1	0
TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL			
R/W-0b	R/W-00b		R/W-01b		R/W-01b		R/W-1001b			

Table 19. OCP Control Field Descriptions

Bit	Field	Type	Default	Description
10	TRETRY	R/W	0b	**0b = VDS_OCP and SEN_OCP retry time is 4 ms** 1b = VDS_OCP and SEN_OCP retry time is 50 µs
9-8	DEAD_TIME	R/W	01b	00b = 50-ns dead time **01b = 100-ns dead time** 10b = 200-ns dead time 11b = 400-ns dead time
7-6	OCP_MODE	R/W	01b	00b = Overcurrent causes a latched fault **01b = Overcurrent causes an automatic retrying fault** 10b = Overcurrent is report only but no action is taken 11b = Overcurrent is not reported and no action is taken
5-4	OCP_DEG	R/W	01b	00b = Overcurrent deglitch of 2 µs **01b = Overcurrent deglitch of 4 µs** 10b = Overcurrent deglitch of 6 µs 11b = Overcurrent deglitch of 8 µs
3-0	VDS_LVL	R/W	1001b	0000b = 0.06 V 0001b = 0.13 V 0010b = 0.2 V 0011b = 0.26 V 0100b = 0.31 V 0101b = 0.45 V 0110b = 0.53 V 0111b = 0.6 V 1000b = 0.68 V **1001b = 0.75 V** 1010b = 0.94 V 1011b = 1.13 V 1100b = 1.3 V 1101b = 1.5 V 1110b = 1.7 V 1111b = 1.88 V

8.6.2.5 CSA Control Register (DRV8323x Only) (address = 0x06h)

The CSA control register is shown in Figure 50 and described in Table 20.

Register access type: Read/Write
This register is only available with the DRV8323x family of devices.

Figure 50. CSA Control Register

10	9	8	7	6	5	4	3	2	1	0
CSA_FET	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	CSA_CAL_A	CSA_CAL_B	CSA_CAL_C	SEN_LVL	
R/W-0b	R/W-1b	R/W-0b	R/W-10b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b	

Table 20. CSA Control Field Descriptions

Bit	Field	Type	Default	Description
10	CSA_FET	R/W	0b	**0b = Sense amplifier positive input is SPx** 1b = Sense amplifier positive input is SHx (also automatically sets the LS_REF bit to 1)
9	VREF_DIV	R/W	1b	0b = Sense amplifier reference voltage is VREF (unidirectional mode) **1b = Sense amplifier reference voltage is VREF divided by 2**
8	LS_REF	R/W	0b	**0b = VDS_OCP for the low-side MOSFET is measured across SHx to SPx** 1b = VDS_OCP for the low-side MOSFET is measured across SHx to SNx
7-6	CSA_GAIN	R/W	10b	00b = 5-V/V shunt amplifier gain 01b = 10-V/V shunt amplifier gain **10b = 20-V/V shunt amplifier gain** 11b = 40-V/V shunt amplifier gain
5	DIS_SEN	R/W	0b	**0b = Sense overcurrent fault is enabled** 1b = Sense overcurrent fault is disabled
4	CSA_CAL_A	R/W	0b	**0b = Normal sense amplifier A operation** 1b = Short inputs to sense amplifier A for offset calibration
3	CSA_CAL_B	R/W	0b	**0b = Normal sense amplifier B operation** 1b = Short inputs to sense amplifier B for offset calibration
2	CSA_CAL_C	R/W	0b	**0b = Normal sense amplifier C operation** 1b = Short inputs to sense amplifier C for offset calibration
1-0	SEN_LVL	R/W	11b	00b = Sense OCP 0.25 V 01b = Sense OCP 0.5 V 10b = Sense OCP 0.75 V **11b = Sense OCP 1 V**

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV832x family of devices is primarily used in three-phase brushless DC motor control applications. The design procedures in the *Typical Application* section highlight how to use and configure the DRV832x family of devices.

9.2 Typical Application

9.2.1 Primary Application

The DRV8323R SPI device is used in this application example.

Typical Application (continued)

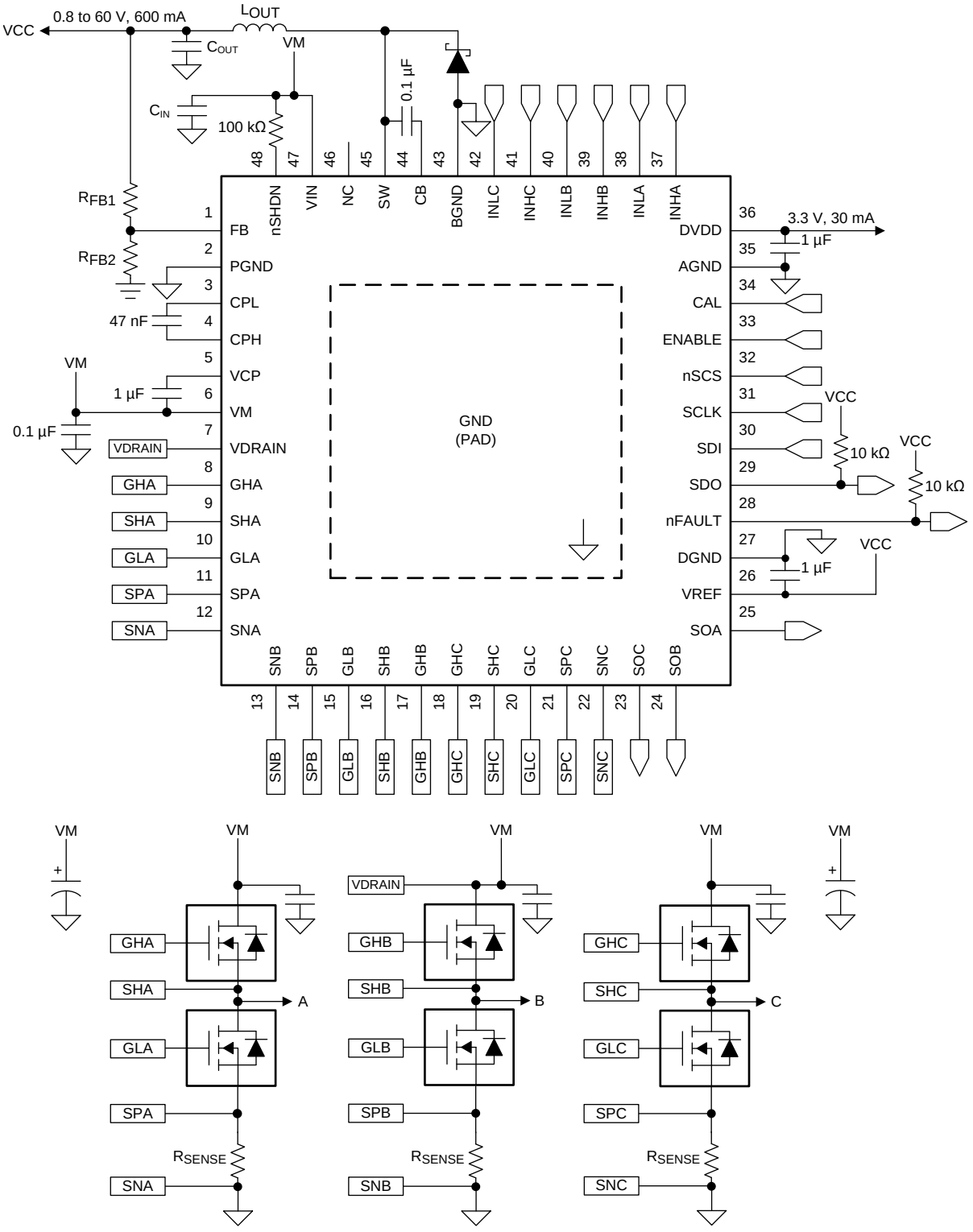


Figure 51. Primary Application Schematic

Typical Application (continued)

9.2.1.1 Design Requirements

Table 21 lists the example input parameters for the system design.

Table 21. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	24 V
Supply voltage range		8 V to 45 V
MOSFET part number		CSD18536KCS
MOSFET total gate charge	Q_g	83 nC (typical) at V_{VGS} = 10 V
MOSFET gate to drain charge	Q_{gd}	14 nC (typical)
Target output rise time	t_r	100 to 300 ns
Target output fall time	t_f	50 to 150 ns
PWM Frequency	f_{PWM}	45 kHz
Buck regulator output voltage	V_{VCC}	3.3 V
Maximum motor current	I_{max}	100 A
ADC reference voltage	V_{VREF}	3.3 V
Winding sense current range	I_{SENSE}	–40 A to +40 A
Motor RMS current	I_{RMS}	28.3 A
Sense resistor power rating	P_{SENSE}	2 W
System ambient temperature	T_A	–20°C to +105°C

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 External MOSFET Support

The DRV832x family of devices MOSFET support is based on the charge-pump capacity and output PWM switching frequency. For a quick calculation of MOSFET driving capacity, use Equation 9 and Equation 10 for three phase BLDC motor applications.

Trapezoidal 120° Commutation: $I_{VCP} > Q_g \times f_{PWM}$ (9)

Sinusoidal 180° Commutation: $I_{VCP} > 3 \times Q_g \times f_{PWM}$

where

- f_{PWM} is the maximum desired PWM switching frequency.
- I_{VCP} is the charge pump capacity, which depends on the VM pin voltage.
- The multiplier based on the commutation control method, may vary based on implementation. (10)

9.2.1.2.1.1 Example

If a system at V_{VM} = 8 V (I_{VCP} = 15 mA) uses a maximum PWM switching frequency of 45 kHz, then the charge-pump can support MOSFETs using trapezoidal commutation with a Q_g < 167 nC, and MOSFETs with sinusoidal commutation Q_g < 56 nC.

9.2.1.2.2 IDRIVE Configuration

The gate drive current strength, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the outputs. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET may not turn on completely within the t_{DRIVE} time and a gate drive fault may be asserted. Additionally, slow rise and fall times will lead to higher switching power losses. TI recommends adjusting these values in system with the required external MOSFETs and motor to determine the best possible setting for any application.

The I_{DRIVEP} and I_{DRIVEN} current for both the low-side and high-side MOSFETs are independently adjustable on SPI devices through the SPI registers. On hardware interface devices, both source and sink settings are selected simultaneously on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge Q_{gd}, desired rise time (t_r), and a desired fall time (t_f), use Equation 11 and Equation 12 to calculate the value of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} > Q_{gd} \times t_r \quad (11)$$

$$I_{DRIVEN} > Q_{gd} \times t_f \quad (12)$$

9.2.1.2.2.1 Example

Use Equation 13 and Equation 14 to calculate the value of $I_{DRIVEP1}$ and $I_{DRIVEP2}$ (respectively) for a gate to drain charge of 14 nC and a rise time from 100 to 300 ns.

$$I_{DRIVEP1} = \frac{14\ nC}{100\ ns} = 140\ mA \quad (13)$$

$$I_{DRIVEP2} = \frac{14\ nC}{300\ ns} = 47\ mA \quad (14)$$

Select a value for I_{DRIVEP} that is between 47 mA and 140 mA. For this example, the value of I_{DRIVEP} was selected as 120-mA source.

Use Equation 15 and Equation 16 to calculate the value of $I_{DRIVEN1}$ and $I_{DRIVEN2}$ (respectively) for a gate to drain charge of 14 nC and a fall time from 50 to 150 ns.

$$I_{DRIVEN1} = \frac{14\ nC}{50\ ns} = 280\ mA \quad (15)$$

$$I_{DRIVEN2} = \frac{14\ nC}{150\ ns} = 93\ mA \quad (16)$$

Select a value for I_{DRIVEN} that is between 93 mA and 280 mA. For this example, the value of I_{DRIVEN} was selected as 240-mA sink.

9.2.1.2.3 V_{DS} Overcurrent Monitor Configuration

The V_{DS} monitors are configured based on the worst-case motor current and the $R_{DS(on)}$ of the external MOSFETs as shown in Equation 17.

$$V_{DS\_OCP} > I_{max} \times R_{DS(on)max} \quad (17)$$

9.2.1.2.3.1 Example

The goal of this example is to set the V_{DS} monitor to trip at a current greater than 100 A. According to the *CSD18536KCS 60 V N-Channel NexFET™ Power MOSFET* data sheet, the $R_{DS(on)}$ value is 1.8 times higher at 175°C, and the maximum $R_{DS(on)}$ value at a V_{GS} of 10 V is 1.6 mΩ. From these values, the approximate worst-case value of $R_{DS(on)}$ is 1.8 × 1.6 mΩ = 2.88 mΩ.

Using Equation 17 with a value of 2.88 mΩ for $R_{DS(on)}$ and a worst-case motor current of 100 A, Equation 18 shows the calculated the value of the V_{DS} monitors.

$$V_{DS\_OCP} > 100\ A \times 2.88\ m\Omega$$

$$V_{DS\_OCP} > 0.288\ V \quad (18)$$

For this example, the value of V_{DS_OCP} was selected as 0.31 V.

The SPI devices allow for adjustment of the deglitch time for the V_{DS} overcurrent monitor. The deglitch time can be set to 2 µs, 4 µs, 6 µs, or 8 µs.

9.2.1.2.4 Sense-Amplifier Bidirectional Configuration (DRV8323 and DRV8323R)

The sense amplifier gain on the DRV8323, DRV8323R devices and sense resistor value are selected based on the target current range, VREF voltage supply, sense-resistor power rating, and operating temperature range. In bidirectional operation of the sense amplifier, the dynamic range at the output is approximately calculated as shown in Equation 19.

$$V_O = \left(V_{VREF} - 0.25\ V\right) - \frac{V_{VREF}}{2} \quad (19)$$

Use Equation 20 to calculate the approximate value of the selected sense resistor with V_O calculated using Equation 19.

$$R = \frac{V_O}{A_V \times I} \quad P_{SENSE} > I_{RMS}^2 \times R \tag{20}$$

From Equation 19 and Equation 20, select a target gain setting based on the power rating of the target sense resistor.

9.2.1.2.4.1 Example

In this system example, the value of VREF voltage is 3.3 V with a sense current from –40 to +40 A. The linear range of the SOx output is 0.25 V to V_{VREF} – 0.25 V (from the V_{LINEAR} specification). The differential range of the sense amplifier input is –0.3 to +0.3 V (V_{DIFF}).

$$V_O = (3.3\ V - 0.25\ V) - \frac{3.3\ V}{2} = 1.4\ V \tag{21}$$

$$R = \frac{1.4\ V}{A_V \times 40\ A} \quad 2\ W > 28.3^2 \times R \rightarrow R < 2.5\ m\Omega \tag{22}$$

$$2.5\ m\Omega > \frac{1.4\ V}{A_V \times 40\ A} \rightarrow A_V > 14 \tag{23}$$

Therefore, the gain setting must be selected as 20 V/V or 40 V/V and the value of the sense resistor must be less than 2.5 mΩ to meet the power requirement for the sense resistor. For this example, the gain setting was selected as 20 V/V. The value of the resistor and worst case current can be verified that R < 2.5 mΩ and I_{max} = 40 A does not violate the differential range specification of the sense amplifier input (V_{SPxD}).

9.2.1.2.5 Buck Regulator Configuration (DRV8320R and DRV8323R)

For a detailed design procedure and information on selecting the proper buck regulator external components, refer to *LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency Eco-mode*.

9.2.1.3 Application Curves

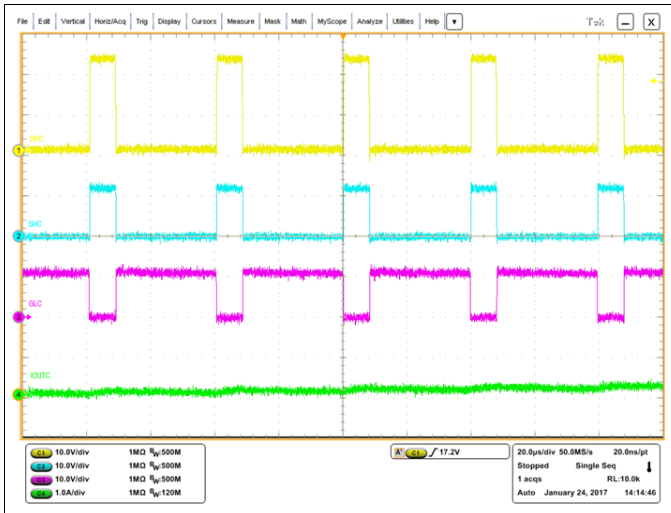


Figure 52. Gate-Drive 20% Duty Cycle

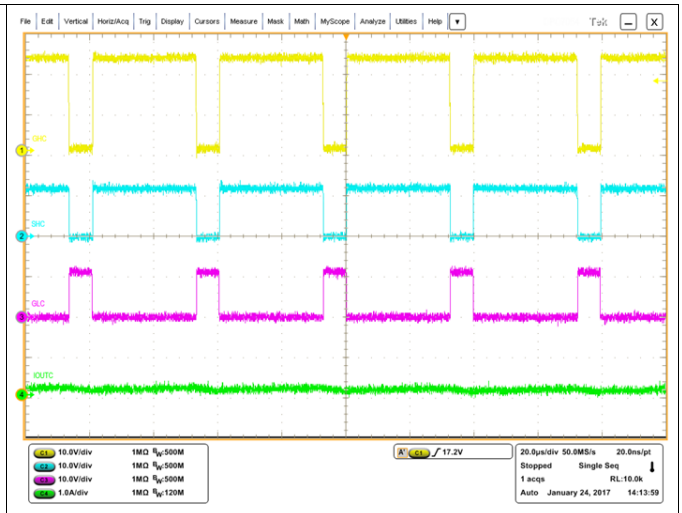


Figure 53. Gate-Drive 80% Duty Cycle

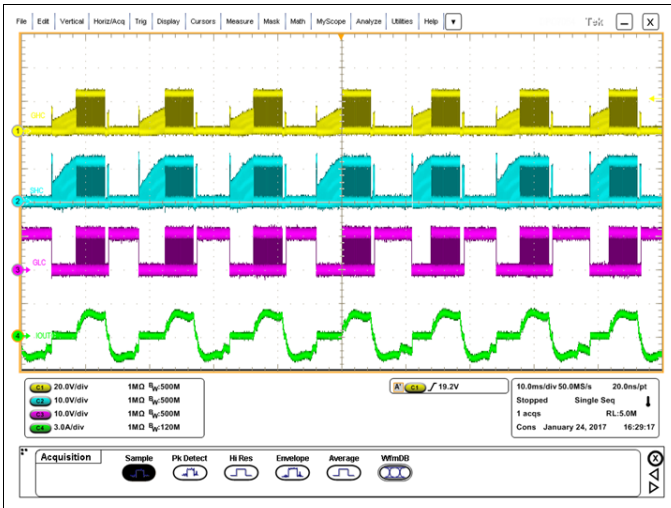


Figure 54. BLDC Motor Commutation 1000 RPM

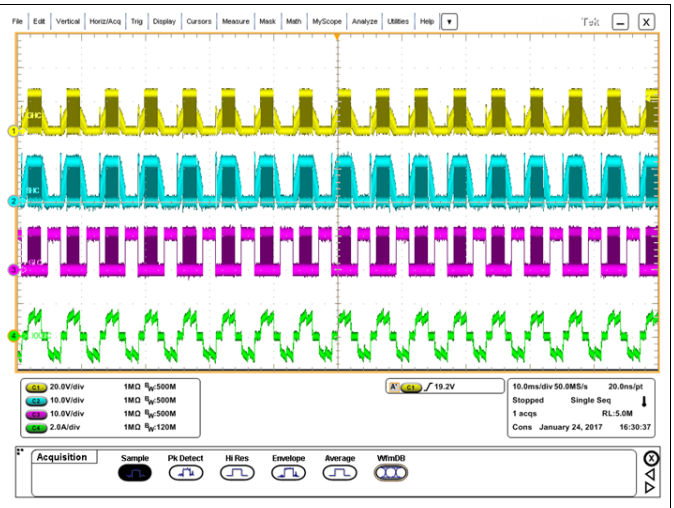


Figure 55. BLDC Motor Commutation 2000 RPM

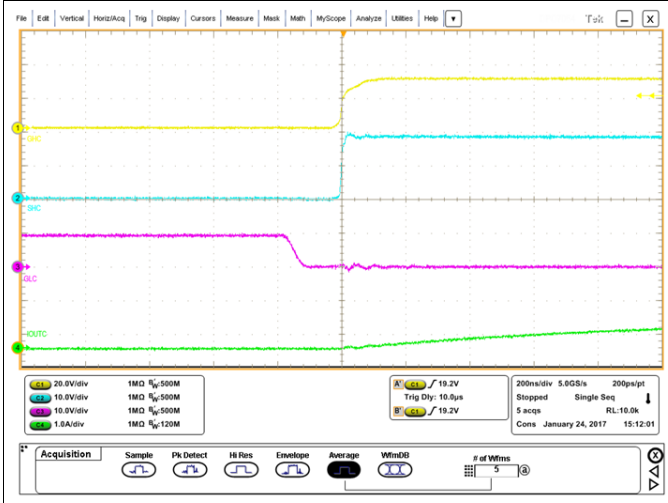


Figure 56. IDRIVE Maximum Setting Positive Current

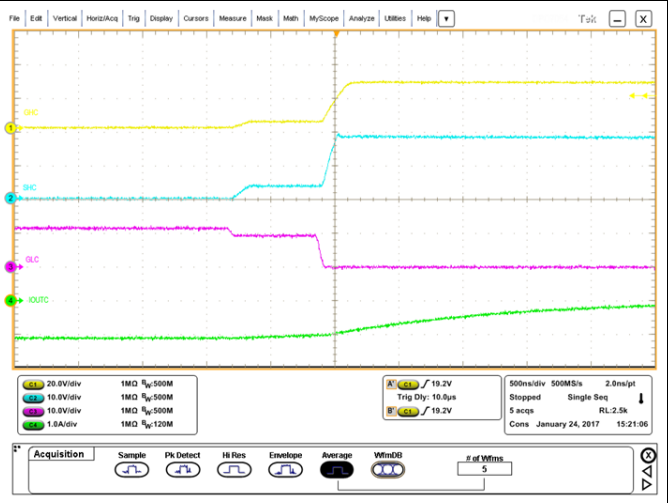


Figure 57. IDRIVE Maximum Setting Negative Current

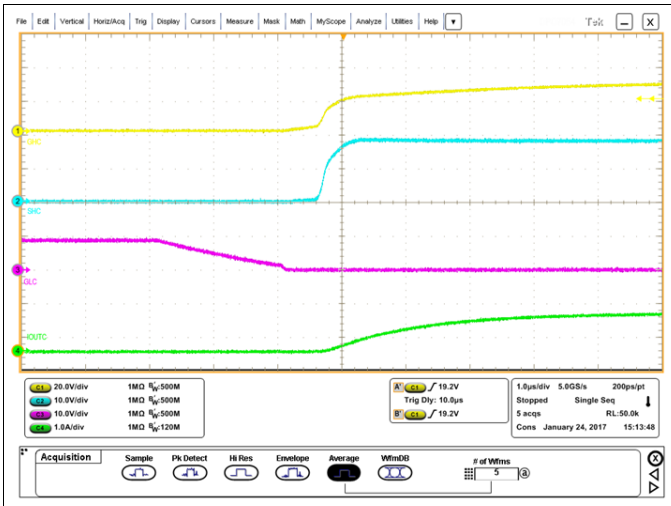


Figure 58. IDRIVE Minimum Setting Positive Current

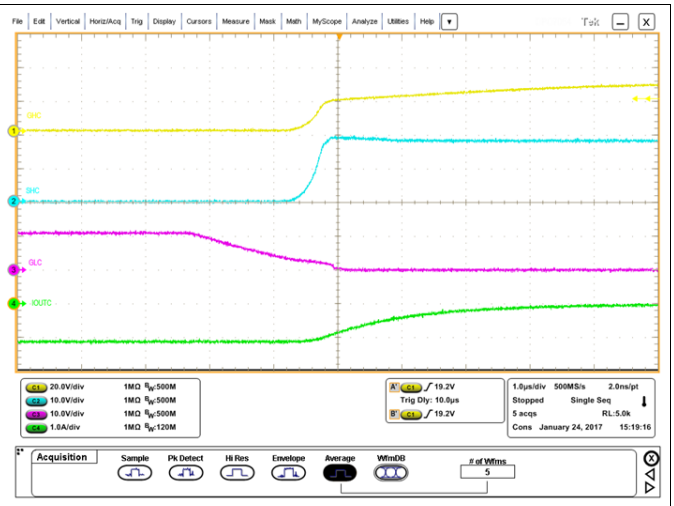


Figure 59. IDRIVE Minimum Setting Negative Current

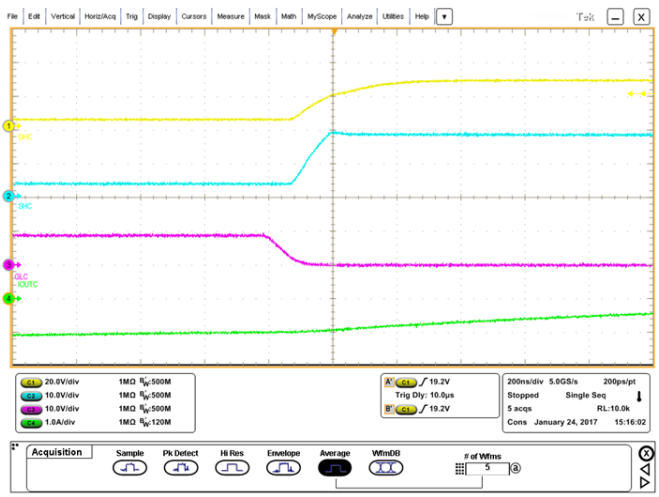


Figure 60. IDRIVE 260 to 520-mA Setting Negative Current

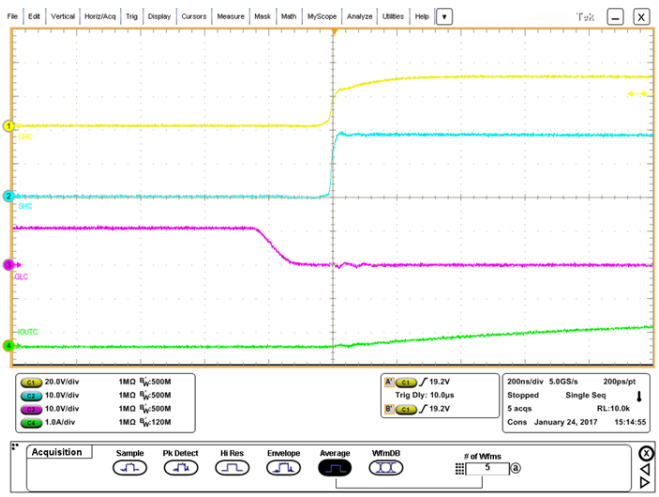


Figure 61. IDRIVE 260 to 520-mA Setting Positive Current

9.2.2 Alternative Application

In this application, a single-sense amplifier is used in unidirectional mode for a summing current sense scheme often used in trapezoidal or hall-based BLDC commutation control.

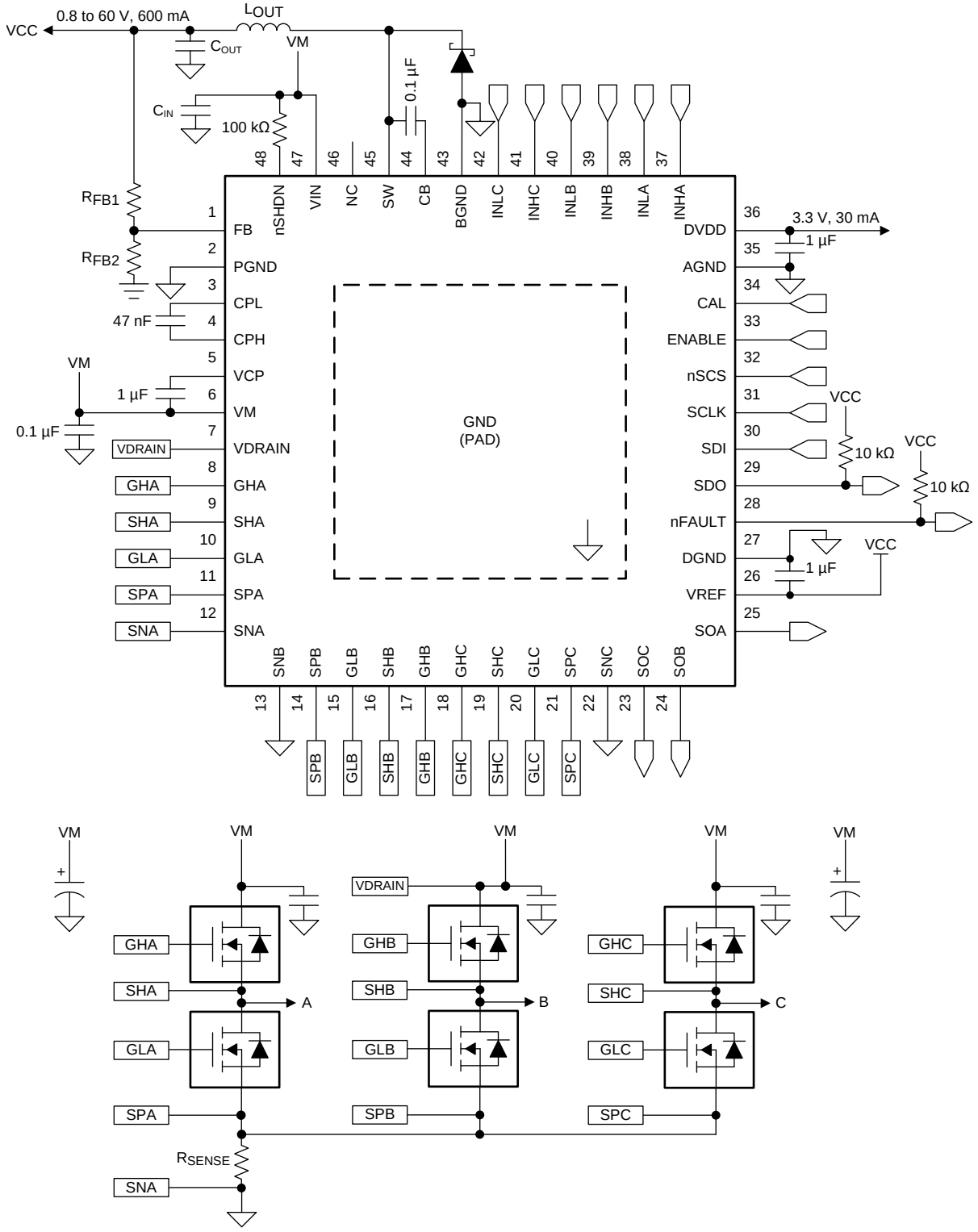


Figure 62. Alternative Application Schematic

9.2.2.1 Design Requirements

Table 22 lists the example design input parameters for system design.

Table 22. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
ADC reference voltage	V_{VREF}	3.3 V
Sensed current	I_{SENSE}	0 to 40 A
Motor RMS current	I_{RMS}	28.3 A
Sense-resistor power rating	P_{SENSE}	3 W
System ambient temperature	T_A	–20°C to +105°C

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Sense Amplifier Unidirectional Configuration

The sense amplifiers are configured to be unidirectional through the registers on SPI devices by writing a 0 to the VREF_DIV bit.

The sense-amplifier gain and sense resistor values are selected based on the target current range, VREF, sense-resistor power rating, and operating temperature range. In unidirectional operation of the sense amplifier, use Equation 24 to calculate the approximate value of the dynamic range at the output.

$$V_O = \left(V_{VREF} - 0.25\ V\right) - 0.25\ V = V_{VREF} - 0.5\ V \tag{24}$$

Use Equation 25 to calculate the approximate value of the selected sense resistor.

$$R = \frac{V_O}{A_V \times I} \qquad P_{SENSE} > I_{RMS}{}^2 \times R \tag{25}$$

where

- $V_O = V_{VREF} - 0.5\ V$

From Equation 24 and Equation 25, select a target gain setting based on the power rating of a target sense resistor.

9.2.2.2.1.1 Example

In this system example, the value of VREF is 3.3 V with a sense current from 0 to 40 A. The linear range of the SOx output for the DRV8323x device is 0.25 V to V_{VREF} – 0.25 V (from the V_{LINEAR} specification). The differential range of the sense-amplifier input is –0.3 to +0.3 V (V_{DIFF}).

$$V_O = 3.3\ V - 0.5\ V = 2.8\ V \tag{26}$$

$$R = \frac{2.8\ V}{A_V \times 40\ A} \qquad 3\ W > 28.3^2 \times R \rightarrow R < 3.75\ m\Omega \tag{27}$$

$$3.75\ m\Omega > \frac{2.8\ V}{A_V \times 40\ A} \rightarrow A_V > 18.7 \tag{28}$$

Therefore, the gain setting must be selected as 20 V/V or 40 V/V and the value of the sense resistor must be less than 3.75 mΩ to meet the power requirement for the sense resistor. For this example, the gain setting was selected as 20 V/V. The value of the resistor and worst-case current can be verified that R < 3.75 mΩ and I_{max} = 40 A does not violate the differential range specification of the sense amplifier input (V_{SPxD}).

10 Power Supply Recommendations

The DRV832x family of devices is designed to operate from an input voltage supply (VM) range between 6 V and 60 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the VM pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

10.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

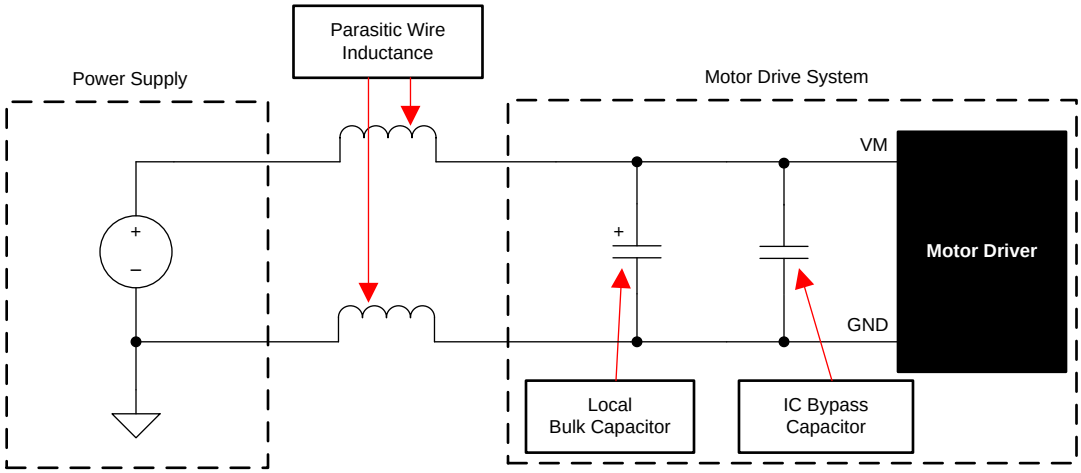


Figure 63. Motor Drive Supply Parasitics Example

11 Layout

11.1 Layout Guidelines

Bypass the VM pin to the PGND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 47 nF, rated for VM, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and VM pins. This capacitor should be 1 µF, rated for 16 V, and be of type X5R or X7R.

Bypass the DVDD pin to the AGND pin with a 1-µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

The VDRAIN pin can be shorted directly to the VM pin. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Do not connect the SLx pins directly to PGND. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations allow for more accurate V_{DS} sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

11.1.1 Buck-Regulator Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI:

- Place the feedback network resistors close to the FB pin and away from the inductor to minimize coupling noise into the feedback pin.
- Place the input bypass capacitor close to the VIN pin to reduce copper trace resistance which effects input voltage ripple of the device.
- Place the inductor close to the SW pin to reduce magnetic and electrostatic noise.
- Place the output capacitor close to the junction of the inductor and the diode. The inductor, diode, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
- Make the ground connection for the diode, C_{VIN}, and C_{OUT} as small as possible and tie it to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane.

For more detail on switching power supply layout considerations refer to *AN-1149 Layout Guidelines for Switching Power Supplies*.

11.2 Layout Example

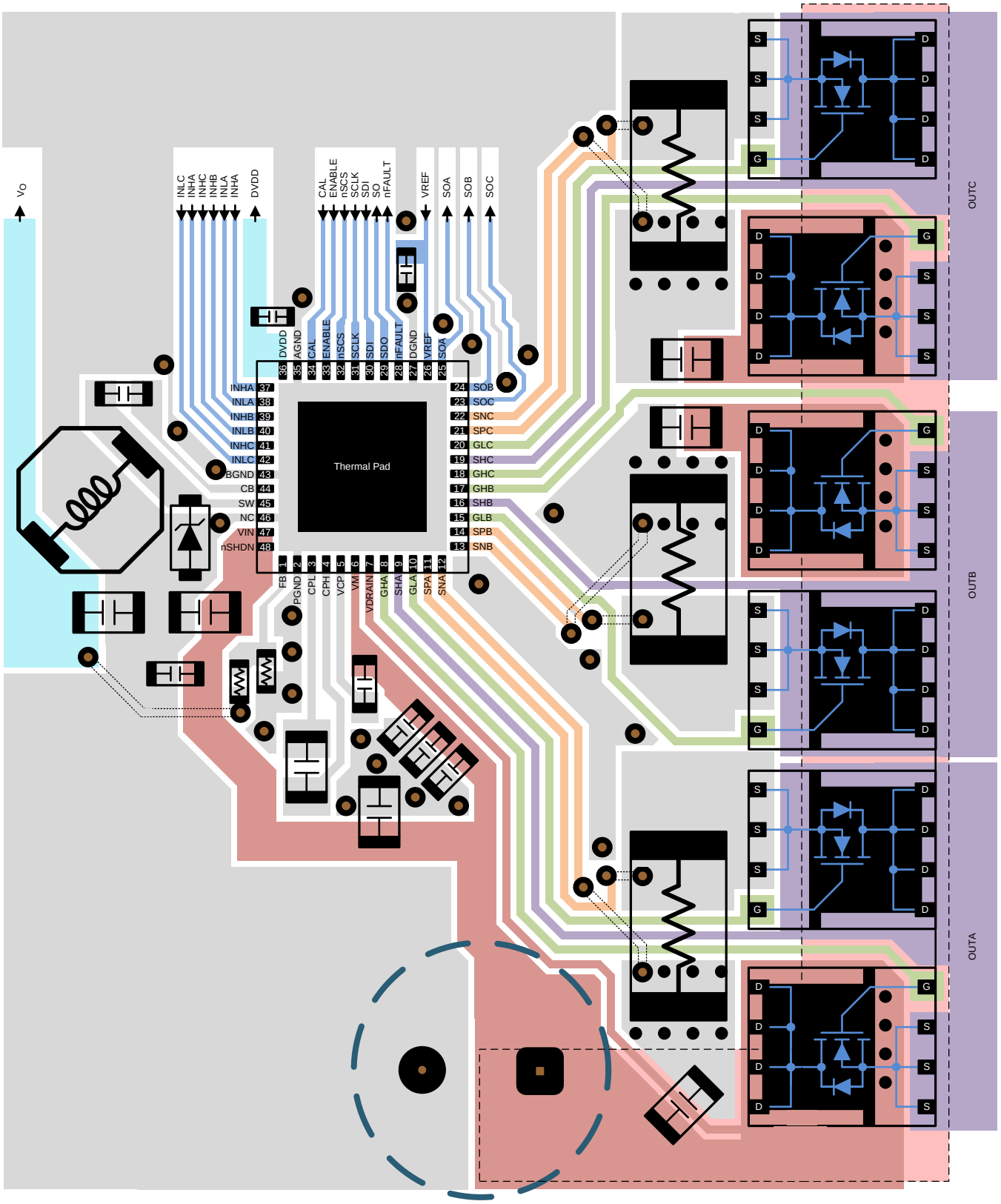


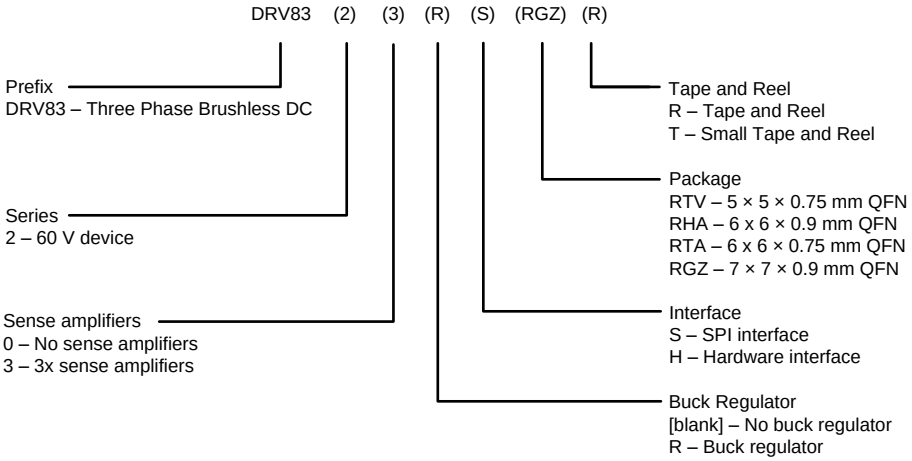
Figure 64. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

The following figure shows a legend for interpreting the complete device name:



12.2 Documentation Support

12.2.1 Related Documentation

- *AN-1149 Layout Guidelines for Switching Power Supplies*
- *CSD18536KCS 60 V N-Channel NexFET™ Power MOSFET*
- *Hardware Design Considerations for an Efficient Vacuum Cleaner using BLDC Motor*
- *Hardware Design Considerations for an Electric Bicycle using BLDC Motor*
- *Industrial Motor Drive Solution Guide*
- *Layout Guidelines for Switching Power Supplies*
- *LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency Eco-mode*
- *QFN/SON PCB Attachment*
- *Sensored 3-Phase BLDC Motor Control Using MSP430™*
- *Understanding IDRIVE and TDRIVE In TI Motor Gate Drivers*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 23. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8320	Click here	Click here	Click here	Click here	Click here
DRV8320R	Click here	Click here	Click here	Click here	Click here
DRV8323	Click here	Click here	Click here	Click here	Click here
DRV8323R	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

Eco-mode, NexFET, MSP430, E2E are trademarks of Texas Instruments.
SIMPLE SWITCHER is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8320HRTVR	ACTIVE	WQFN	RTV	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8320H	Samples
DRV8320HRTVT	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8320H	Samples
DRV8320RHRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8320RH	Samples
DRV8320RHRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8320RH	Samples
DRV8320RSRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8320RS	Samples
DRV8320RSRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8320RS	Samples
DRV8320SRTVR	ACTIVE	WQFN	RTV	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8320S	Samples
DRV8320SRTVT	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8320S	Samples
DRV8323HRTAR	ACTIVE	WQFN	RTA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8323H	Samples
DRV8323HRTAT	ACTIVE	WQFN	RTA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8323H	Samples
DRV8323RHRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RH	Samples
DRV8323RHRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RH	Samples
DRV8323RSRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS	Samples
DRV8323RSRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS	Samples
DRV8323SRTAR	ACTIVE	WQFN	RTA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8323S	Samples
DRV8323SRTAT	ACTIVE	WQFN	RTA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 125	DRV8323S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

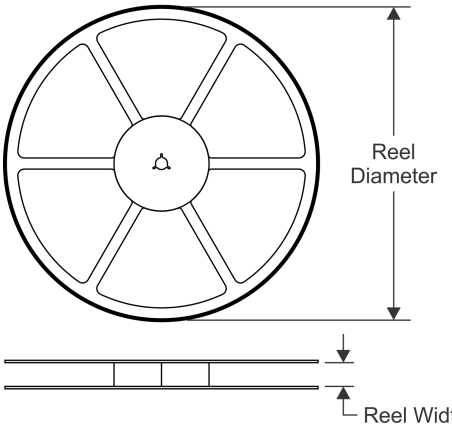
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

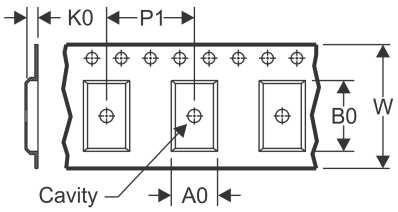
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

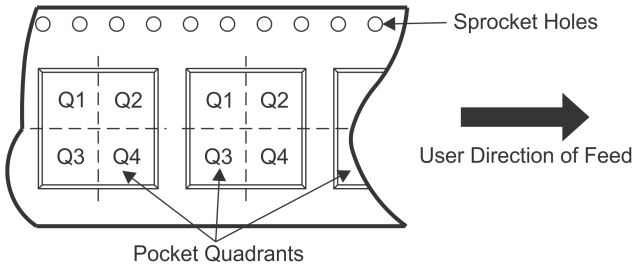


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

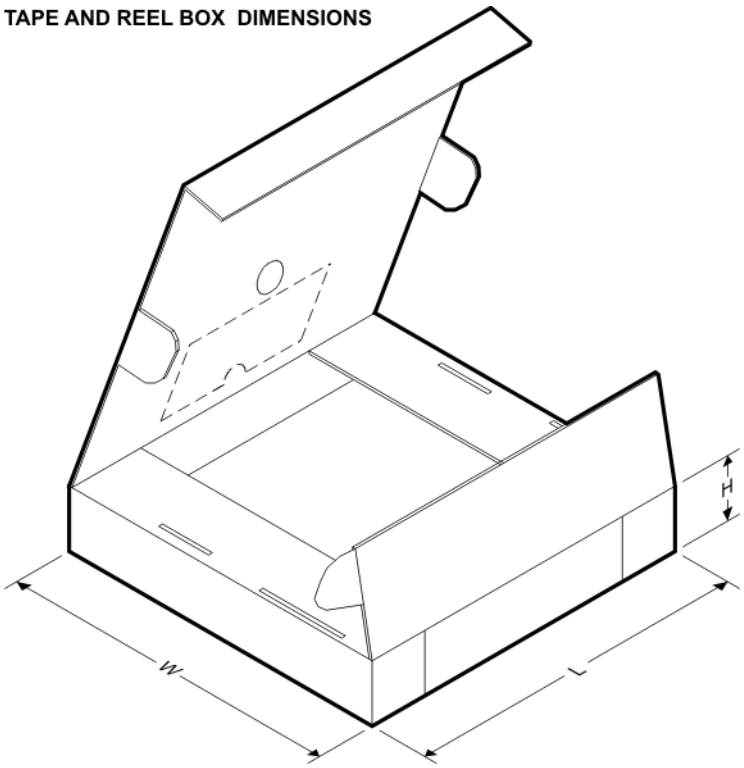
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8320HRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8320HRTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8320RHRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320RHRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320RSRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320RSRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320SRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8320SRTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8323RHRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DRV8323RHRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DRV8323RSRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DRV8323RSRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

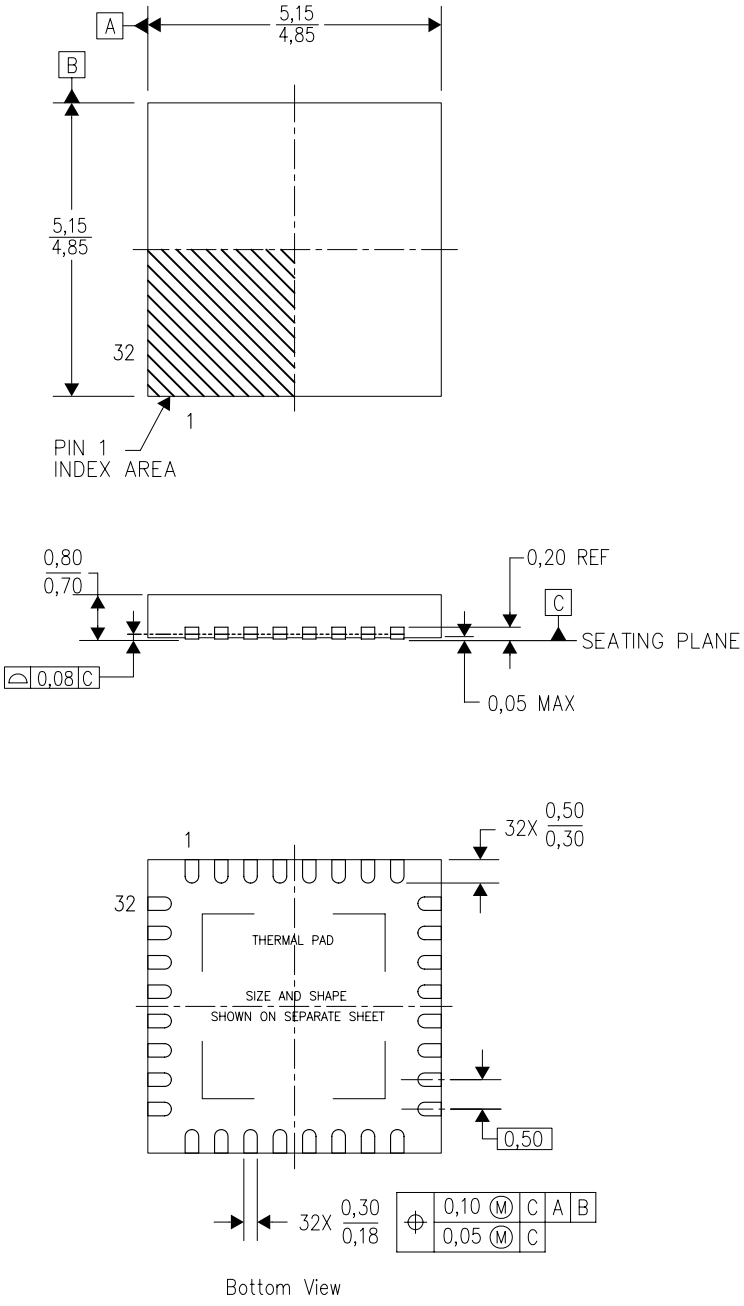
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8320HRTVR	WQFN	RTV	32	3000	367.0	367.0	35.0
DRV8320HRTVT	WQFN	RTV	32	250	210.0	185.0	35.0
DRV8320RHRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DRV8320RHRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
DRV8320RSRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DRV8320RSRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
DRV8320SRTVR	WQFN	RTV	32	3000	367.0	367.0	35.0
DRV8320SRTVT	WQFN	RTV	32	250	210.0	185.0	35.0
DRV8323RHRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
DRV8323RHRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
DRV8323RSRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
DRV8323RSRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

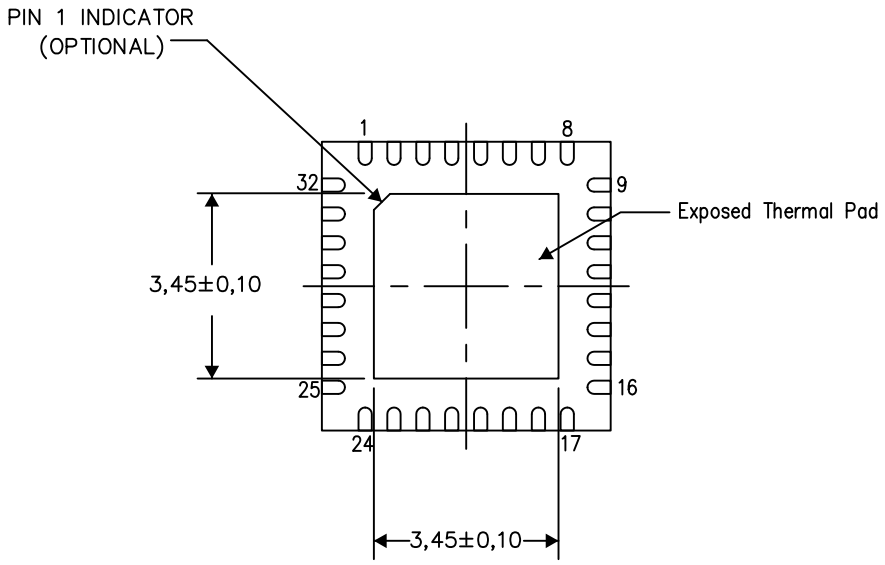
RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



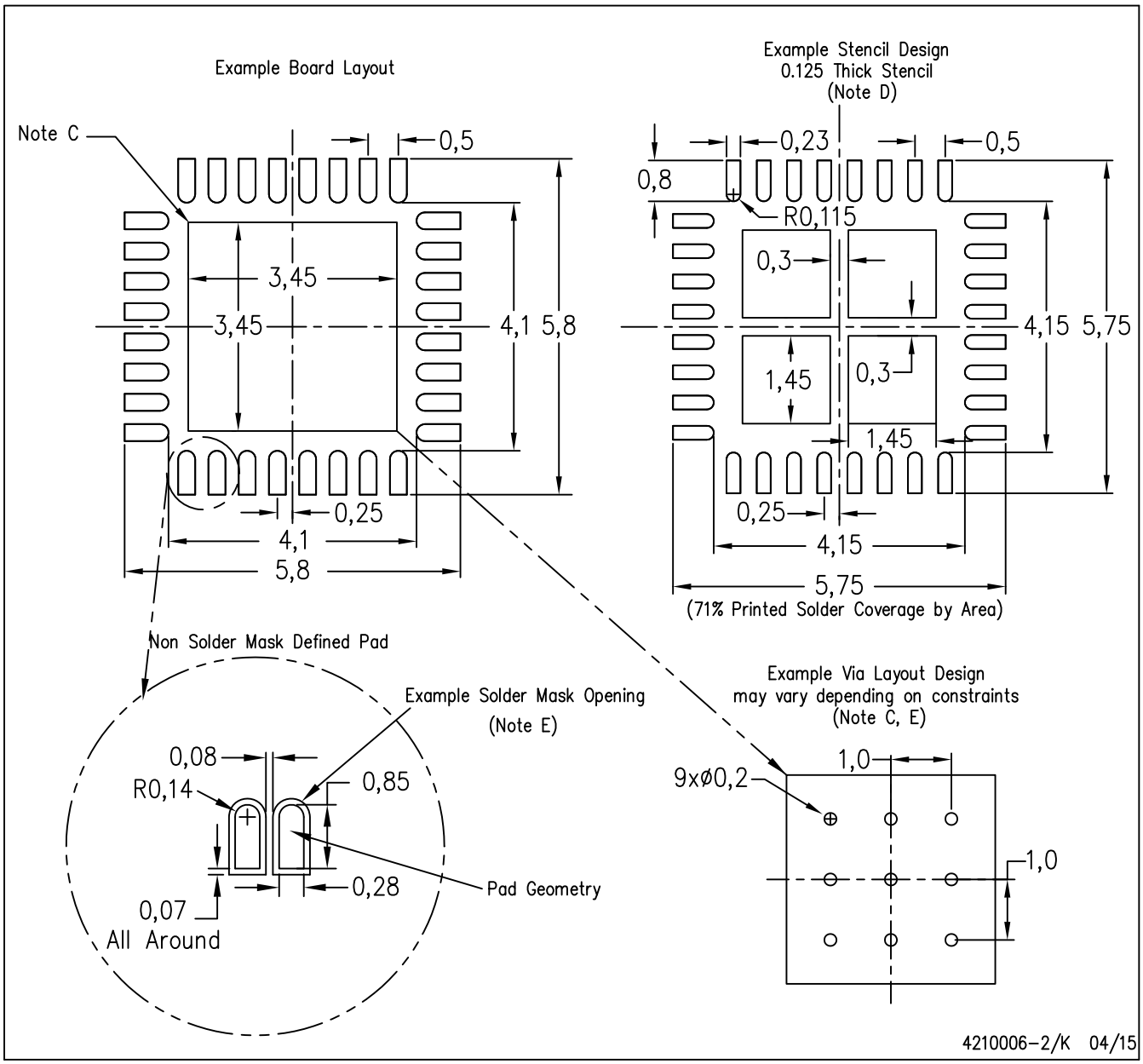
Bottom View

Exposed Thermal Pad Dimensions

4206250–2/Q 05/15

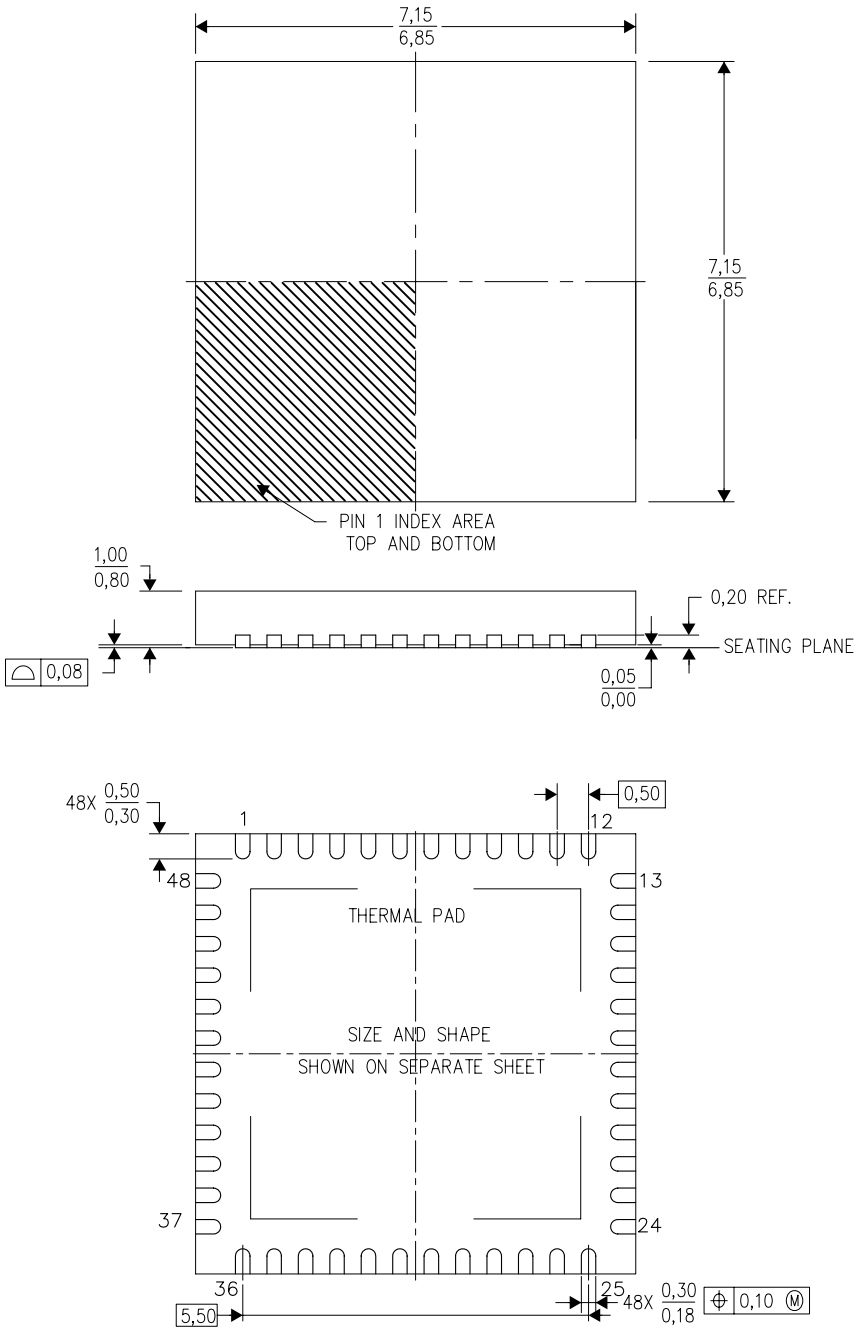
NOTE: All linear dimensions are in millimeters

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

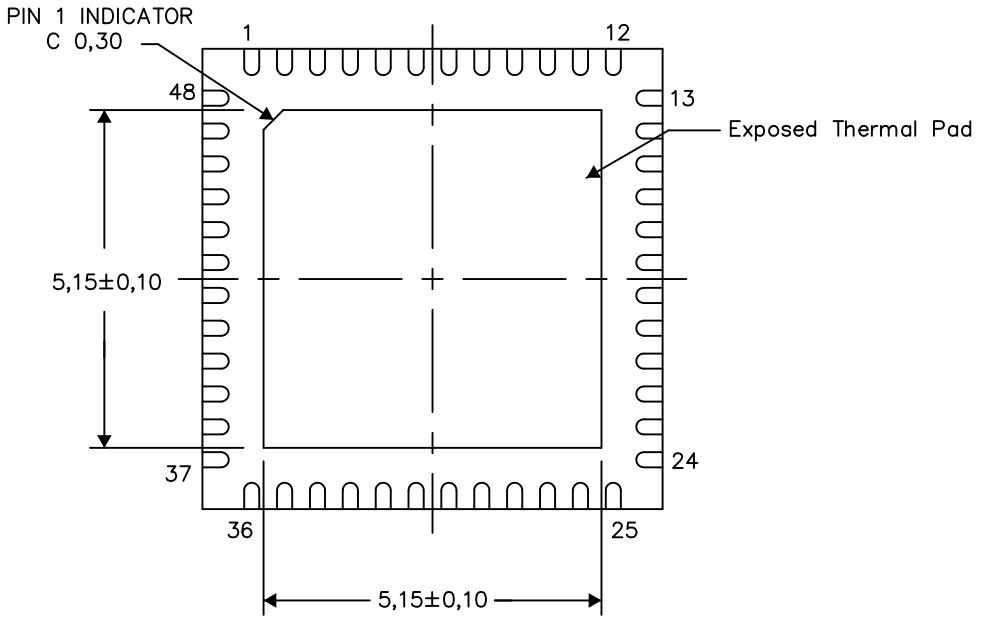
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



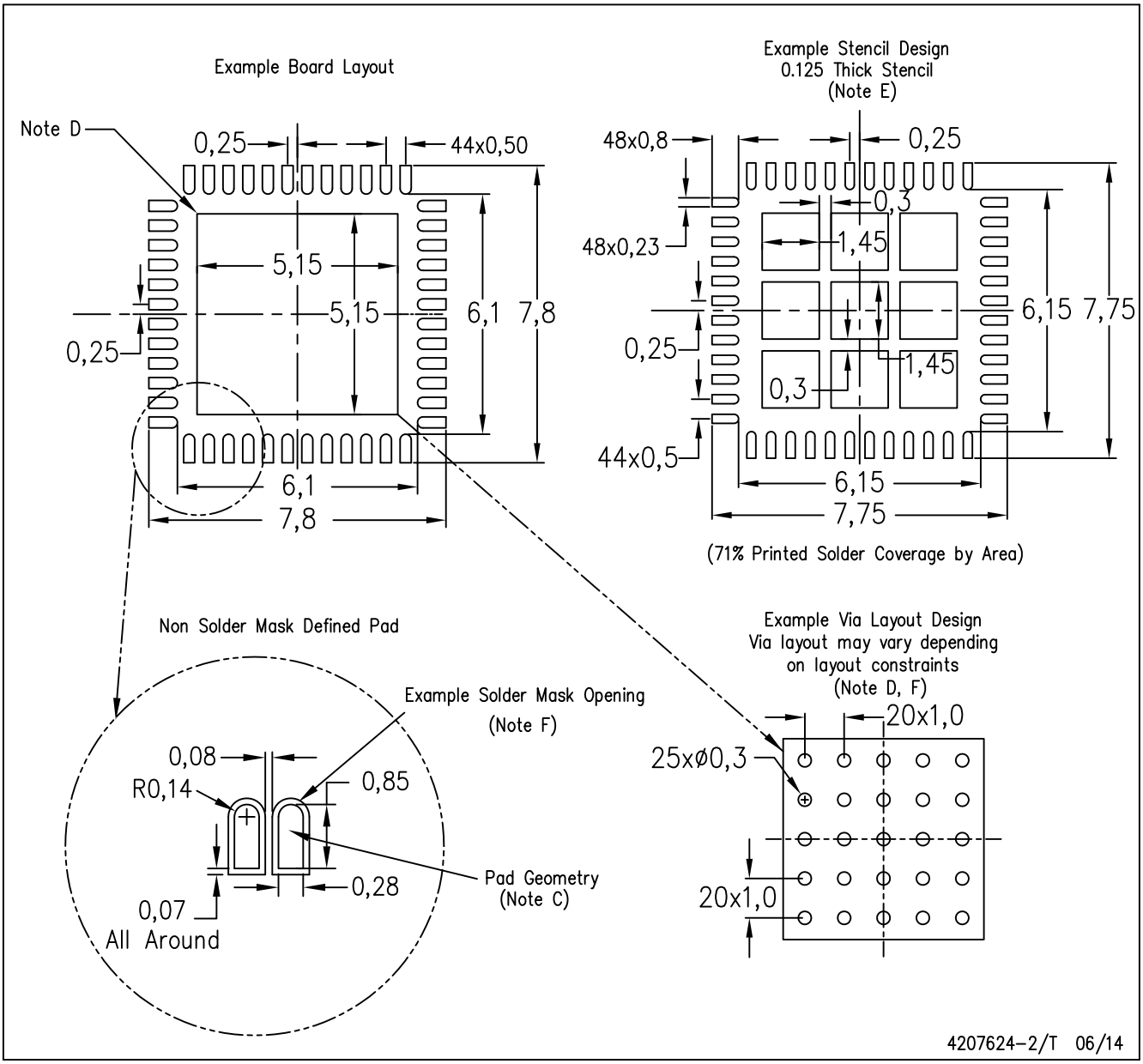
Bottom View

Exposed Thermal Pad Dimensions

4206354–2/Z 03/15

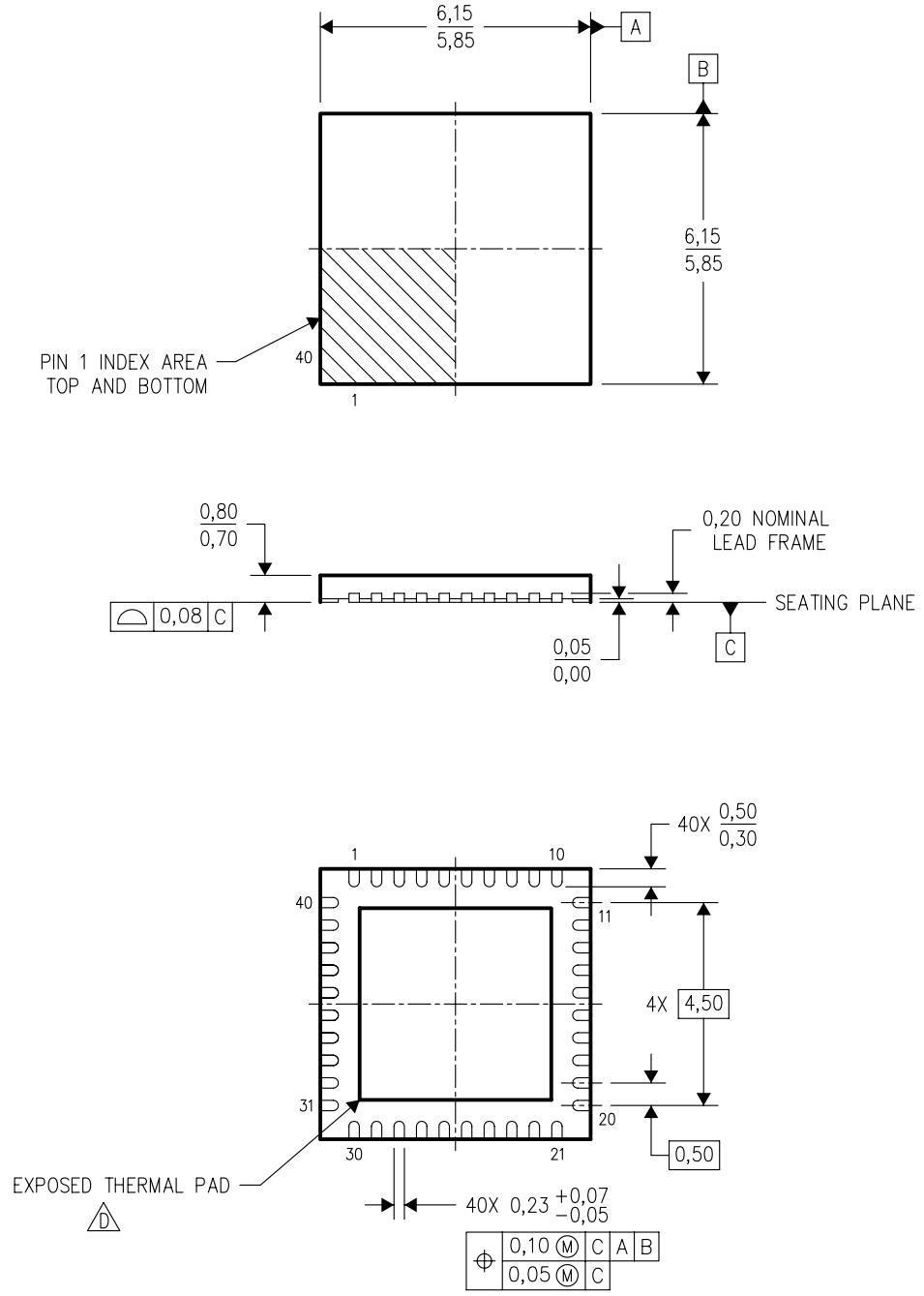
NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



4204422/B 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

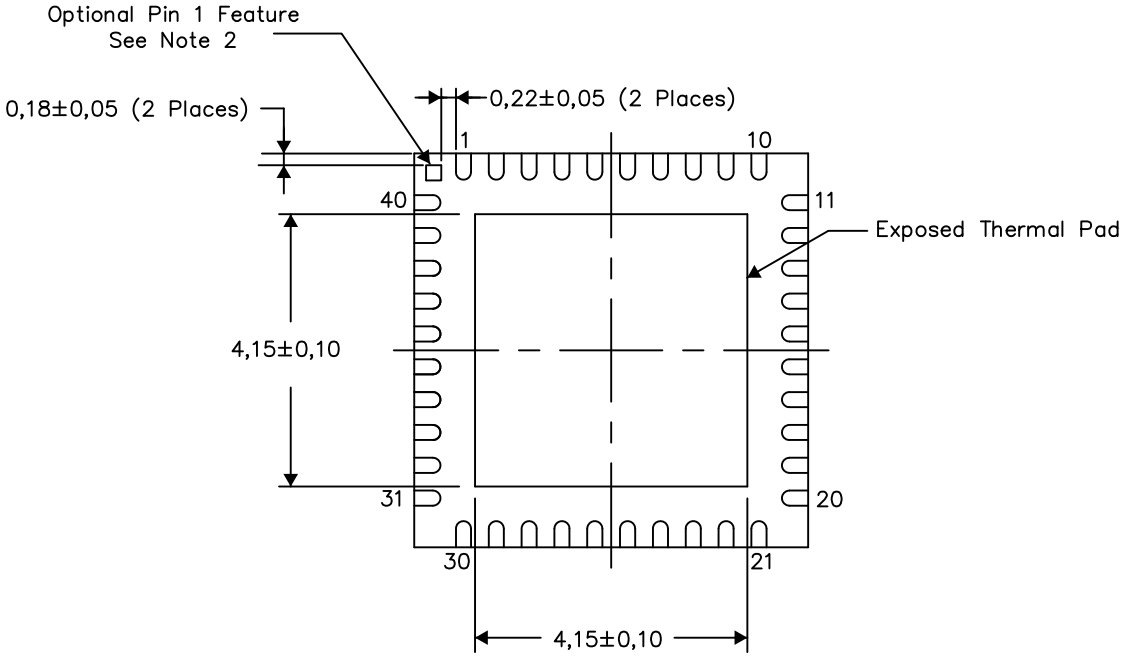
RTA (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

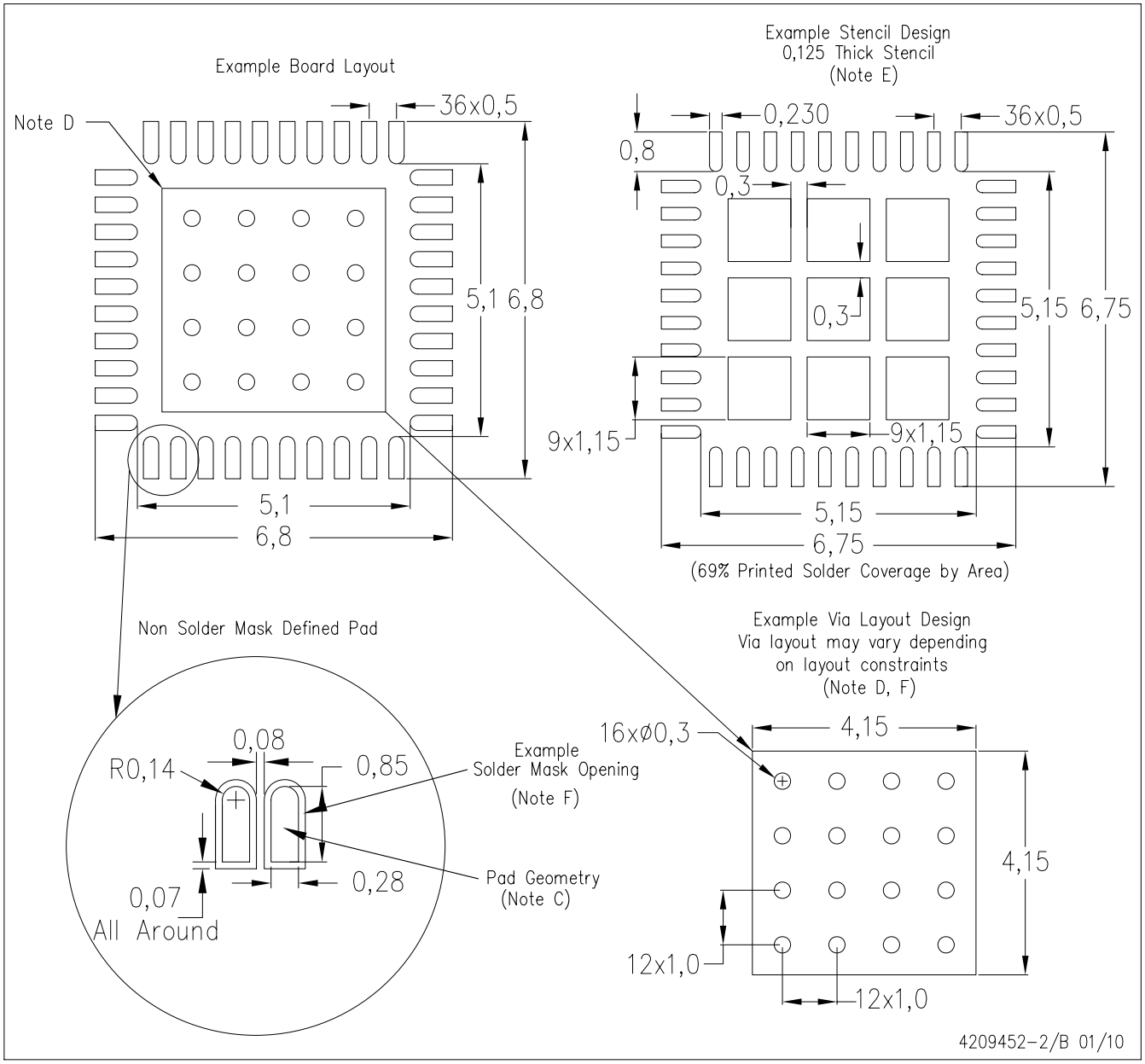
Exposed Thermal Pad Dimensions

4206335–2/F 04/14

NOTES:

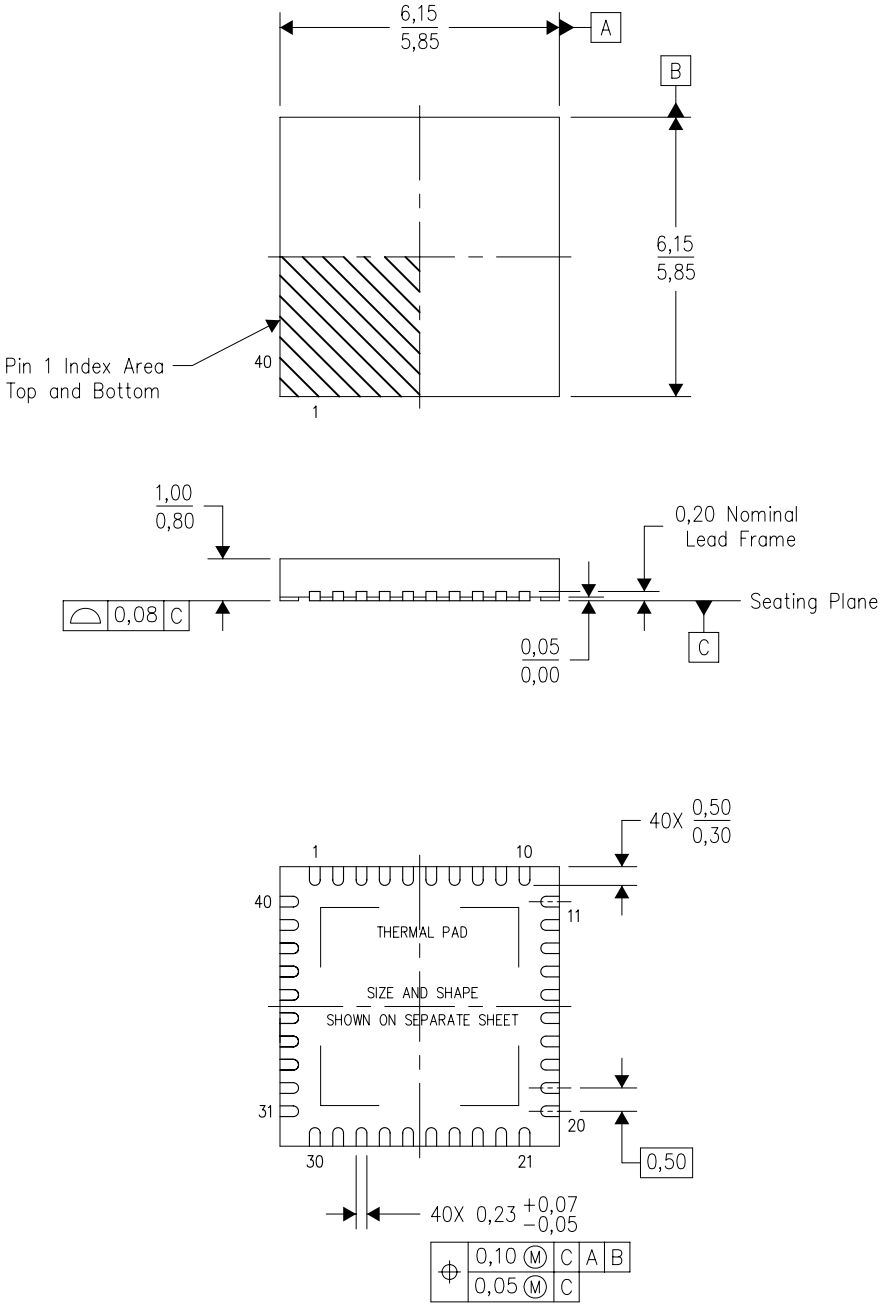
1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RTA (S–PWQFN–N40)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

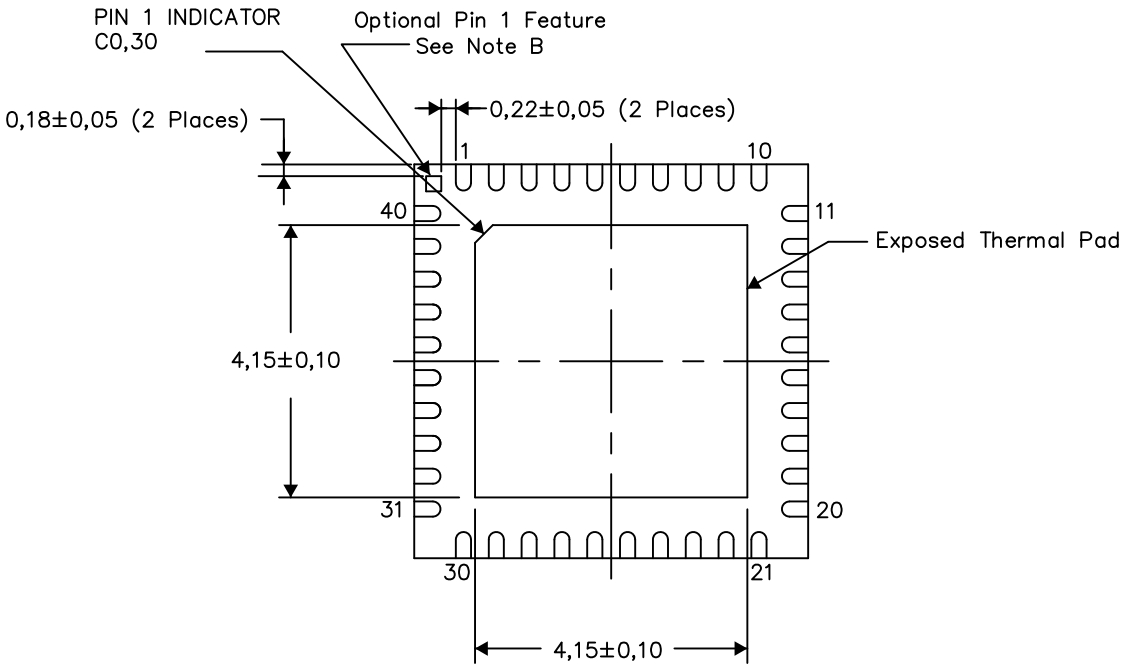
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

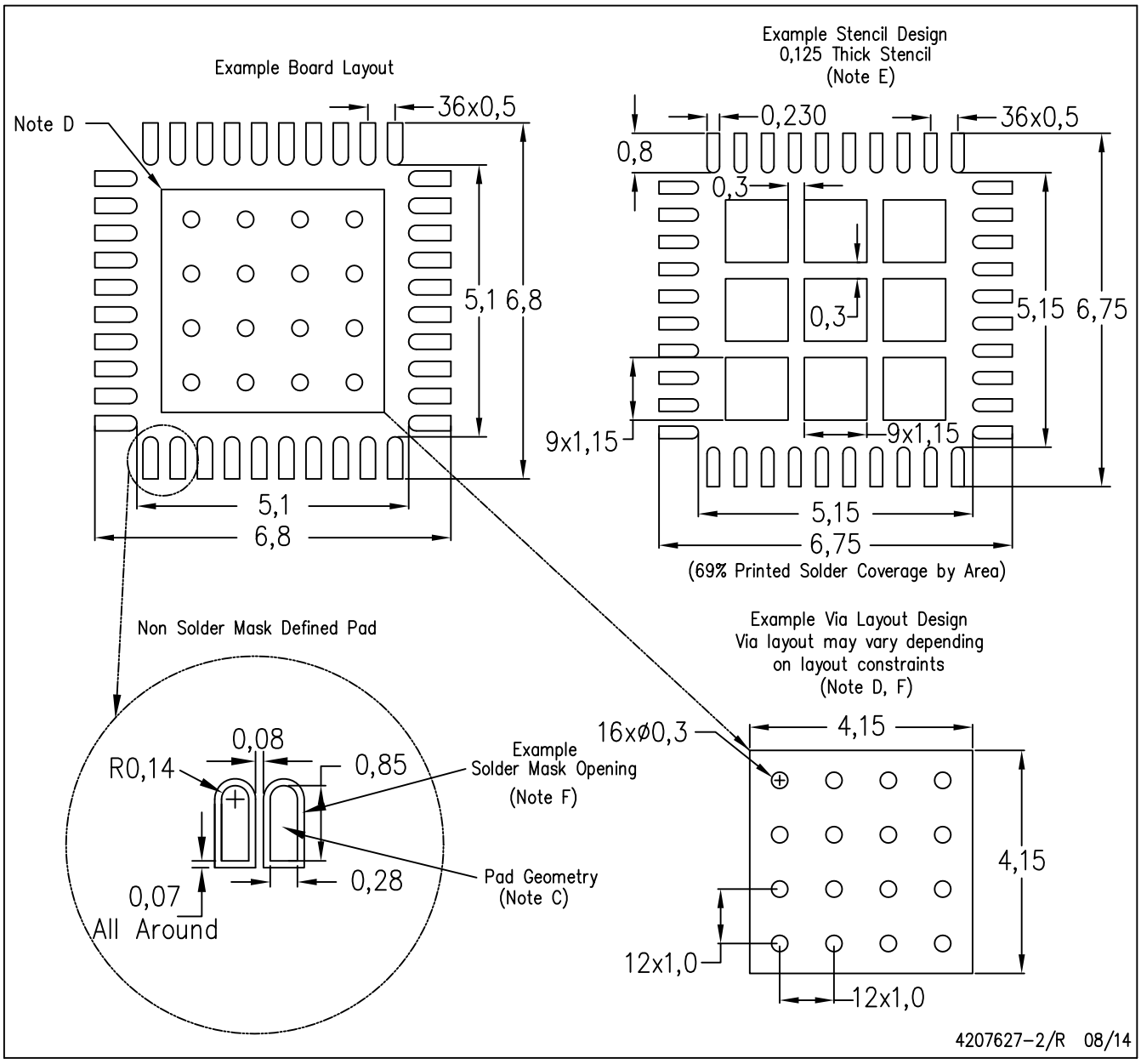
Exposed Thermal Pad Dimensions

4206355–2/X 08/14

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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