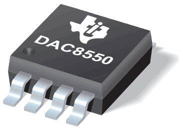


16-BIT, ULTRA-LOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy: 3LSB**
- **Glitch Energy: 0.1nV-s**
- ***Micro*Power Operation: 140µA at 2.7V**
- **Power-On Reset to Midscale**
- **Power Supply: +2.7V to +5.5V**
- **16-Bit Monotonic Over Temperature**
- **Settling Time: 10µs to ±0.003% FSR**
- **Low-Power Serial Interface with Schmitt-Triggered Inputs**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Output Amplifier**
- **Power-Down Capability**
- **2's Complement Input**
- **$\overline{\text{SYNC}}$ Interrupt Facility**
- **Drop-In Compatible with DAC8531/01 and DAC8551 (Binary Input)**
- **Available in a Tiny MSOP-8 Package**

APPLICATIONS

- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo-Control**
- **PC Peripherals**
- **Portable Instrumentation**
- **Programmable Attenuation**

DESCRIPTION

The DAC8550 is a small, low-power, voltage output, 16-bit digital-to-analog converter (DAC). It is monotonic, provides good linearity, and minimizes undesired code-to-code transient voltages. The DAC8550 uses a versatile, 3-wire serial interface that operates at clock rates of up to 30MHz and is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

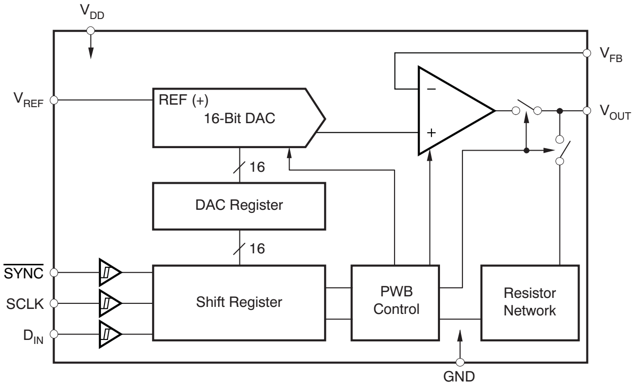
The DAC8550 requires an external reference voltage to set its output range. The DAC8550 incorporates a power-on reset circuit that ensures that the DAC output powers up at midscale and remains there until a valid write takes place to the device. The DAC8550 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 200nA at 5V.

The low-power consumption of this device in normal operation makes it ideal for portable, battery-operated equipment. Power consumption is 0.38mW at 2.7V, reducing to less than 1µW in power-down mode.

The DAC8550 is available in an MSOP-8 package.

For additional flexibilty, see the DAC8551, a binary-coded counterpart to the DAC8550.

FUNCTIONAL BLOCK DIAGRAM



SPI, QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor.
All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8550	±12	±1	MSOP-8	DGK	–40°C to +105°C	D80	DAC8550IDGKT	Tape and Reel, 250
							DAC8550IDGKR	Tape and Reel, 2500
DAC8550B	±8	±1	MSOP-8	DGK	–40°C to +105°C	D80	DAC8550IBDGKT	Tape and Reel, 250
							DAC8550IBDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	UNIT
Supply voltage, V_{DD} to GND	–0.3V to 6V
Digital input voltage range, V_I to GND	–0.3V to +V_{DD} + 0.3V
Output voltage, V_{OUT} to GND	–0.3V to +V_{DD} + 0.3V
Operating free-air temperature range, T_A	–40°C to +105°C
Storage temperature range, T_{STG}	–65°C to +150°C
Junction temperature range, $T_{J(max)}$	150°C
Power dissipation (DGK package)	$(T_J\text{max} – T_A)/\theta_{JA}$
Thermal impedance, θ_{JA}	206°C/W
Thermal impedance, θ_{JC}	44°C/W

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, –40°C to +105°C range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)							
	Resolution			16			Bits
E_L	Relative accuracy	Measured by line passing through codes –32283 and +32063	DAC8550		±3	±12	LSB
			DAC8550B		±3	±8	LSB
E_D	Differential nonlinearity	16-bit Monotonic			±0.25	±1	LSB
E_O	Zero-code error	Measured by line passing through codes –32283 and +32063.			±2	±12	mV
E_{FS}	Full-scale error				±0.05	±0.5	% of FSR
E_G	Gain error				±0.02	±0.2	% of FSR
	Zero-code error drift				±5		µV/°C
	Gain temperature coefficient				±1		ppm of FSR/°C
PSRR	Power-supply rejection ratio	R_L = 2kΩ, C_L = 200pF			0.75		mV/V

(1) Linearity calculated using a reduced code range of –32283 to +32063; output unloaded.

ELECTRICAL CHARACTERISTICS (continued)

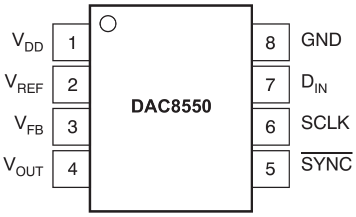
V_{DD} = 2.7V to 5.5V, –40°C to +105°C range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS (2)						
V_O	Output voltage range		0		V_{REF}	V
t_{SD}	Output voltage settling time	To ±0.003% FSR, 1200h to 8D00h, R_L = 2kΩ, 0pF < C_L < 200pF		8	10	µs
		R_L = 2kΩ, C_L = 500pF		12		µs
SR	Slew rate			1.8		V/µs
	Capacitive load stability	R_L = ∞		470		pF
		R_L = 2kΩ		1000		pF
	Code change glitch impulse	1LSB change around major carry		0.1		nV-s
	Digital feedthrough	SCLK toggling, FSYNC high		0.1		
z_O	DC output impedance	At mid-code input		1		Ω
I_{OS}	Short-circuit current	V_{DD} = 5V		50		mA
		V_{DD} = 3V		20		
t_{ON}	Power-up time	Coming out of power-down mode, V_{DD} = 5V		2.5		µs
		Coming out of power-down mode, V_{DD} = 3V		5		
AC PERFORMANCE						
SNR	Signal-to-noise ratio	BW = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		95		dB
THD	Total harmonic distortion			–85		
SFDR	Spurious-free dynamic range			87		
SINAD	Signal-to-noise and distortion			84		
REFERENCE INPUT						
V_{REF}	Reference voltage		0		V_{DD}	V
$I_{I(REF)}$	Reference current input range	V_{REF} = V_{DD} = 5V		40	75	µA
		V_{REF} = V_{DD} = 3.6V		30	45	µA
$z_{I(REF)}$	Reference input impedance			125		kΩ
LOGIC INPUTS (3)						
Input current				±1		µA
V_{IL}	Low-level input voltage	V_{DD} = 5V			0.8	V
		V_{DD} = 3V			0.6	
V_{IH}	High-level input voltage	V_{DD} = 5V	2.4			V
		V_{DD} = 3V	2.1			
	Pin capacitance				3	pF
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
I_{DD} (normal mode)		Input code equals mid-scale, no load, does not include reference current				
	V_{DD} = 3.6V to 5.5V	V_{IH} = V_{DD} and V_{IL} = GND		160	250	µA
	V_{DD} = 2.7V to 3.6V			140	240	
I_{DD} (all power-down modes)		V_{IH} = V_{DD} and V_{IL} = GND				
	V_{DD} = 3.6V to 5.5V			0.2	2	µA
	V_{DD} = 2.7V to 3.6V			0.05	2	
POWER EFFICIENCY						
I_{OUT}/I_{DD}		I_{LOAD} = 2mA, V_{DD} = 5V		89		%
TEMPERATURE RANGE						
Specified performance			–40		+105	°C

(2) Specified by design and characterization, not production tested.
(3) Specified by design and characterization, not production tested.

PIN CONFIGURATION

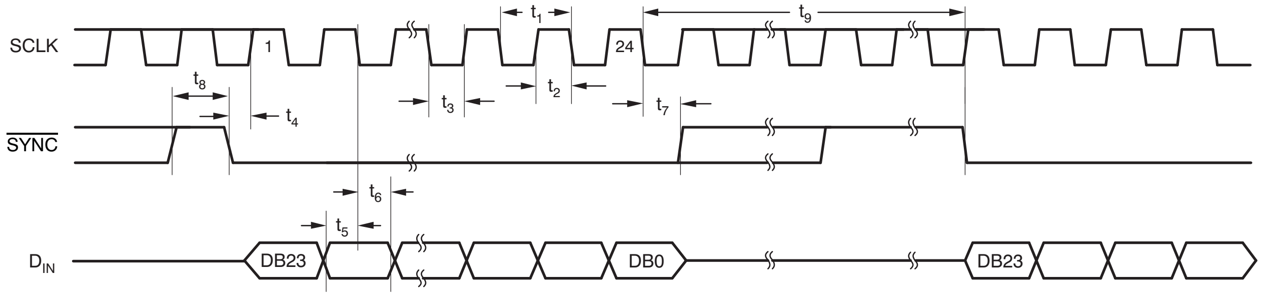
MSOP-8
(Top View)



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Power-supply input, 2.7V to 5.5V.
2	V_{REF}	Reference voltage input.
3	V_{FB}	Feedback connection for the output amplifier.
4	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{SYNC}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{SYNC}$ is taken HIGH before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8550). Schmitt-Trigger logic input.
6	SCLK	Serial clock input. Data can be transferred at rates up to 30MHz. Schmitt-Trigger logic input.
7	D_{IN}	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
8	GND	Ground reference point for all circuitry on the part.

SERIAL WRITE OPERATION



TIMING CHARACTERISTICS(1)(2)

V_{DD} = 2.7V to 5.5V, all specifications –40°C to +105°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1 (3)	SCLK cycle time	V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			
t_2	SCLK HIGH time	V_{DD} = 2.7V to 3.6V	13			ns
		V_{DD} = 3.6V to 5.5V	13			
t_3	SCLK LOW time	V_{DD} = 2.7V to 3.6V	22.5			ns
		V_{DD} = 3.6V to 5.5V	13			
t_4	$\overline{\text{SYNC}}$ to SCLK rising edge setup time	V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			
t_5	Data setup time	V_{DD} = 2.7V to 3.6V	5			ns
		V_{DD} = 3.6V to 5.5V	5			
t_6	Data hold time	V_{DD} = 2.7V to 3.6V	4.5			ns
		V_{DD} = 3.6V to 5.5V	4.5			
t_7	24th SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			
t_8	Minimum $\overline{\text{SYNC}}$ HIGH time	V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			
t_9	24th SCLK falling edge to $\overline{\text{SYNC}}$ falling edge	V_{DD} = 2.7V to 5.5V	100			ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See Serial Write Operation Timing Diagram.
(3) Maximum SCLK frequency is 30MHz at V_{DD} = 3.6V to 5.5V and 20MHz at V_{DD} = 2.7V to 3.6V.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (-40°C)

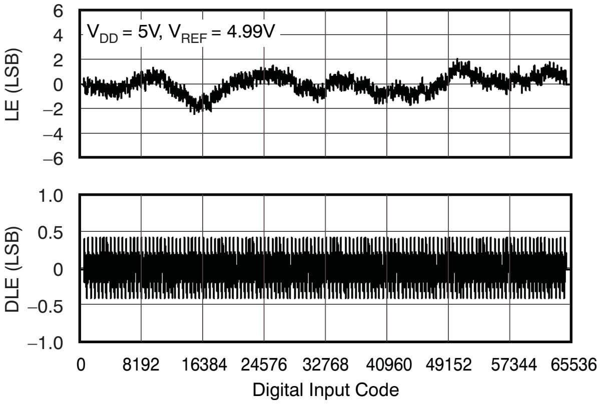


Figure 1.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

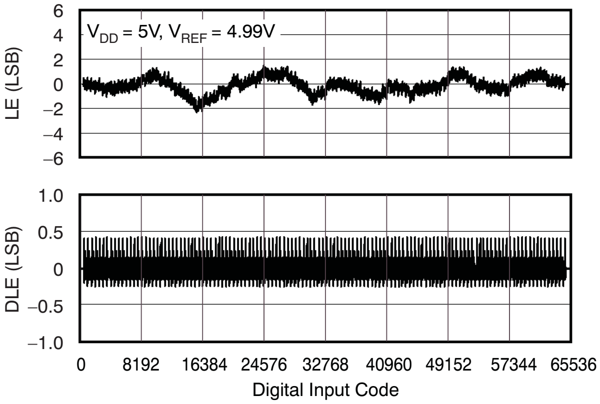


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

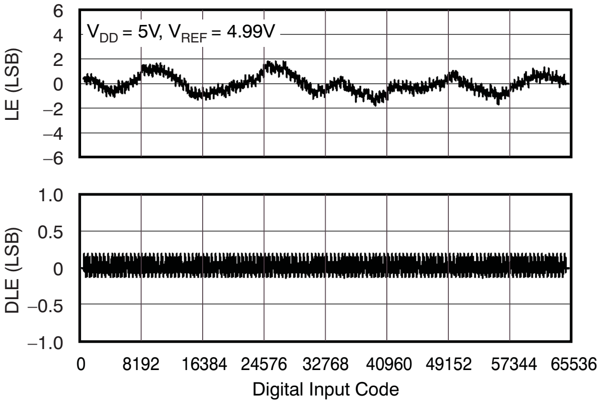


Figure 3.

ZERO-SCALE ERROR vs TEMPERATURE

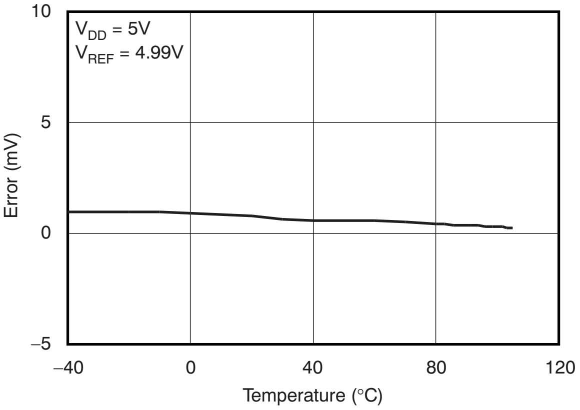


Figure 4.

FULL-SCALE ERROR vs TEMPERATURE

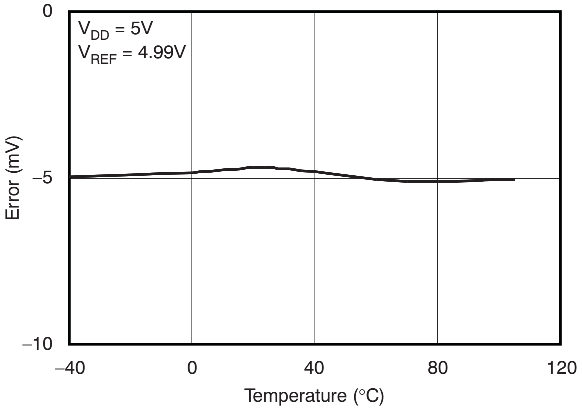


Figure 5.

SOURCE AND SINK CURRENT CAPABILITY

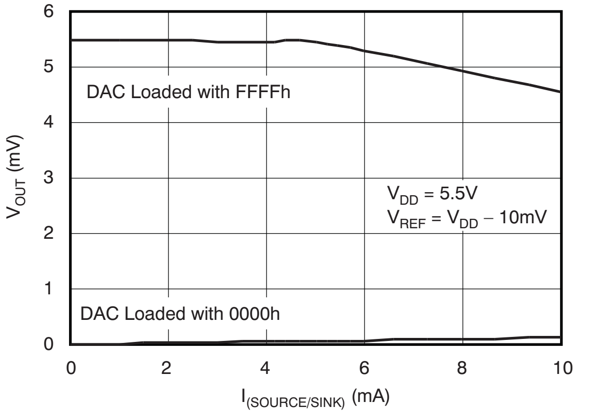


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = +25°C, unless otherwise noted.

SUPPLY CURRENT vs DIGITAL INPUT CODE

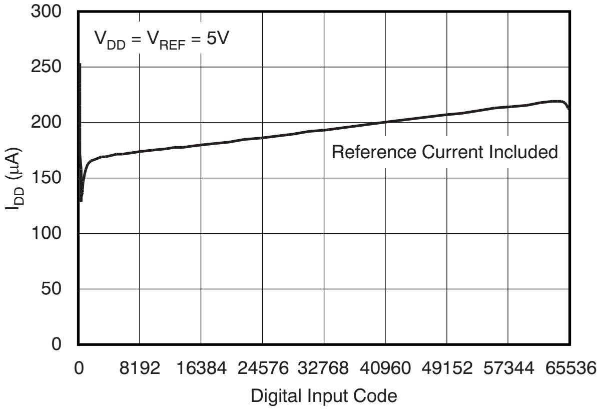


Figure 7.

POWER-SUPPLY CURRENT vs TEMPERATURE

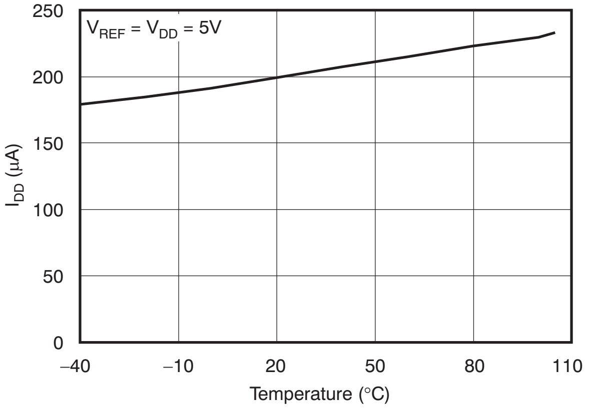


Figure 8.

SUPPLY CURRENT vs SUPPLY VOLTAGE

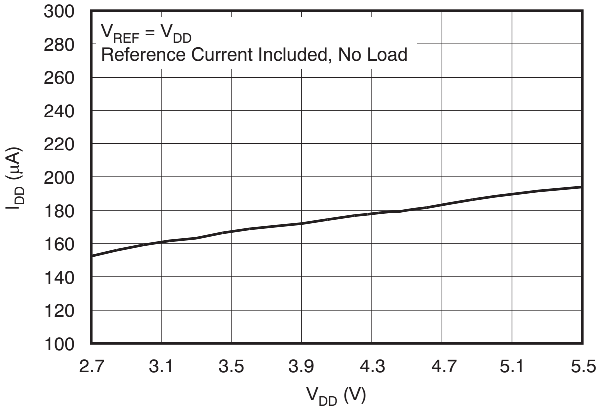


Figure 9.

POWER-DOWN CURRENT vs SUPPLY VOLTAGE

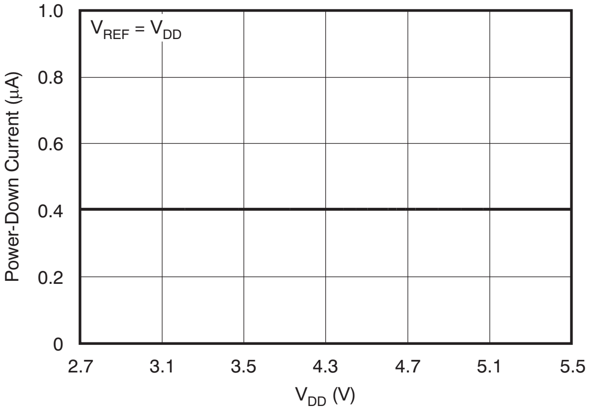


Figure 10.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

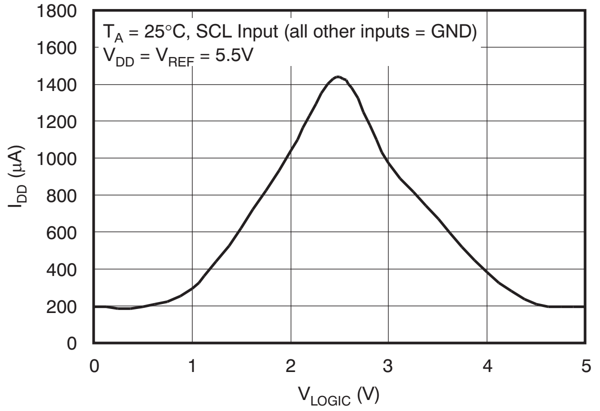


Figure 11.

FULL-SCALE SETTLING TIME: 5V RISING EDGE

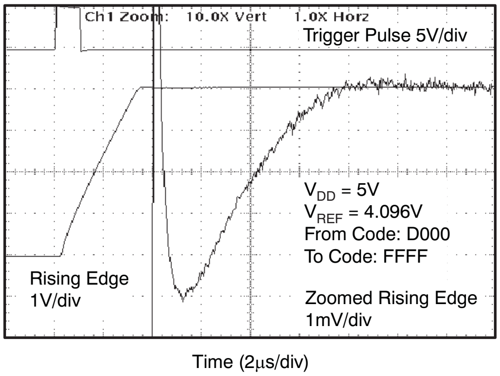


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = +25°C, unless otherwise noted.

FULL-SCALE SETTLING TIME: 5V FALLING EDGE

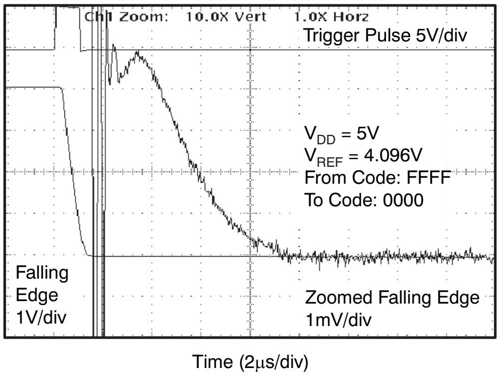


Figure 13.

HALF-SCALE SETTLING TIME: 5V RISING EDGE

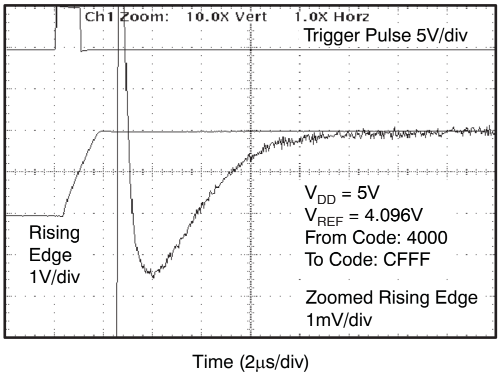


Figure 14.

HALF-SCALE SETTLING TIME: 5V FALLING EDGE

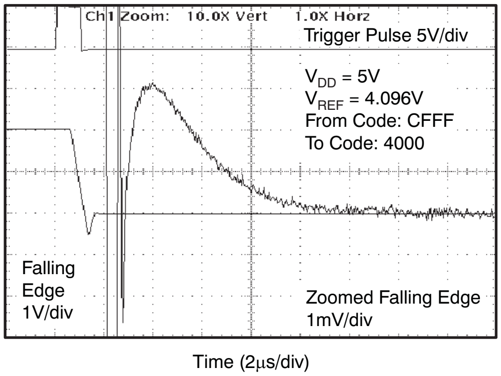


Figure 15.

GLITCH ENERGY: 5V, 1LSB STEP, RISING EDGE

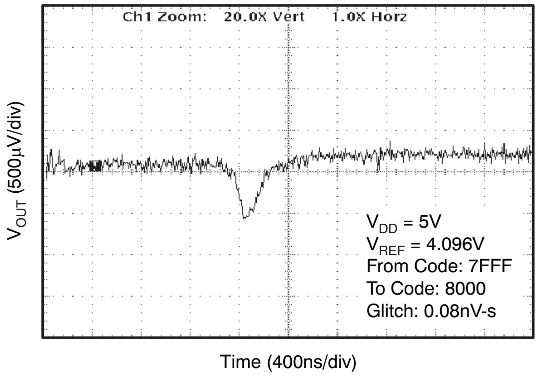


Figure 16.

GLITCH ENERGY: 5V, 1LSB STEP, FALLING EDGE

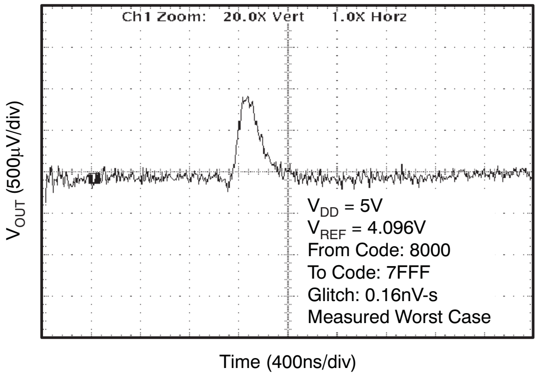


Figure 17.

GLITCH ENERGY: 5V, 16LSB STEP, RISING EDGE

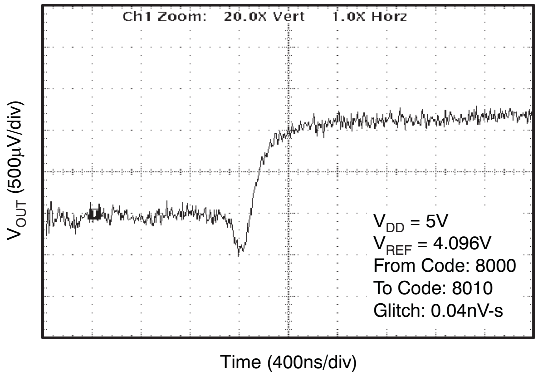


Figure 18.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = +25°C, unless otherwise noted.

GLITCH ENERGY: 5V, 16LSB STEP, FALLING EDGE

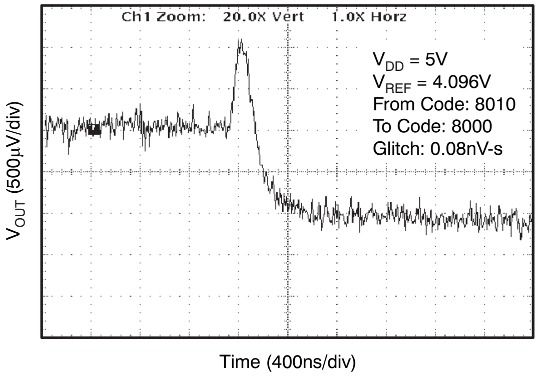


Figure 19.

GLITCH ENERGY: 5V, 256LSB STEP, RISING EDGE

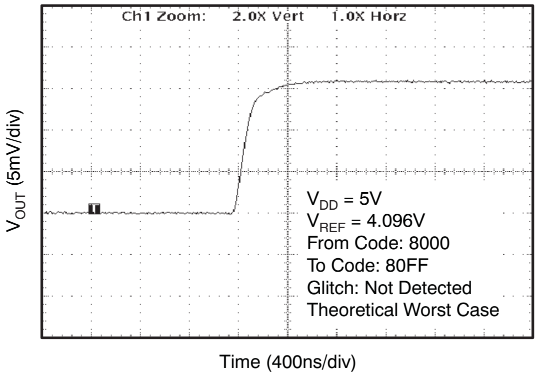


Figure 20.

GLITCH ENERGY: 5V, 256LSB STEP, FALLING EDGE

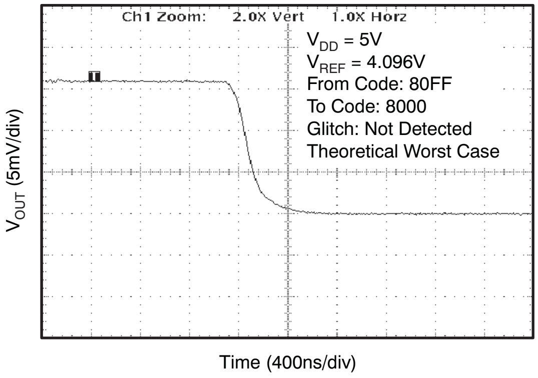


Figure 21.

TOTAL HARMONIC DISTORTION
vs OUTPUT FREQUENCY

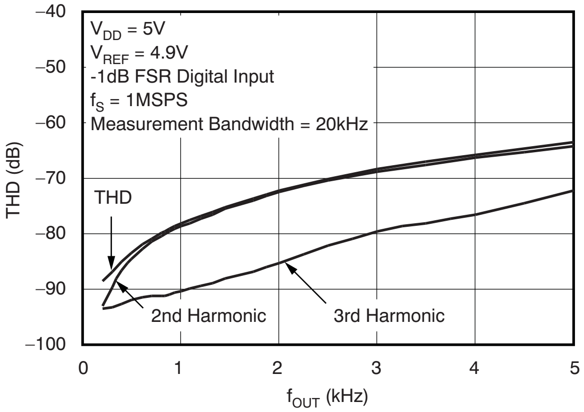


Figure 22.

SIGNAL-TO-NOISE RATIO
vs OUTPUT FREQUENCY

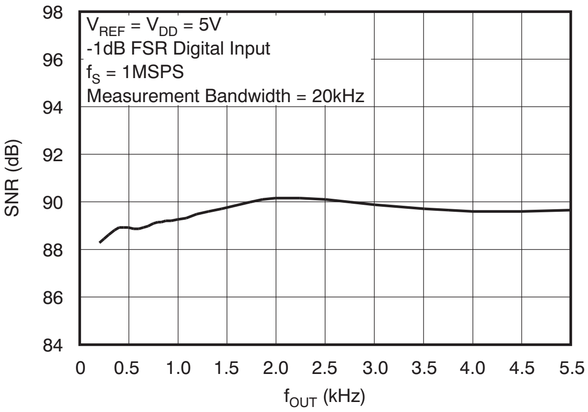


Figure 23.

POWER SPECTRAL DENSITY

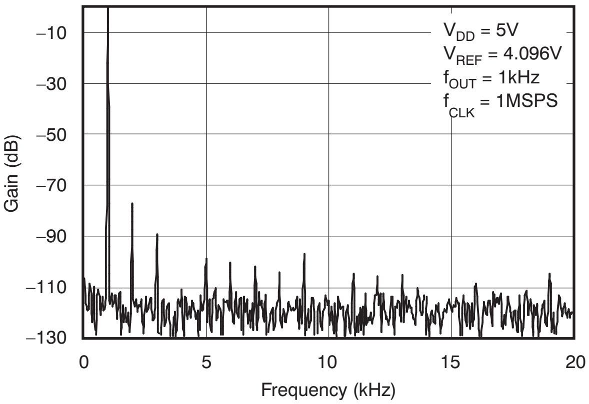


Figure 24.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = +25°C, unless otherwise noted.

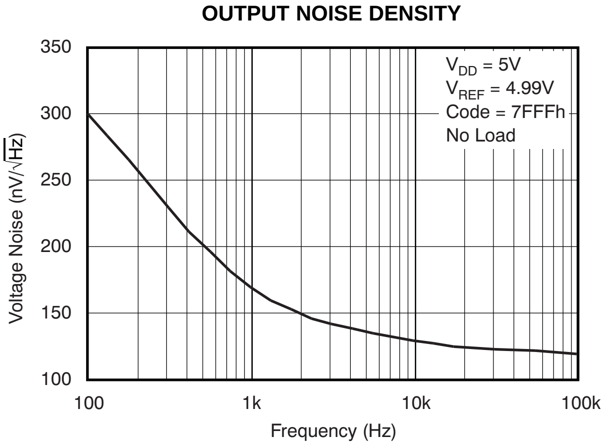
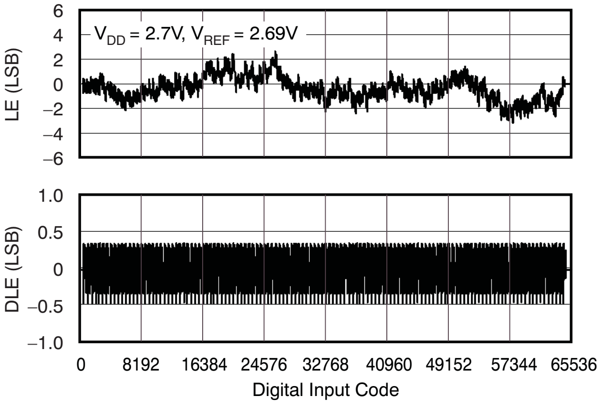


Figure 25.

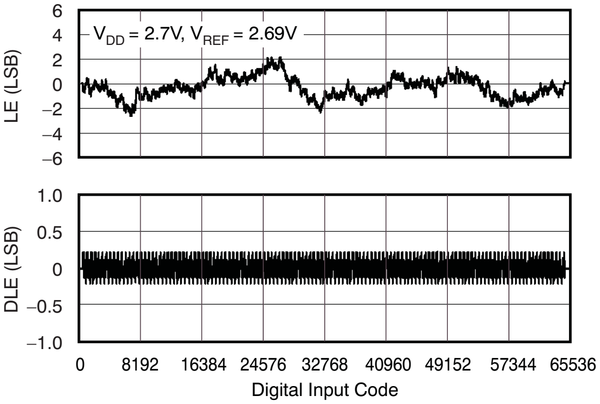
TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V

At T_A = +25°C, unless otherwise noted.



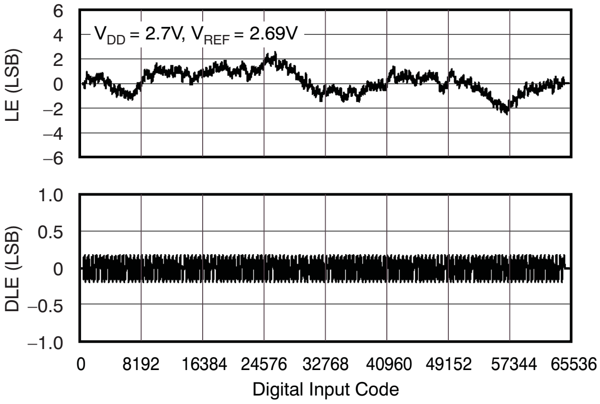
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (-40°C)

Figure 26.



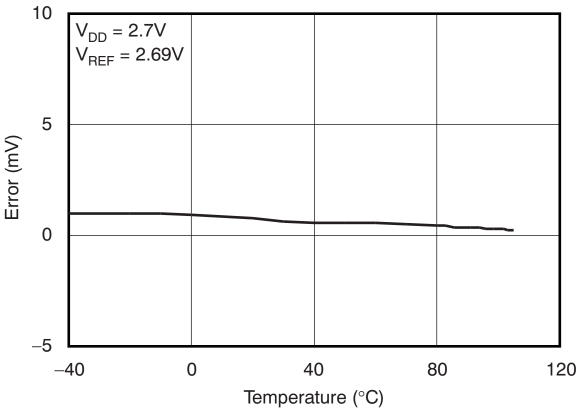
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

Figure 27.



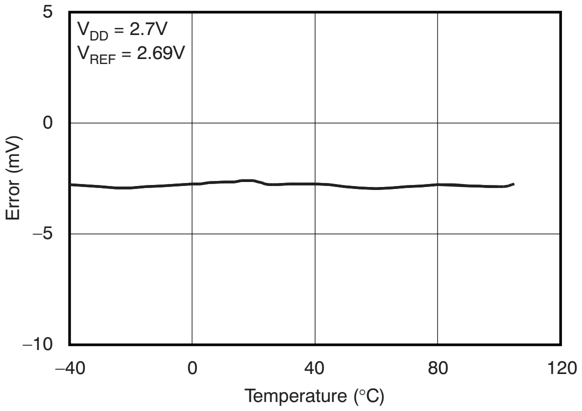
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

Figure 28.



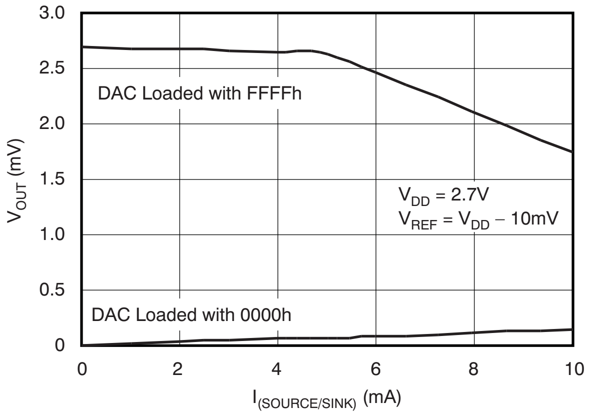
ZERO-SCALE ERROR vs TEMPERATURE

Figure 29.



FULL-SCALE ERROR vs TEMPERATURE

Figure 30.



SOURCE AND SINK CURRENT CAPABILITY

Figure 31.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V (continued)

At T_A = +25°C, unless otherwise noted.

SUPPLY CURRENT vs DIGITAL INPUT CODE

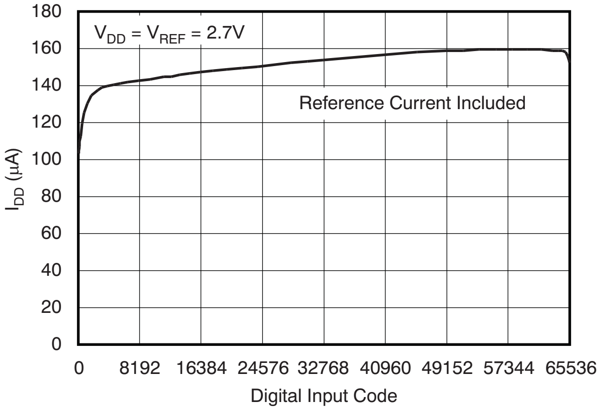


Figure 32.

POWER-SUPPLY CURRENT vs TEMPERATURE

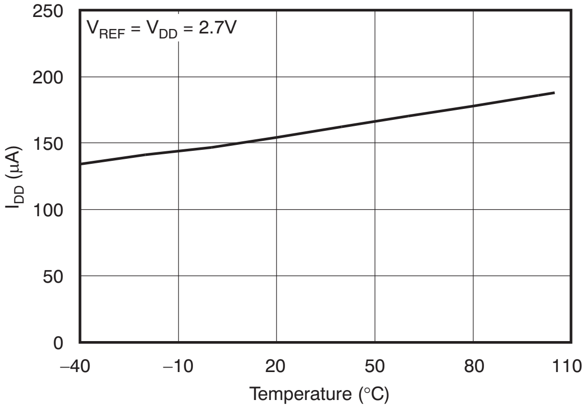


Figure 33.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

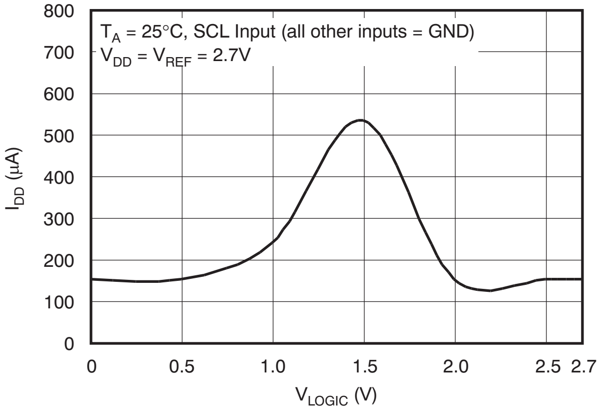


Figure 34.

FULL-SCALE SETTLING TIME: 2.7V RISING EDGE

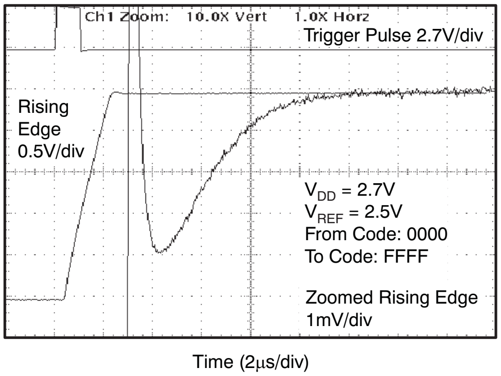


Figure 35.

FULL-SCALE SETTLING TIME: 2.7V FALLING EDGE

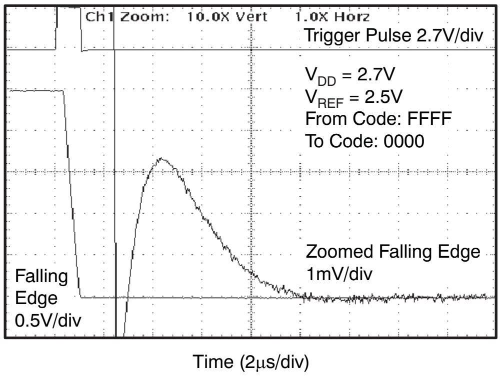


Figure 36.

HALF-SCALE SETTLING TIME: 2.7V RISING EDGE

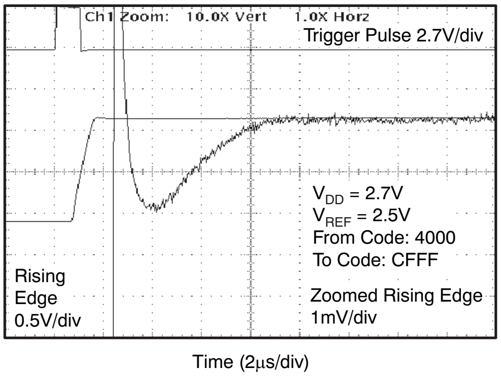


Figure 37.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V (continued)

At T_A = +25°C, unless otherwise noted.

HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE

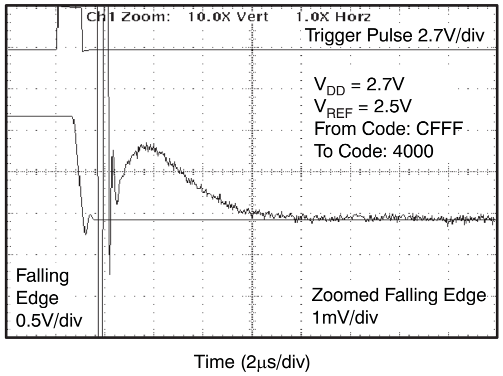


Figure 38.

GLITCH ENERGY: 2.7V, 1LSB STEP, RISING EDGE

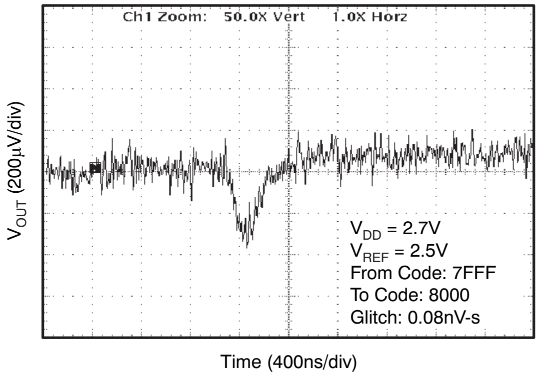


Figure 39.

GLITCH ENERGY: 2.7V, 1LSB STEP, FALLING EDGE

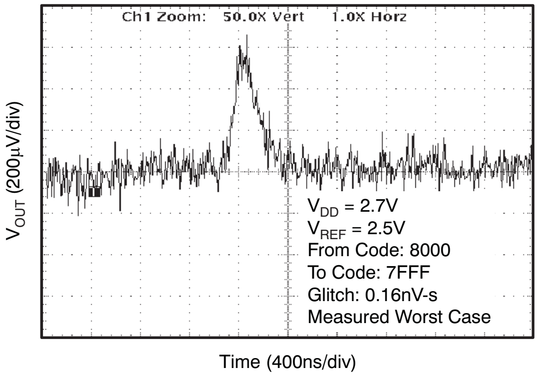


Figure 40.

GLITCH ENERGY: 2.7V, 16LSB STEP, RISING EDGE

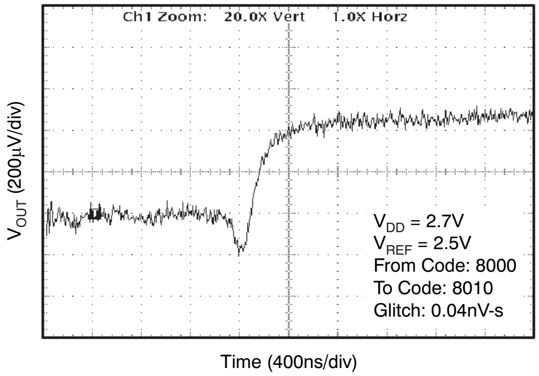


Figure 41.

GLITCH ENERGY: 2.7V, 16LSB STEP, FALLING EDGE

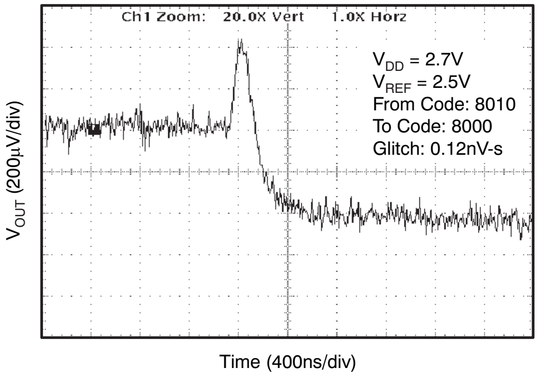


Figure 42.

GLITCH ENERGY: 2.7V, 256LSB STEP, RISING EDGE

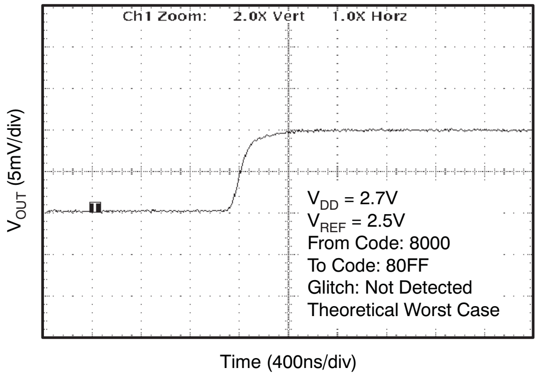


Figure 43.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V (continued)

At T_A = +25°C, unless otherwise noted.

GLITCH ENERGY: 2.7V, 256LSB STEP, FALLING EDGE

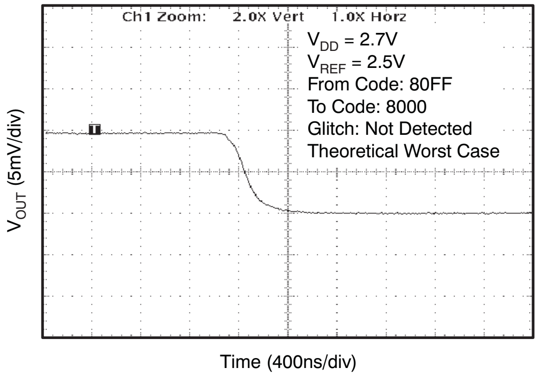


Figure 44.

THEORY OF OPERATION

DAC SECTION

The architecture of the DAC8850 consists of a string DAC followed by an output buffer amplifier. Figure 45 shows the block diagram of the DAC architecture.

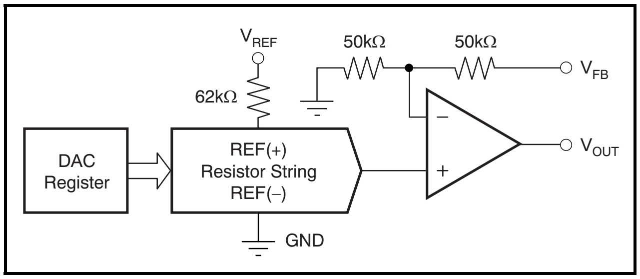


Figure 45. DAC8550 Architecture

The input coding to the DAC8550 is 2's complement, so the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{REF}}{2} + \frac{V_{REF} \times D}{65536} \qquad (1)$$

where D = decimal equivalent of the 2's complement code that is loaded to the DAC register; D ranges from –32768 to +32767 where D = 0 is centered at $V_{REF}/2$.

RESISTOR STRING

The resistor string section is shown in Figure 46. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Monotonicity is ensured because of the string resistor architecture.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail output voltages with a range of 0V to V_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 1.8V/µs with a full-scale setting time of 8µs with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin. This architecture allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

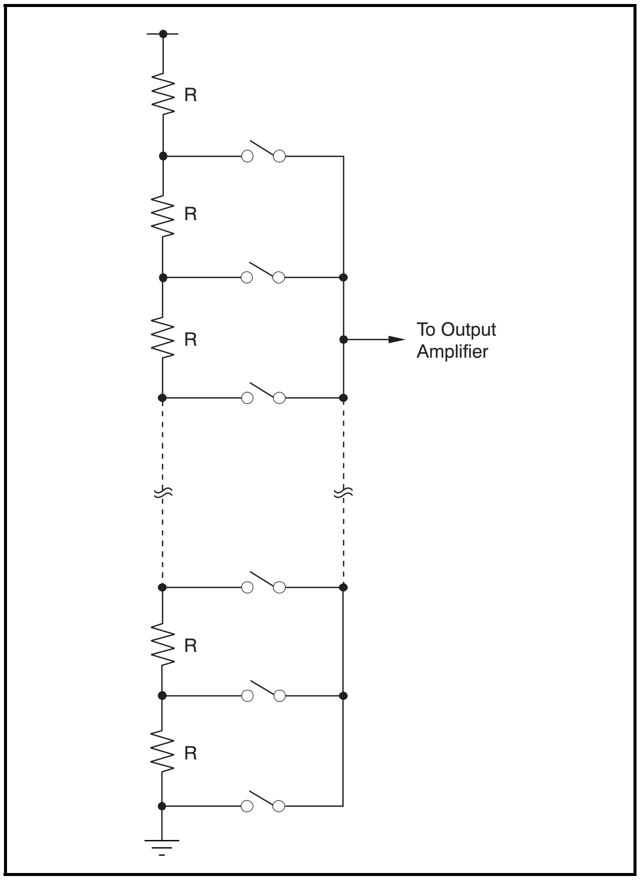


Figure 46. Resistor String

SERIAL INTERFACE

The DAC8550 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI, QSPI, and Microwire interface standards, as well as most DSP interfaces. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8550 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is excuted (that is, a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Since the $\overline{SYNC}$ buffer draws more current when the $\overline{SYNC}$ signal is HIGH than it does when it is LOW, $\overline{\text{SYNC}}$ should be idled LOW between write sequences for lowest power operation of the part. As mentioned above, it must be brought HIGH again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide, as shown in Figure 47. The first six bits are *don't care* bits. The next two bits (PD1 and PD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). For a more complete description of the various modes see the *Power-Down Modes* section. The next 16 bits are the data bits. These bits are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 48.

POWER-ON RESET

The DAC8550 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the output voltages are set to midscale; they remain that way until a valid write sequence is made to the DAC. The power-on reset is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

DB23 DB0

X	X	X	X	X	X	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 47. DAC8550 Data Input Register Format

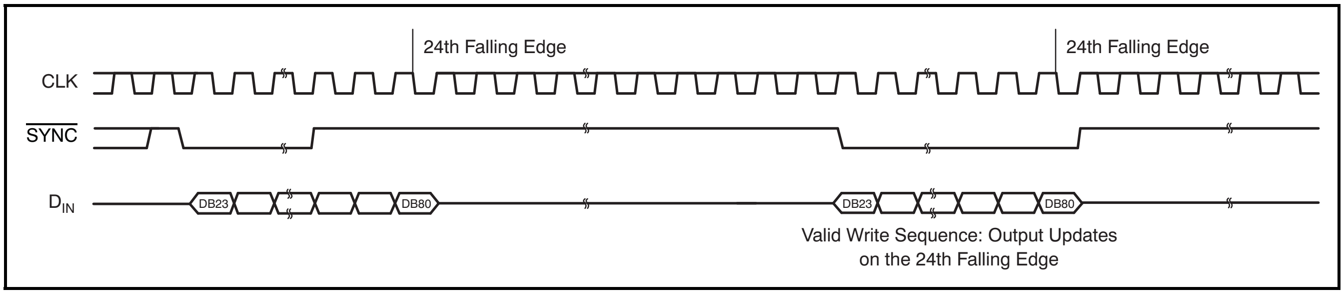


Figure 48. $\overline{\text{SYNC}}$ Interrupt Facility

POWER-DOWN MODES

The DAC8550 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 1 shows how the state of the bits corresponds to the mode of operation of the device.

Table 1. Operating Modes

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal operation
—	—	Power-down modes
0	1	Output typically 1kΩ to GND
1	0	Output typically 100kΩ to GND
1	1	High-Z

When both bits are set to '0', the device works normally with a typical current consumption of 200µA at 5V. However, for the three power-down modes, the supply current falls to 200nA at 5V (50nA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. The advantage with this configuration is that the output impedance of the device is known while in power-down mode. There are three different options. The output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 49.

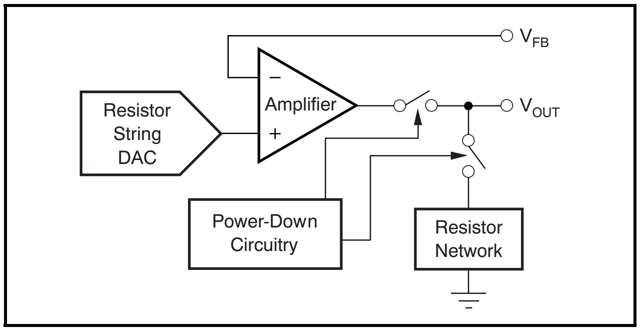


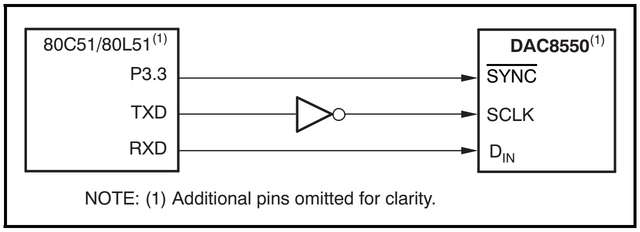
Figure 49. Output Stage During Power-Down

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5µs for V_{DD} = 5V, and 5µs for V_{DD} = 3V. See the Typical Characteristics for more information.

MICROPROCESSOR INTERFACING

DAC8550 to 8051 Interface

See Figure 50 for a serial interface between the DAC8550 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8550, while RXD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data are to be transmitted to the DAC8550, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC8550 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.

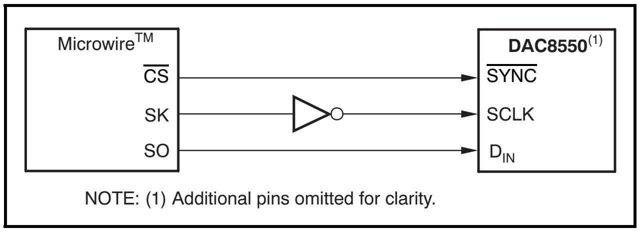


NOTE: (1) Additional pins omitted for clarity.

Figure 50. DAC8550 to 80C51/80L51 Interface

DAC8550 to Microwire Interface

Figure 51 shows an interface between the DAC8550 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and clocked into the DAC8550 on the rising edge of the SK signal.

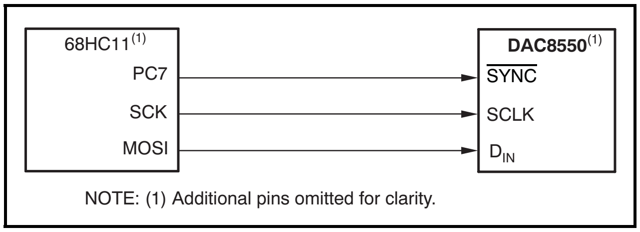


NOTE: (1) Additional pins omitted for clarity.

Figure 51. DAC8550 to Microwire Interface

DAC8550 to 68HC11 Interface

Figure 52 shows a serial interface between the DAC8550 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8550, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7), similar to the 8051 diagram.



NOTE: (1) Additional pins omitted for clarity.

Figure 52. DAC8550 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is held LOW (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC8550, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation are performed to the DAC. PC7 is taken HIGH at the end of this procedure.

APPLICATION INFORMATION

USING THE REF02 AS A POWER SUPPLY FOR THE DAC8550

Due to the extremely low supply current required by the DAC8550, an alternative option is to use a REF02 +5V precision voltage reference to supply the required voltage to the device, as shown in Figure 53.

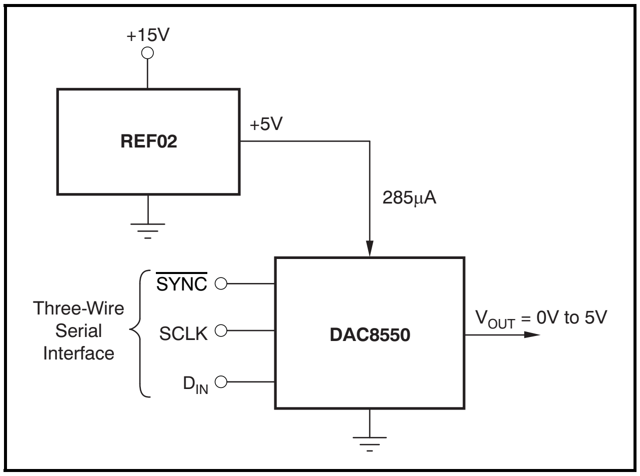


Figure 53. REF02 as a Power Supply to the DAC8550

This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 outputs a steady supply voltage for the DAC8550. If the REF02 is used, the current it needs to supply to the DAC8550 is 250µA. This configuration is with no load on the output of the DAC. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5kΩ load on the DAC output) is:

$$200\ \mu A + \frac{5\ V}{5\ k\Omega} = 1.2\ mA \quad (2)$$

The load regulation of the REF02 is typically 0.005%/mA, resulting in an error of 299µV for the 1.2mA current drawn from it. This value corresponds to an 8.9LSB error.

BIPOLAR OPERATION USING THE DAC8550

The DAC8550 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 54. The circuit shown gives an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[\left(\frac{V_{REF}}{2} + V_{REF} \times \frac{D}{65536}\right) \times \left(\frac{R_1 + R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_2}{R_1}\right)\right]$$

where D represents the input code in 2's complement (–32768 to +32767).

With V_{REF} = 5V, $R_1 = R_2$ = 10kΩ.

$$V_O = 10 \times \frac{D}{65536} \quad (4)$$

Using this example, an output voltage range of ±5V with 8000h corresponding to a –5V output and 8FFFh corresponding to a 5V output can be achieved. Similarly, using V_{REF} = 2.5V, a ±2.5V output voltage range can be achieved.

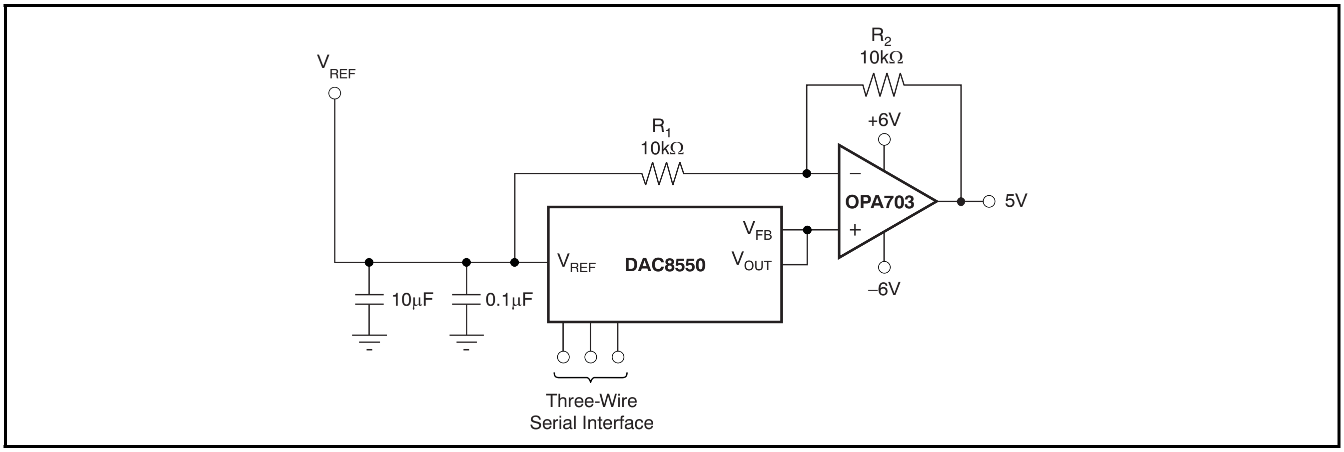


Figure 54. Bipolar Output Range

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8550 offers single-supply operation and is used often in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8550, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to V_{DD} should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a 5V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1µF to 10µF capacitor and 0.1µF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors, all designed to essentially low-pass filter the 5V supply, removing the high-frequency noise.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC8550IBDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8550IBDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8550IBDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8550IBDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8550IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8550IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8550IDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8550IDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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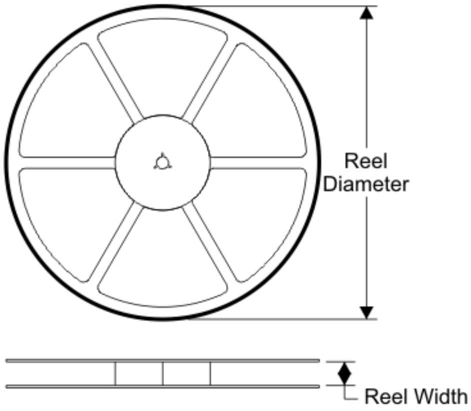
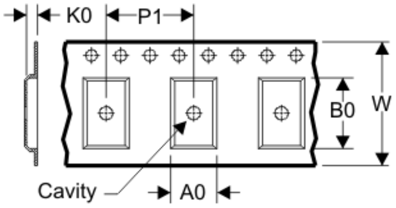
TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

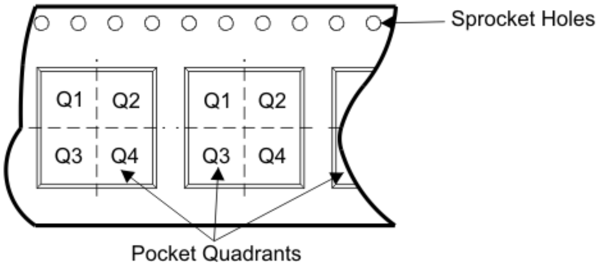


TAPE DIMENSIONS



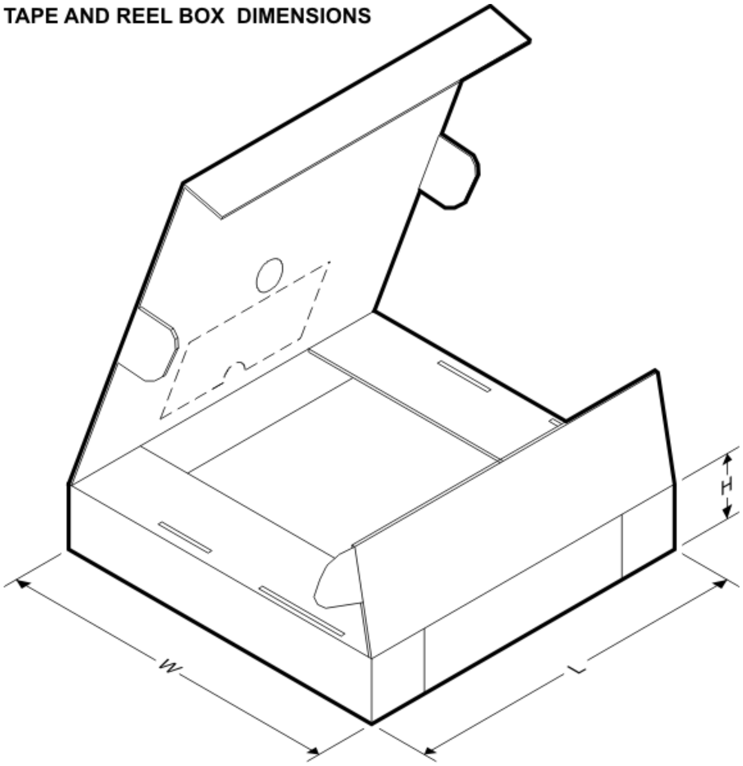
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



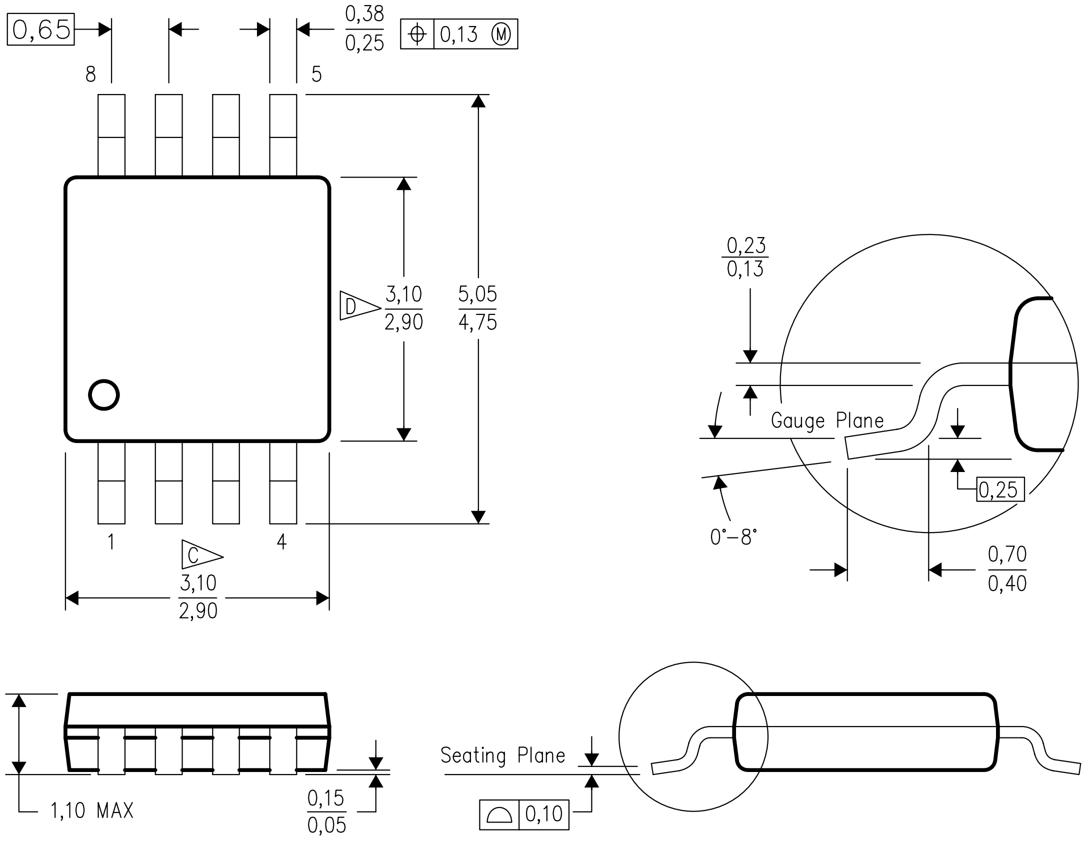
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8550IBDGKR	DGK	8	SITE 60	330	12	5.3	3.4	1.4	8	12	Q1
DAC8550IBDGKT	DGK	8	SITE 60	330	12	5.3	3.4	1.4	8	12	Q1
DAC8550IDGKR	DGK	8	SITE 60	330	12	5.3	3.4	1.4	8	12	Q1
DAC8550IDGKT	DGK	8	SITE 60	330	12	5.3	3.4	1.4	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
DAC8550IBDGKR	DGK	8	SITE 60	346.0	346.0	29.0
DAC8550IBDGKT	DGK	8	SITE 60	346.0	346.0	29.0
DAC8550IDGKR	DGK	8	SITE 60	346.0	346.0	29.0
DAC8550IDGKT	DGK	8	SITE 60	346.0	346.0	29.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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