

# CY74FCT825T

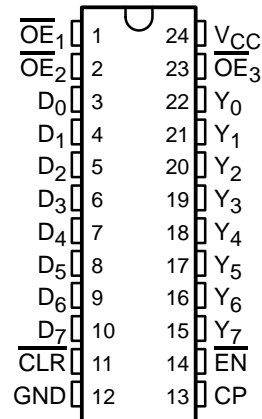
## 8-BIT BUS-INTERFACE REGISTER

### WITH 3-STATE OUTPUTS

SCCS070A – OCTOBER 2001 – REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29825
- Reduced  $V_{OH}$  (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- 64-mA Output Sink Current  
32-mA Output Source Current
- High-Speed Parallel Register With Positive-Edge-Triggered D-Type Flip-Flops
- Buffered Common Clock-Enable ( $\overline{EN}$ ) and Asynchronous-Clear ( $\overline{CLR}$ ) Inputs
- 3-State Outputs

Q PACKAGE  
(TOP VIEW)



#### description

This bus-interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The CY74FCT825T is an 8-bit buffered register with all the CY74FCT823T controls, plus multiple enables ( $\overline{OE}_1$ ,  $\overline{OE}_2$ ,  $\overline{OE}_3$ ) to allow multiuser control of the interface, e.g.,  $\overline{CS}$ , DMA, and RD/WR. This device is ideal for use as an output port requiring high  $I_{OL}/I_{OH}$ .

This device is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

$T_A$	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	6	CY74FCT825CTQCT	FCT825C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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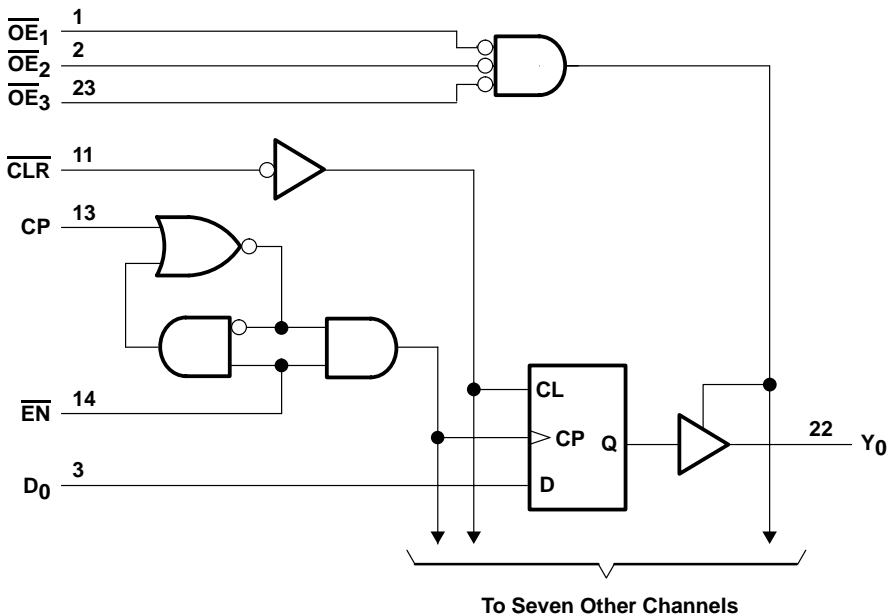
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PIN DESCRIPTION		
NAME	I/O	DESCRIPTION
D	I	D flip-flop data inputs
$\overline{\text{CLR}}$	I	When $\overline{\text{CLR}}$ is low and $\overline{\text{OE}}$ is low, Q outputs are low. When $\overline{\text{CLR}}$ is high, data can be entered into the register.
CP	O	Clock pulse for the register. Enters data into the register on the low-to-high clock transition.
Y	O	Register 3-state outputs
$\overline{\text{EN}}$	I	Clock enable. When $\overline{\text{EN}}$ is low, data on the D input is transferred to the Q output on the low-to-high clock transition. When $\overline{\text{EN}}$ is high, the Q outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output control. When $\overline{\text{OE}}$ is high, the Y outputs are in the high-impedance state. When $\overline{\text{OE}}$ is low, true register data is present at the Y outputs.

FUNCTION TABLE							
INPUTS					INTERNAL OUTPUTS		FUNCTION
OE	CLR	EN	D	CP	Q	Y	
H	H	L	L	↑	L	Z	Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = High logic level, L = Low logic level, X = Don't care, NC = No change, ↑ = Low-to-high transition, Z = High-impedance state

logic diagram (positive logic)



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**absolute maximum rating over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note1) .....	61°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–32	mA
$I_{OL}$ Low-level output current			64	mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>IN</sub> = −18 mA		−0.7	−1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = −32 mA	2		V	
		I <sub>OH</sub> = −15 mA	2.4	3.3		
V <sub>OL</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 64 mA		0.3	0.55	V
V <sub>hys</sub>	All inputs			0.2		V
I <sub>I</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = V <sub>CC</sub>			5	μA
I <sub>IH</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 2.7 V			±1	μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 0.5 V			±1	μA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 2.7 V			10	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0.5 V			−10	μA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0 V	−60	−120	−225	mA
I <sub>off</sub>	V <sub>CC</sub> = 0 V,	V <sub>OUT</sub> = 4.5 V			±1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V		0.1	0.2	mA
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V <sup>§</sup> , f <sub>1</sub> = 0, Outputs open			0.5	2	mA
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.25 V, One bit switching at 50% duty cycle, Outputs open, OE = EN = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V			0.06	0.12	mA/MHz
I <sub>C</sub> <sup>#</sup>	V <sub>CC</sub> = 5.25 V, Outputs open, OE = EN = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V	0.7	1.4	mA
			V <sub>IN</sub> = 3.4 V or GND	1.2	3.4	
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V	1.6	3.2	
			V <sub>IN</sub> = 3.4 V or GND	3.9	12.2	
C <sub>i</sub>				5	10	pF
C <sub>o</sub>				9	12	pF

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.



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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER			TEST LOAD	CY74FCT825AT		CY74FCT825BT		CY74FCT825CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CP	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	7		6		6		ns
		$\overline{\text{CLR}}$ low		6		6		6		
$t_{su}$	Setup time, before CP $\uparrow$	Data	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	4		3		3		ns
		$\overline{\text{EN}}$		4		3		3		
$t_h$	Hold time, after CP $\uparrow$	Data	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	2		1.5		1.5		ns
		$\overline{\text{EN}}$		2		0		0		
$t_{rec}$	Recovery time	$\overline{\text{CLR}}$ before CP $\uparrow$	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	6		6		6		ns

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT825AT		CY74FCT825BT		CY74FCT825CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	10		7.5		6		ns
$t_{PHL}$				10		7.5		6		
$t_{PLH}$	CP	Y	$C_L = 300 \text{ pF}$ , $R_L = 500 \Omega$	20		15		12.5		ns
$t_{PHL}$				20		15		12.5		
$t_{PLH}$	$\overline{\text{CLR}}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	14		9		8		ns
$t_{PZH}$	$\overline{\text{OE}}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	12		8		7		ns
$t_{PZL}$				12		8		7		
$t_{PZH}$	$\overline{\text{OE}}$	Y	$C_L = 300 \text{ pF}$ , $R_L = 500 \Omega$	23		15		12.5		ns
$t_{PZL}$				23		15		12.5		
$t_{PHZ}$	$\overline{\text{OE}}$	Y	$C_L = 5 \text{ pF}$ , $R_L = 500 \Omega$	7		6.5		6		ns
$t_{PLZ}$				7		6.5		6		
$t_{PHZ}$	$\overline{\text{OE}}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	8		7.5		6.5		ns
$t_{PLZ}$				8		7.5		6.5		

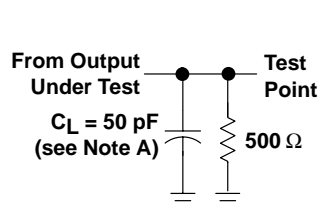
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## 8-BIT BUS-INTERFACE REGISTER

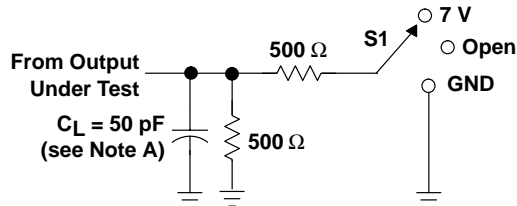
### WITH 3-STATE OUTPUTS

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#### PARAMETER MEASUREMENT INFORMATION

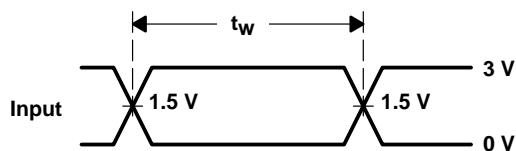


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

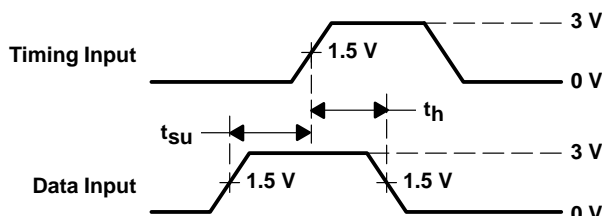


LOAD CIRCUIT FOR  
3-STATE OUTPUTS

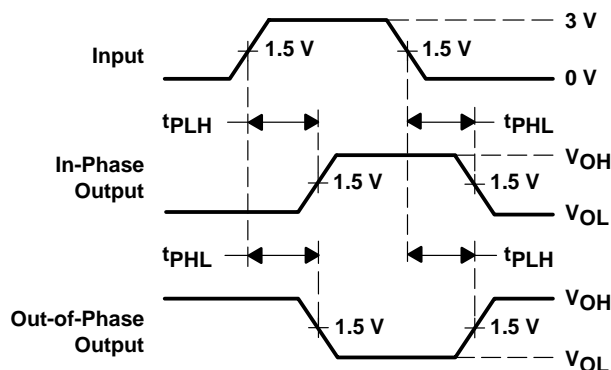
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



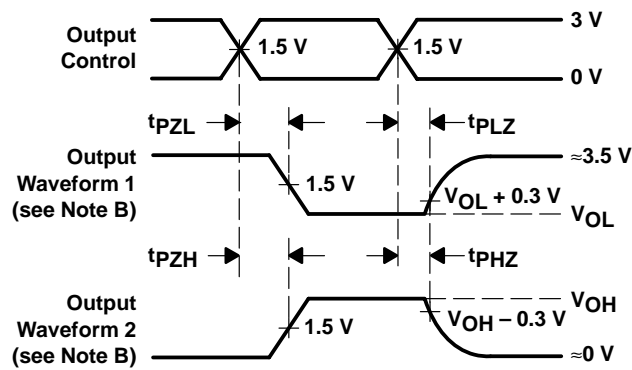
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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