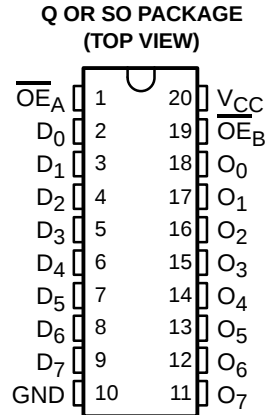


CY74FCT2541T

8-BIT BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

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- Function and Pinout Compatible With FCT and F Logic
- 25-Ω Output Series Resistors to Reduce Transmission-Line Reflection Noise
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- 12-mA Output Sink Current
15-mA Output Source Current
- 3-State Outputs



description

The CY74FCT2541T is an octal buffer and line driver designed to be employed as a memory-address driver, clock driver, and bus-oriented transmitter/receiver. On-chip termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2541T can replace the CY74FCT541T to reduce noise in an existing design. The speed of the CY74FCT2541T is comparable to bipolar logic counterparts, while reducing power dissipation. Input and output voltage levels allow direct interface with TTL and CMOS devices without external components.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	4.1	CY74FCT2541CTQCT	FCT2541C
		Tube	4.1	CY74FCT2541CTSOC	FCT2541C
	SOIC – SO	Tape and reel	4.1	CY74FCT2541CTSOCT	
		Tube	4.8	CY74FCT2541ATQCT	FCT2541A
	SOIC – SO	Tape and reel	4.8	CY74FCT2541ATSOCT	FCT2541A
		Tube	4.8	CY74FCT2541ATSOC	
	QSOP – Q	Tape and reel	8	CY74FCT2541TQCT	FCT2541
		Tube	8	CY74FCT2541TSOC	FCT2541
	SOIC – SO	Tape and reel	8	CY74FCT2541TSOCT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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CY74FCT2541T

8-BIT BUFFER/LINE DRIVER

WITH 3-STATE OUTPUTS

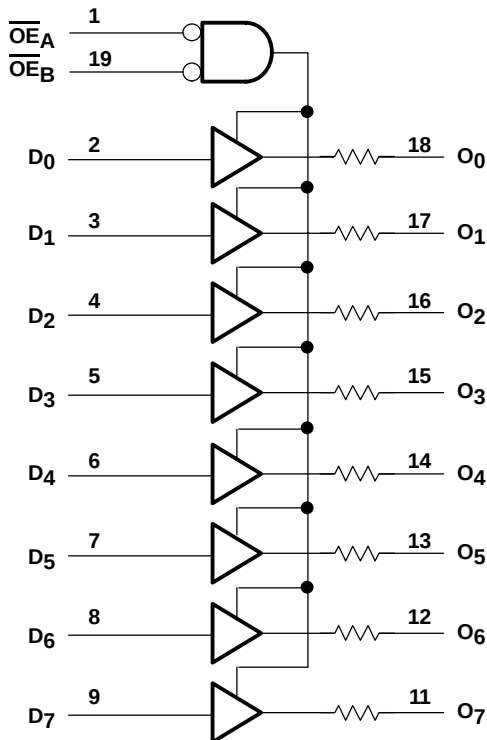
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FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state

logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	−0.5 V to 7 V
DC input voltage range	−0.5 V to 7 V
DC output voltage range	−0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T_A	−65°C to 135°C
Storage temperature range, T_{Stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC 51-7.

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recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current			–15	mA
I _{OL}	Low-level output current			12	mA
T _A	Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK}	V _{CC} = 4.75 V,	I _{IN} = –18 mA		–0.7	–1.2	V
V _{OH}	V _{CC} = 4.75 V,	I _{OH} = –15 mA	2.4	3.3		V
V _{OL}	V _{CC} = 4.75 V,	I _{OL} = 12 mA		0.3	0.55	V
R _{out}	V _{CC} = 4.75 V,	I _{OL} = 12 mA	20	25	40	Ω
V _{hys}	All inputs			0.2		V
I _I	V _{CC} = 5.25 V,	V _{IN} = V _{CC}			5	μA
I _{IH}	V _{CC} = 5.25 V,	V _{IN} = 2.7 V			±1	μA
I _{IL}	V _{CC} = 5.25 V,	V _{IN} = 0.5 V			±1	μA
I _{OZH}	V _{CC} = 5.25 V,	V _{OUT} = 2.7 V			15	μA
I _{OZL}	V _{CC} = 5.25 V,	V _{OUT} = 0.5 V			–15	μA
I _{OS} [‡]	V _{CC} = 5.25 V,	V _{OUT} = 0 V	–60	–120	–225	mA
I _{off}	V _{CC} = 0 V,	V _{OUT} = 4.5 V			±1	μA
I _{CC}	V _{CC} = 5.25 V,	V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} – 0.2 V		0.1	0.2	mA
ΔI _{CC}	V _{CC} = 5.25 V, V _{IN} = 3.4 V [§] , f ₁ = 0, Outputs open			0.5	2	mA
I _{CCD} [¶]	V _{CC} = 5.25 V at 50% duty cycle, Outputs open, One bit switching, OE _A = OE _B = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.06	0.12	mA/MHz
I _C [#]	V _{CC} = 5.25 V, Outputs open, OE _A = OE _B = GND	One bit switching at f ₁ = 10 MHz, at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4	mA
			V _{IN} = 3.4 V or GND	1	2.4	
		Eight bits switching at f ₁ = 2.5 MHz, at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1.3	2.6	
			V _{IN} = 3.4 V or GND	3.3	10.6	
C _i				5	10	pF
C _o				9	12	pF

[†] Typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

[§] Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

[¶] This parameter is derived for use in total power-supply calculations.

[#] I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



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switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2541T		CY74FCT2541AT		CY74FCT2541CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	O	1.5	8	1.5	4.8	1.5	4.1	ns
t _{PHL}			1.5	8	1.5	4.8	1.5	4.1	
t _{PZH}	$\overline{\text{OE}}$	O	1.5	10	1.5	6.2	1.5	5.8	ns
t _{PZL}			1.5	10	1.5	6.2	1.5	5.8	
t _{PHZ}	$\overline{\text{OE}}$	O	1.5	9.5	1.5	5.6	1.5	5.2	ns
t _{PLZ}			1.5	9.5	1.5	5.6	1.5	5.2	



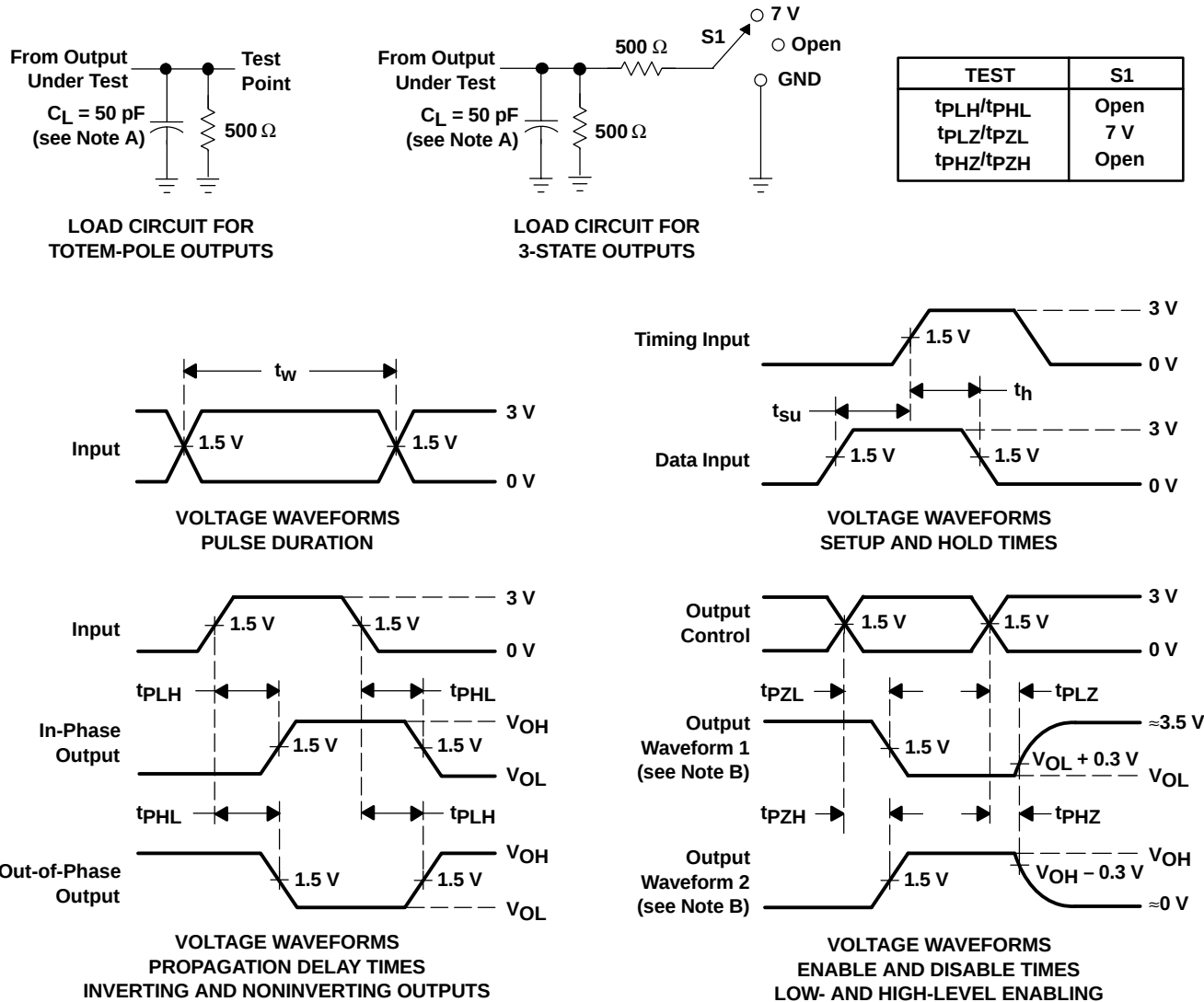
CY74FCT2541T

8-BIT BUFFER/LINE DRIVER

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CY74FCT2541ATQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541ATQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541ATQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541CTQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541CTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541TQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541TQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541TQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2541TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541TSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541TSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2541TSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

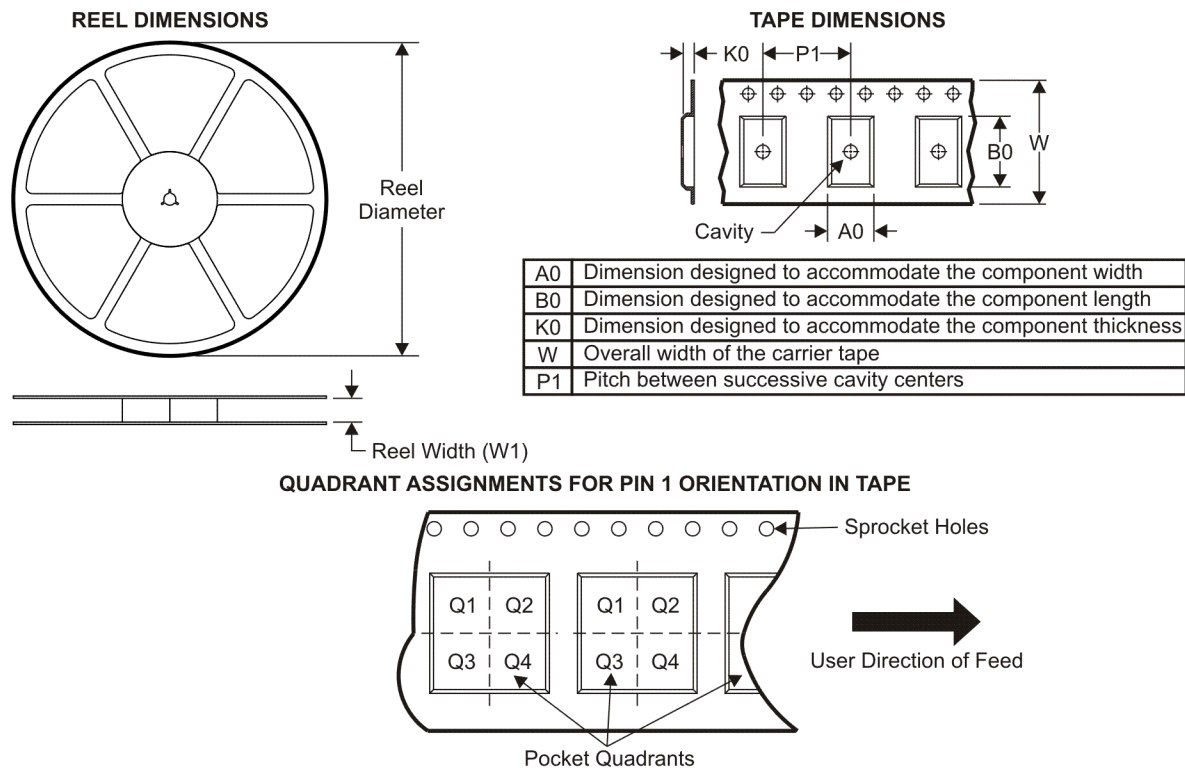
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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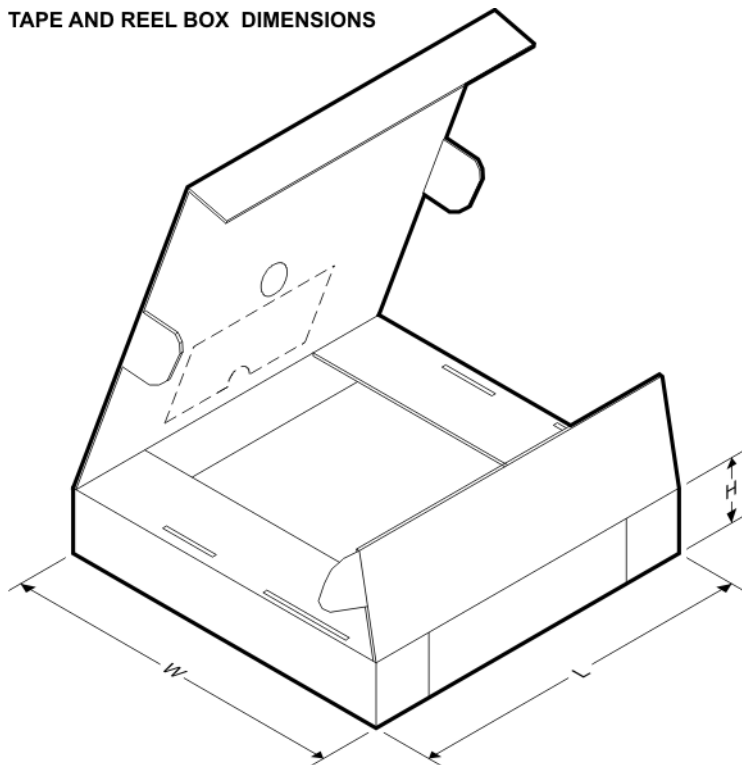
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT2541ATQCT	SSOP/ QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2541CTQCT	SSOP/ QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2541TQCT	SSOP/ QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2541TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

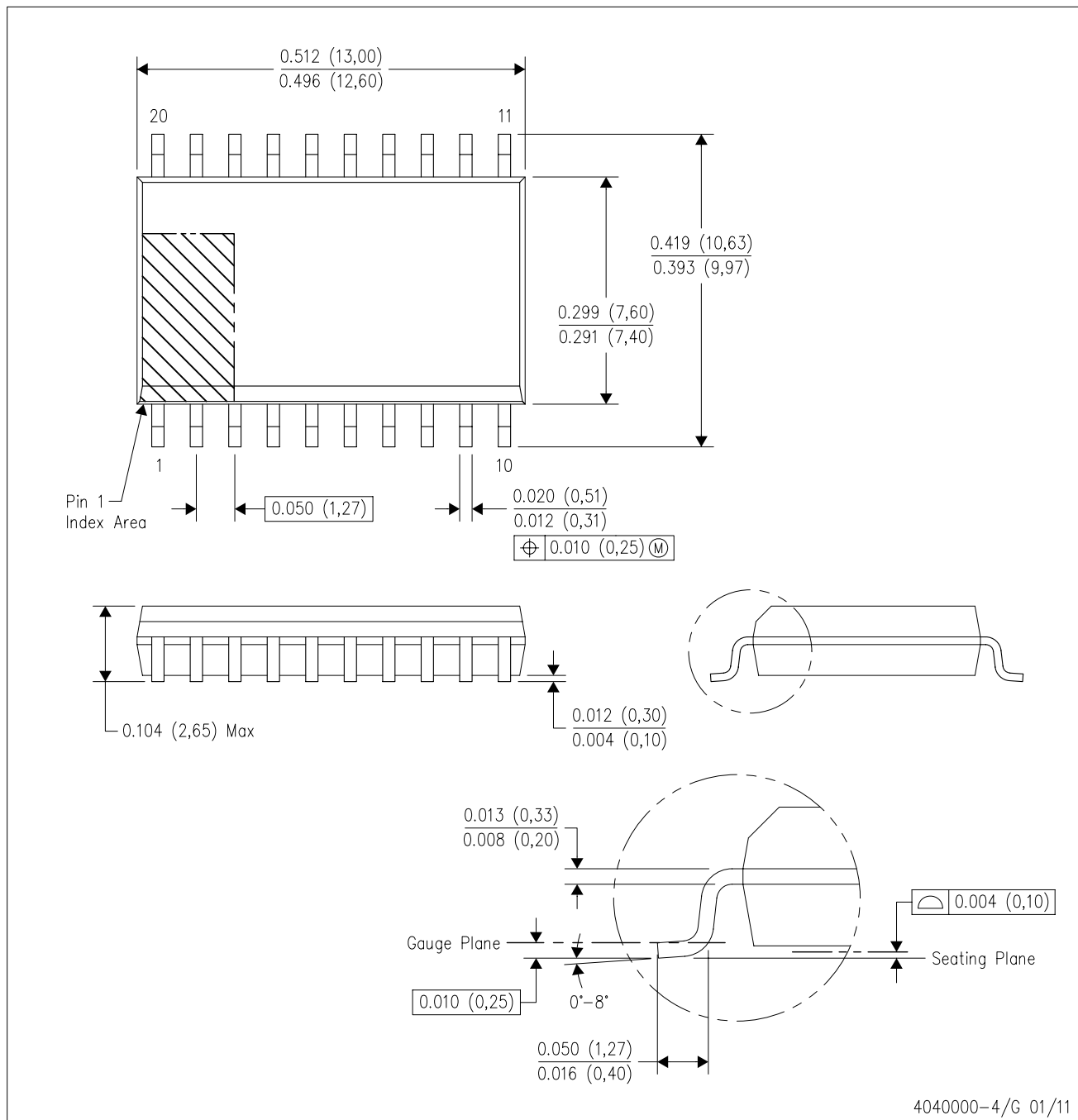


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT2541ATQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2541CTQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2541TQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2541TSOCT	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R-PDSO-G20)

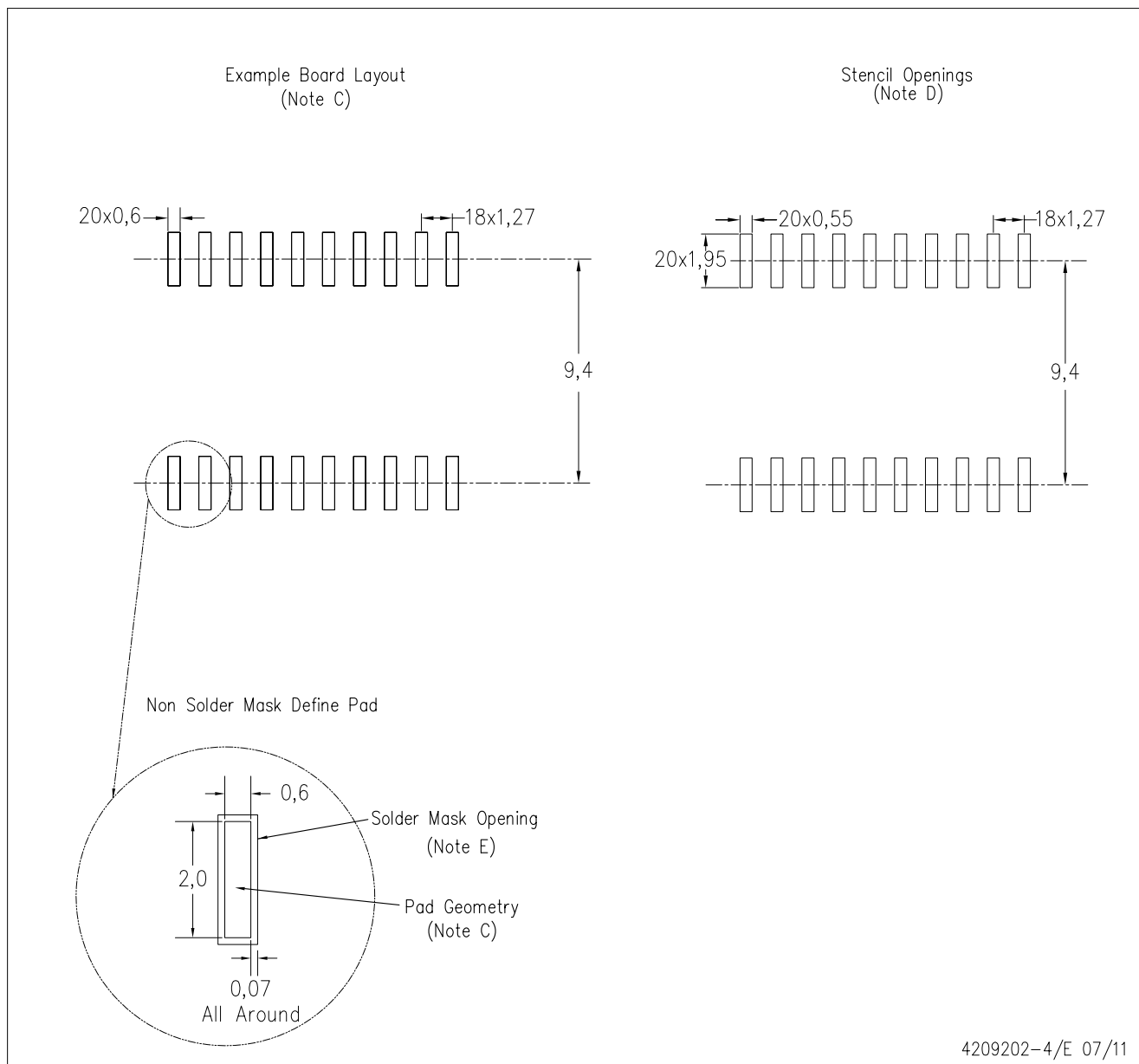
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

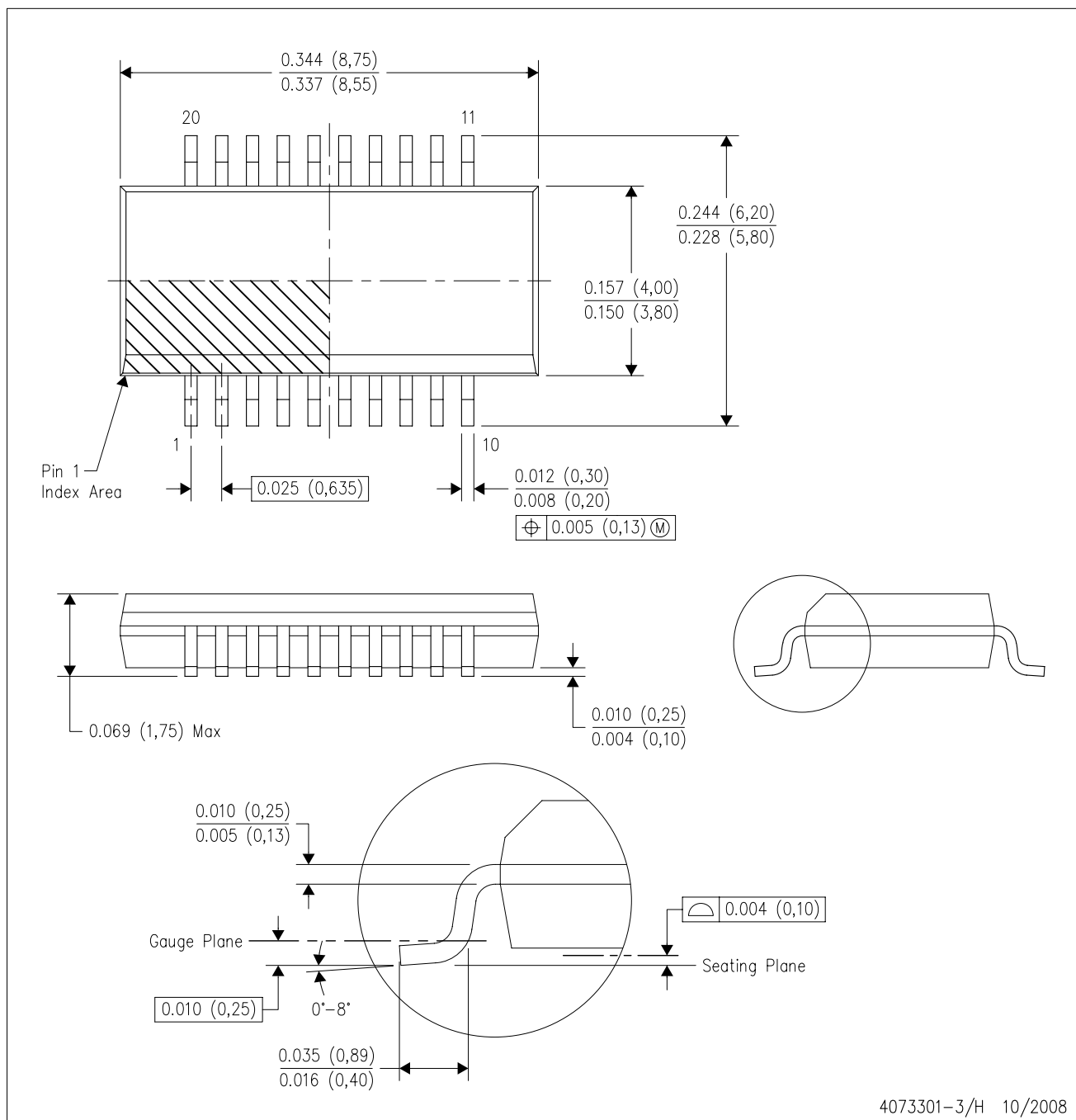
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G20)

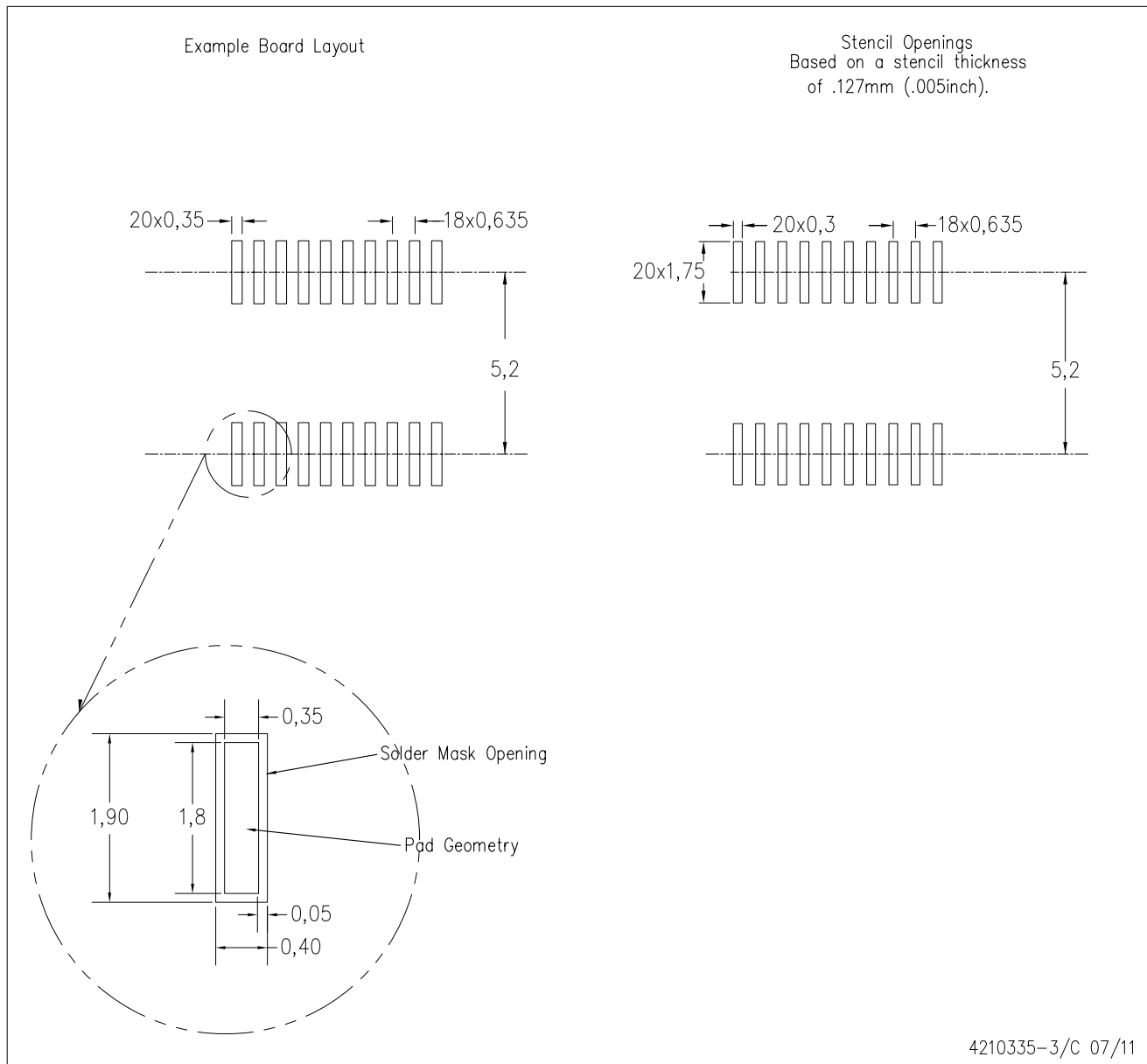
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AD.

DBQ (R-PDSO-G20)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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