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FEATURES

- 1.8-V Phase Lock Loop Clock Driver for Double Data Rate (DDR II) Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 10 MHz to 400 MHz
- Low Current Consumption: <135 mA
- Low Jitter (Cycle-Cycle): ±30 ps
- Low Output Skew: 35 psLow Period Jitter: ±20 ps
- Low Dynamic Phase Offset: ±15 ps

- Low Static Phase Offset: ±50 ps
- Distributes One Differential Clock Input to Ten Differential Outputs
- 52-Ball µBGA (MicroStar[™] Junior BGA, 0,65-mm pitch) and 40-Pin MLF
- External Feedback Pins (FBIN, FBIN) are Used to Synchronize the Outputs to the Input Clocks
- Meets or Exceeds JESD82-8 PLL Standard for PC2-3200/4300
- Fail-Safe Inputs

DESCRIPTION

The CDCU877 is a high-performance, low-jitter, low-skew, zero-delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pairs of clock outputs (Yn, $\overline{\text{Yn}}$) and to one differential pair of feedback clock outputs (FBOUT, FBOUT). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the LVCMOS control pins (OE, OS), and the analog power input (AV_{DD}). When OE is low, the clock outputs, except FBOUT/ $\overline{\text{FBOUT}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS (output select) is a program pin that must be tied to GND or V_{DD}. When OS is high, OE functions as previously described. When OS and OE are both low, OE has no affect on Y7/ $\overline{\text{Y7}}$, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock inputs (CK, $\overline{\text{CK}}$) are logic low, the device enters in a low power mode. An input logic detection circuit on the differential inputs, independent from input buffers, detects the logic low level and performs in a low power state where all outputs, the feedback, and the PLL are off. When the clock inputs transition from being logic low to being differential signals, the PLL turns back on, the inputs and the outputs are enabled, and the PLL obtains phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the clock input pair (CK, $\overline{\text{CK}}$) within the specified stabilization time.

The CDCU877 is able to track spread spectrum clocking (SSC) for reduced EMI. This device operates from —40°C to 85°C.

ORDERING INFORMATION

T _A	52-BALL BGA ⁽¹⁾	40-Pin MLF
	CDCU877ZQL	CDCU877RHA
-40°C to 85°C	CDCU877AZQL	CDCU877ARHA
-40°C 10 85°C	CDCU877GQL	CDCU877RTB
	CDCU877AGQL	CDCU877ARTB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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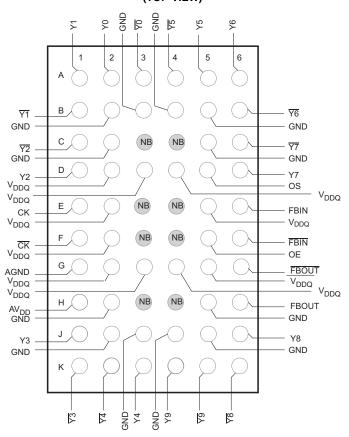
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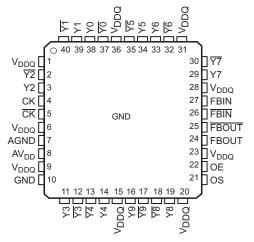
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

MicroStar Junior (ZQL) Package (TOP VIEW)



- A. NC = No Connection
- B. NB = No Ball

RHA/RTB Package (MLF PAckage (TOP VIEW)



40-pin HP-VFQFP-N (6,0 x 6,0 mm Body Size, 0,5 mm Pitch, M0#220, Variation VJJD-2, E2 = D2 = 2,9 mm \pm 0,15 mm) Package Pinouts



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TERMINAL FUNCTIONS

TI	ERMINAL		1/0	DECORIDATION
NAME	GQL/ZQL	RHA/RTB	I/O	DESCRIPTION
AGND	G1	7		Analog ground
AV_{DD}	H1	8		Analog power
CK	E1	4	I	Clock input with a (10 kΩ to 100 kΩ) pulldown resistor
СК	F1	5	Ι	Complementary clock input with a (10 k Ω to 100 k Ω) pulldown resistor
FBIN	E6	27	I	Feedback clock input
FBIN	F6	26	1	Complementary feedback clock input
FBOUT	H6	24	0	Feedback clock output
FBOUT	G6	25	0	Complementary feedback clock output
OE	F5	22	I	Output enable (asynchronous)
os	D5	21	1	Output select (tied to GND or V _{DD})
GND	B2, B3, B4, B5, C2, C5, H2, H5, J2, J3, J4, J5	10		Ground
V_{DDQ}	D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	1, 6, 9, 15, 20, 23, 28, 31, 36		Logic and output power
Y[0:9]	A2, A1, D1, J1, K3, A5, A6, D6, J6, K4	3, 11, 14, 16, 19, 29, 33, 34, 38, 39	0	Clock outputs
Y[0:9]	A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	2, 12, 13, 18, 17, 30, 32, 35, 37, 40	0	Complementary clock outputs

FUNCTION TABLE

		INPUTS			OUTPUTS						
AVDD	OE	os	CK	CK	Υ	Y	FBOUT	FBOUT	PLL		
GND	Н	Х	L	Н	L	Н	L	Н	Bypassed/Off		
GND	Н	Х	Н	L	Н	L	Н	L	Bypassed/Off		
GND	L	Н	L	Н	L _Z	L_Z	L	Н	Bypassed/Off		
GND	L	L	Н	L	L _Z Y7 Active	L _Z Y7 Active	Н	L	Bypassed/Off		
1.8 V Nominal	L	Н	L	Н	L _Z	L _Z	L	Н	On		
1.8 V Nominal	L	L	Н	L	L _Z Y7 Active	L _Z Y7 Active	Н	L	On		
1.8 V Nominal	Н	Х	L	Н	L	Н	L	Н	On		
1.8 V Nominal	Н	Х	Н	L	Н	L	Н	L	On		
1.8 V Nominal	Х	Х	L	L	L _Z	L _Z	L _Z	L _Z	Off		
X	Χ	Х	Н	Н	Reserved						



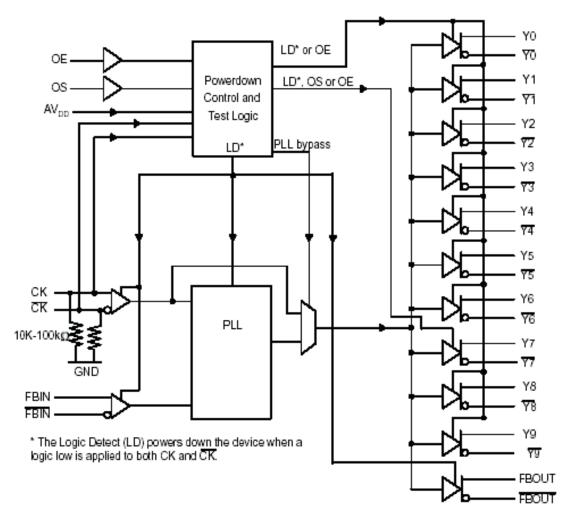


Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)



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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	V _{DDQ} or AV _{DD}	-0.5	2.5	V
VI	Input voltage range ⁽²⁾⁽³⁾		-0.5	$V_{DDQ} + 0.5$	V
Vo	Output voltage range (2)(3)		-0.5	$V_{DDQ} + 0.5$	V
I _{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DDQ}$		±50	mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DDQ}$		±50	mA
Io	Continuous output current	$V_O = 0$ to V_{DDQ}		±50	mA
	Continuous current through each V _{DDQ} or		±100	mA	
T _{stg}	Storage temperature range	Storage temperature range			

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V	Output supply voltage, V _{DDQ}		1.7	1.8	1.9	V
V _{CC}	Supply Voltage, AV _{DD} ⁽¹⁾			V_{DDQ}		V
V_{IL}	Low-level input voltage ⁽²⁾	OE, OS			0.35 x V _{DDQ}	V
V_{IH}	High-level input voltage (2)	CK, CK	0.65 x V _{DDQ}			V
I _{OH}	High-level output current (see Figure 2	2)			-9	mA
I _{OL}	Low-level output current (see Figure 2	2)			9	mA
V_{IX}	Input differential-pair cross voltage		(V _{DDQ} /2) - 0.15		$(V_{DDQ}/2) + 0.15$	V
V_{I}	Input voltage level		-0.3		V _{DDQ} + 0.3	V
V	Input differential voltage (2)	DC	0.3		V _{DDQ} + 0.4	V
V _{ID}	(see Figure 9)	AC	0.6		V _{DDQ} + 0.4	V
T _A	Operating free-air temperature		-40		85	°C

⁽¹⁾ The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are specified. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} , see Figure 9 for definition. The CK and

The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽³⁾ This value is limited to 2.5 V maximum.

 $[\]overline{\text{CK}}$, V_{IH} and V_{IL} limits define the dc low and high levels for the logic detect state.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	AV_{DD} , V_{DDQ}	MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IK}	Input		I _I = 18 mA	1.7			-1.2	V	
V	Lligh lovel output voltage		I _{OH} = -100 μA	1.7 to 1.9	V _{DDQ} - 0.2			V	
V _{OH}	High-level output voltage	*	$I_{OH} = -9 \text{ mA}$	1.7	1.1			V	
V	Low-level output voltage		I _{OL} = 100 μA				0.1	V	
V_{OL}	VOL Low-level output voltage		I _{OL} = 9 mA	1.7			0.6	V	
$I_{O(DL)}$	Low-level output current	, dissabled	$V_{O(DL)} = 100 \text{ mV}, OE = L$	1.7	100			μΑ	
V_{OD}	Differential output voltag	e ⁽¹⁾		1.7	0.5			V	
I _I	Input current	CK, CK		1.9			±250		
		OE, OS, FBIN, FBIN		1.9			±10	μΑ	
I _{DD(LD)}	Supply current, static (I _D	_{DQ} + I _{ADD})	CK and $\overline{\text{CK}}$ = L	1.9			500	μΑ	
I _{DD}	Supply current, dynamic (see Note ⁽²⁾ for CPD ca	(I _{DDQ} + I _{ADD})	CK and $\overline{\text{CK}}$ = 270 MHz. All outputs are open (not connected to a PCB)	1.9			135	mA	
	(see Note Viol CPD ca	iculation)	All outputs are loaded with 2 pF and 120-Ω termination resistor	1.9			235		
0	Innut conscitores	CK, CK	V V or CND	1.8	2		3		
C _I	Input capacitance FBIN, FBIN		$V_I = V_{DD}$ or GND	1.8	2		3		
0	Change in input assessed	CK, CK	V V or CND	1.8			0.25	pF	
$C_{I(\Delta)}$	Change in input current FBIN, FBIN		$V_I = V_{DD}$ or GND	1.8			0.25		

⁽¹⁾ V_{OD} is the magnitude of the difference between the true and complimentary outputs. See Figure 9 for a definition.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)(1)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ı	Clock frequency (operating) ⁽¹⁾⁽²⁾		10	400	MHz
t _{CK}	Clock frequency (application) ⁽¹⁾⁽³⁾	AV V - 18V +01V	160	340	MHz
t_{DC}	Duty cycle, input clock	AV_{DD} , $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$	40%	60%	
tL	Stabiliztion time (4)			12	μs

- (1) The PLL must be able to handle spread spectrum induced skew.
- (2) Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low speed system debug).
- (3) Application clock frequency indicates a range over which the PLL must meet all timing parameters.
- (4) Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and CK go to a logic low state, enter the power-down mode and later return to active operation. CK and CK may be left floating after they have been driven low for one complete clock cycle.

⁽²⁾ Total I_{DD} = I_{DDQ} + I_{ADD} = f_{CK} × C_{PD} × V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(f_{CK} × V_{DDQ}) where f_{CK} is the input frequency, V_{DDQ} is the power supply, and C_{PD} is the power dissipation capacitance.



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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see $^{(1)}$) AV_{DD}, V_{DD} = 1.8 V \pm 0.1 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
t _{en}	Enable time, OE to any Y/Y	See Figure 11			8	ns			
t _{dis}	Disable time, OE to any Y/Y	See Figure 11			8	ns			
t _{jit(cc+)}	Civale to suple period ittem(2)	400 MHz to 400 MHz and Figure 4	0		40				
t _{jit(cc-)}	Cycle-to-cycle period jitter ⁽²⁾	160 MHz to 190 MHz, see Figure 4	0		-40	ps			
t _{jit(cc+)}	Civale to suple period (there(2))	400 MHz to 240 MHz and Figure 4	0		30				
t _{jit(cc-)}	Cycle-to-cycle period jitter ⁽²⁾	160 MHz to 340 MHz, see Figure 4	0		-30	ps			
$t_{(\omega)}$	Static phase offset time ⁽³⁾	See Figure 5	-50		50	ps			
t _{(ω)dyn}	Dynamic phase offset time	See Figure 10	-15		15	ps			
t _{sk(o)}	Output clock skew	See Figure 6			35	ps			
	Period jitter (4)(2)	160 MHz to 190 MHz, see Figure 7	-30		30				
t _{jit(per)}	Period jitter (4)(-)	190 MHz to 340 MHz, see Figure 7	-20		20	ps			
	Half-period jitter ⁽⁴⁾⁽²⁾	160 MHz to 190 MHz, see Figure 8	-115		115				
		190 MHz to 250 MHz, see Figure 8	-70		70	nc			
t _{jit(hper)}		250 MHz to 300 MHz, see Figure 8	-40		40	ps			
		300 MHz to 340 MHz, see Figure 8	-60		60				
	Slew rate, OE	See Figure 3 and Figure 9	0.5						
SR	Input clock slew rate	See Figure 3 and Figure 9	1	2.5	4	V/ns			
	Output clock slew rate ⁽⁵⁾⁽⁶⁾ (no load)	See Figure 3 and Figure 9	1.5	2.5	3				
W	Output differential pair erose valters (7)	CDCU877, See Figure 2	(V _{DDQ} /2) - 0.1	('	(V _{DDQ} /2) + 0.1				
V _{OX}	Output differential-pair cross voltage (7)	CDCU877A ⁽⁸⁾ , See Figure 2 (0 - 85°C)	(V _{DDQ} /2) - 0.1	('	V _{DDQ} /2) + 0.1	V			
	SSC modulation frequency		30		33	kHz			
	SSC clock input frequency deviation		0%		-0.5%				
	PLL loop bandwidth		2			MHz			

⁽¹⁾ There are two different terminations that are used with the following tests. The load/board in Figure 2 is used to measure the input and output differential-pair cross voltage only. The load/board in Figure 3 is used to measure all other tests. For consistency, equal length cables must be used.

- This parameter is specifieded by design and characterization.
- (3) Phase static offset time does not include jitter.
- (4) Period jitter, half-period jitter specifications are separate specifications that must be met independently of each other.
- (5) The output slew rate is determined from the IBIS model with a 120-Ω load only.
 (6) To eliminate the impact of input slew rates on static phase offset, the input skew rates of reference clock input CK and CK and feedback clock inputs FBIN and FBIN are recommended to be nearly equal. The 2.5-V/ns skew rates are shown as a recommended target. Compliance with these typical values is not mandatory if it can adequately shown that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
- Output differential-pair cross voltage specified at the DRAM clock input or the test load.
- (8) V_{OX} of CDCU877A is on average 30 mV lower than that of CDCU877 for the same application.



PARAMETER MEASUREMENT INFORMATION

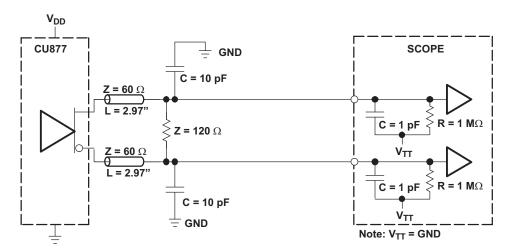


Figure 2. Output Load Test Circuit 1

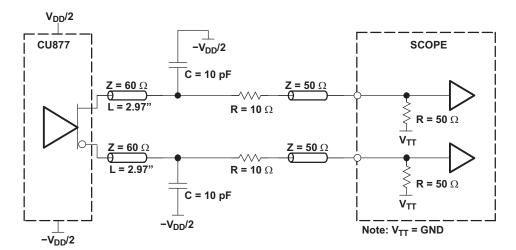


Figure 3. Output Load Test Circuit 2

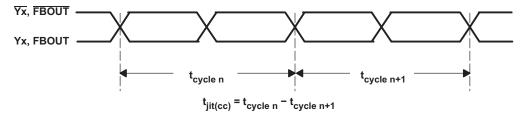


Figure 4. Cycle-To-Cycle Period Jitter

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1.8-V PHASE LOCK LOOP CLOCK DRIVER

PARAMETER MEASUREMENT INFORMATION (continued)

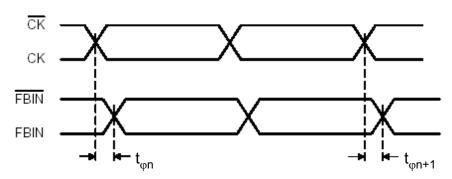


Figure 5. Static Phase Offset

$$t\phi = \frac{\sum_{1}^{n = N} t\phi n}{N}$$

(N is the large number of samples)

(N > 1000 samples)

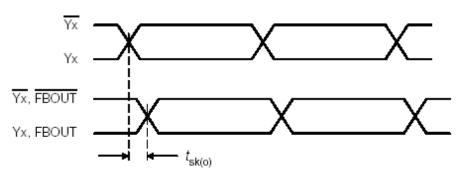


Figure 6. Output Skew

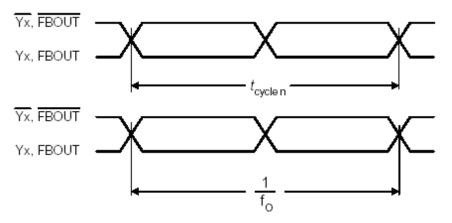


Figure 7. Period Jitter

$$t_{\text{jit(per)}} = t_{\text{cycle n}} - \frac{1}{f_{\text{O}}}$$

(f_O average input frequency measured at CK/\overline{CK}

(2)

(1)



PARAMETER MEASUREMENT INFORMATION (continued)

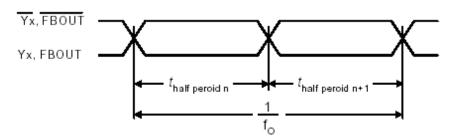


Figure 8. Half-Period Jitter

$$t_{jit(hper)} = t_{half period n} - \frac{1}{2 \times f_{O}}$$

n = any half cycle

(fo average input frequency measured at CK/CK

(3) 80% 80% V_{ID}, V_{OD} Clock Inputs and Outputs, OE 20% 20% $t_{r(i)}$, $t_{r(o)}$ $\mathbf{t}_{\mathsf{f}(\mathsf{i})}, \; \mathbf{t}_{\mathsf{f}(\mathsf{o})}$

Figure 9. Input and Output Slew Rates

$$sIrr_{(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{r(i/o)}} \qquad sIrf_{(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{f(i/o)}}$$

$$CK$$

$$CK$$

$$FBIN$$

$$FBIN$$

$$t_{\phi dyn}$$

Figure 10. Dynamic Phase Offset

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PARAMETER MEASUREMENT INFORMATION (continued)

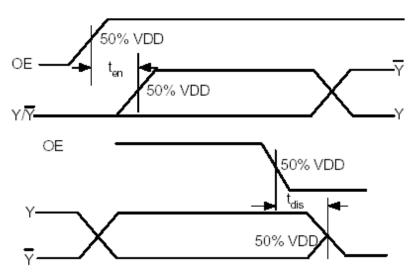
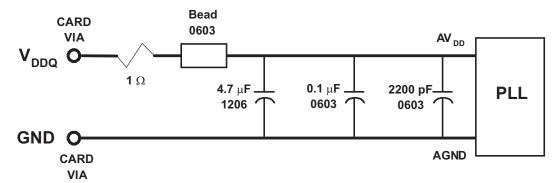


Figure 11. Time Delay Between OE and Clock Output (Y, \overline{Y})

RECOMMENDED AV_{DD} FILTERING



- A. Place the 2200-pF capacitor close to the PLL.
- B. Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).
- C. Recommended bead: Fair-Rite PN 2506036017Y0 or equilvalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

Figure 12. Recommended AV_{DD} Filtering





PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDCU877AGQLR	ACTIVE	BGA MI CROSTA R JUNI OR	GQL	52	1000	TBD	SNPB	Level-2-235C-1 YEAR
CDCU877AGQLT	ACTIVE	BGA MI CROSTA R JUNI OR	GQL	52	250	TBD	SNPB	Level-2-235C-1 YEAR
CDCU877ARHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877ARHARG4	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877ARHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877ARHATG4	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877ARTBR	ACTIVE	QFN	RTB	40	2500	TBD	CU SNPB	Level-3-235C-168 HR
CDCU877ARTBT	ACTIVE	QFN	RTB	40	250	TBD	CU SNPB	Level-3-235C-168 HR
CDCU877AZQLR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	52	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR
CDCU877AZQLT	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	52	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR
CDCU877GQLR	ACTIVE	BGA MI CROSTA R JUNI OR	GQL	52	1000	TBD	SNPB	Level-2-235C-1 YEAR
CDCU877GQLT	ACTIVE	BGA MI CROSTA R JUNI OR	GQL	52	250	TBD	SNPB	Level-2-235C-1 YEAR
CDCU877RHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877RHARG4	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877RHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877RHATG4	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCU877RTBR	ACTIVE	QFN	RTB	40	2500	TBD	CU SNPB	Level-3-235C-168 HR
CDCU877RTBT	ACTIVE	QFN	RTB	40	250	TBD	CU SNPB	Level-3-235C-168 HR
CDCU877ZQLR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	52	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAF
CDCU877ZQLT	ACTIVE	BGA MI CROSTA R JUNI	ZQL	52	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR



PACKAGE OPTION ADDENDUM

3-Jul-2007

	Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
Ī			OR					

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

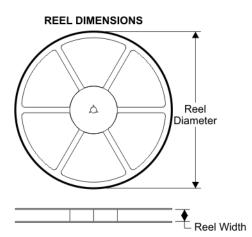
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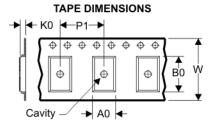
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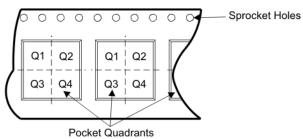
TAPE AND REEL BOX INFORMATION





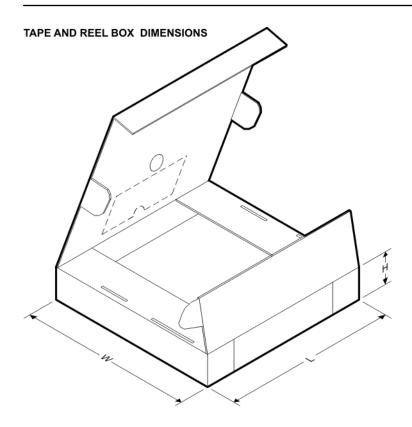
	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCU877AGQLR	GQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
CDCU877AGQLT	GQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
CDCU877ARHAR	RHA	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877ARHAT	RHA	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877ARTBR	RTB	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877ARTBT	RTB	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877AZQLR	ZQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
CDCU877AZQLT	ZQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
CDCU877GQLR	GQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
CDCU877GQLT	GQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
CDCU877RHAR	RHA	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877RHAT	RHA	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877RTBR	RTB	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877RTBT	RTB	40	SITE 28	330	16	6.3	6.3	1.5	12	16	Q2
CDCU877ZQLR	ZQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
CDCU877ZQLT	ZQL	52	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1

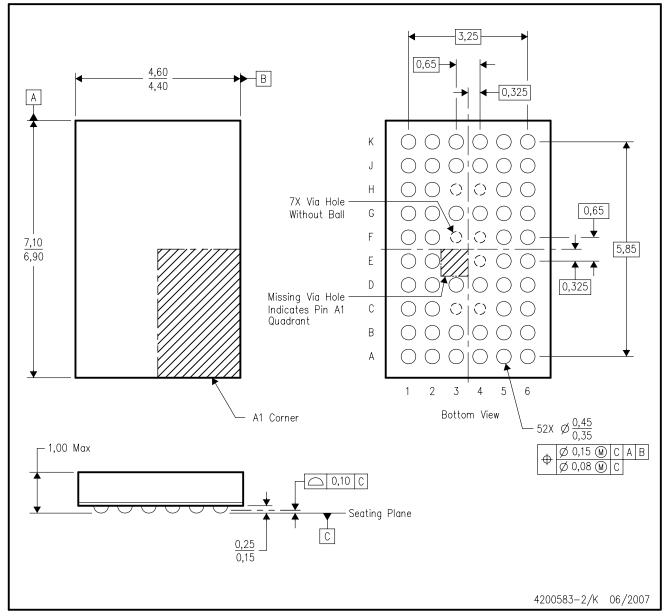




Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CDCU877AGQLR	GQL	52	SITE 60	342.9	336.6	28.58
CDCU877AGQLT	GQL	52	SITE 60	342.9	336.6	28.58
CDCU877ARHAR	RHA	40	SITE 28	342.9	336.6	28.58
CDCU877ARHAT	RHA	40	SITE 28	342.9	336.6	28.58
CDCU877ARTBR	RTB	40	SITE 28	342.9	336.6	28.58
CDCU877ARTBT	RTB	40	SITE 28	342.9	336.6	28.58
CDCU877AZQLR	ZQL	52	SITE 60	342.9	336.6	28.58
CDCU877AZQLT	ZQL	52	SITE 60	342.9	336.6	28.58
CDCU877GQLR	GQL	52	SITE 60	342.9	336.6	28.58
CDCU877GQLT	GQL	52	SITE 60	342.9	336.6	28.58
CDCU877RHAR	RHA	40	SITE 28	342.9	336.6	28.58
CDCU877RHAT	RHA	40	SITE 28	342.9	336.6	28.58
CDCU877RTBR	RTB	40	SITE 28	342.9	336.6	28.58
CDCU877RTBT	RTB	40	SITE 28	342.9	336.6	28.58
CDCU877ZQLR	ZQL	52	SITE 60	342.9	336.6	28.58
CDCU877ZQLT	ZQL	52	SITE 60	342.9	336.6	28.58

GQL (R-PBGA-N52)

PLASTIC BALL GRID ARRAY



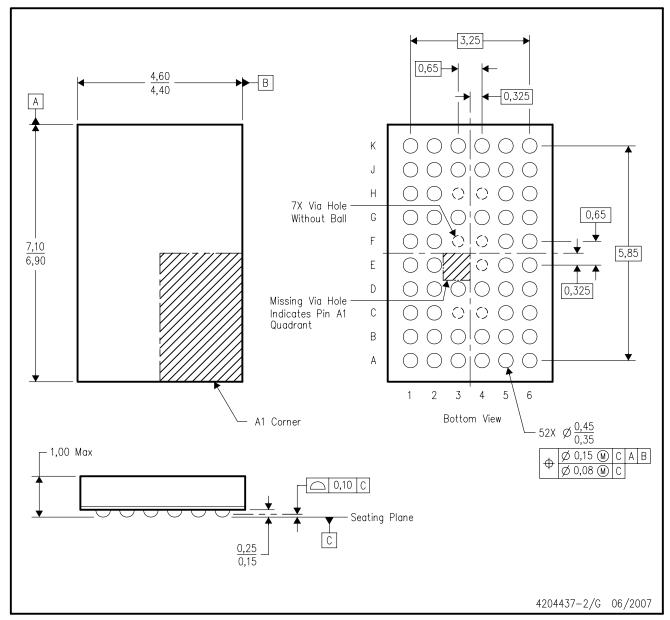
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 52 ZQL package (drawing 4204437) for lead-free.



ZQL (R-PBGA-N52)

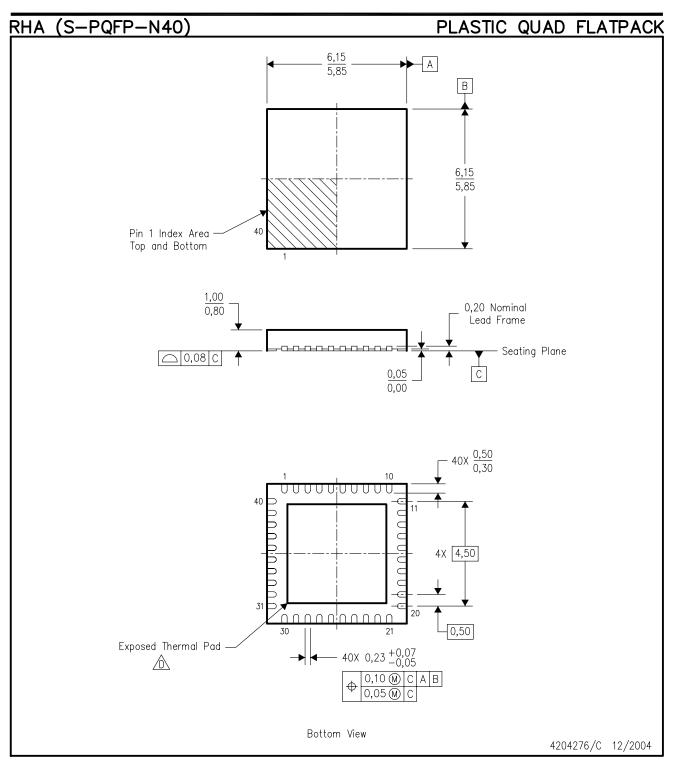
PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is lead-free. Refer to the 52 GQL package (drawing 4200583) for tin-lead (SnPb).





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Package complies to JEDEC MO-220 variation VJJD-2.



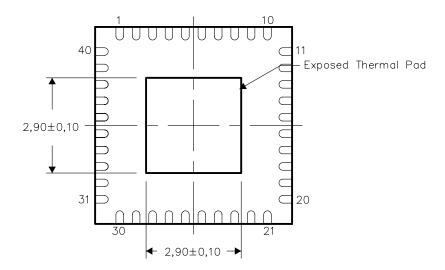


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No—Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

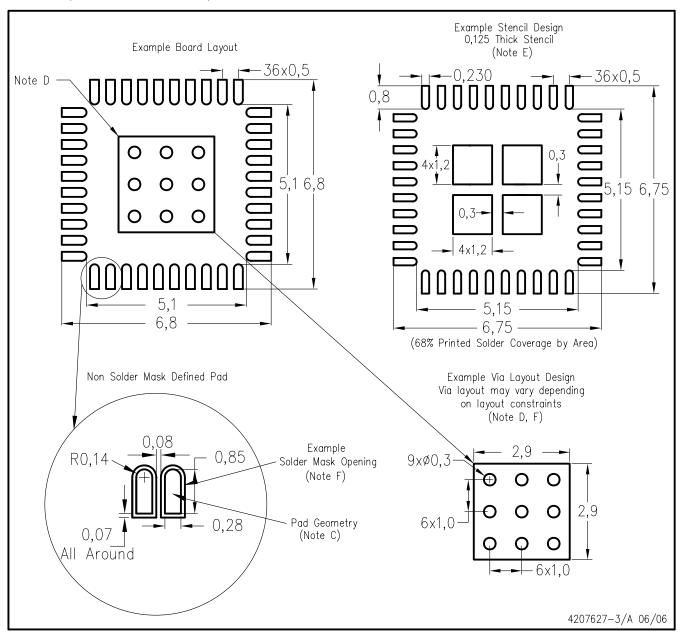


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHA (S-PQFP-N40)



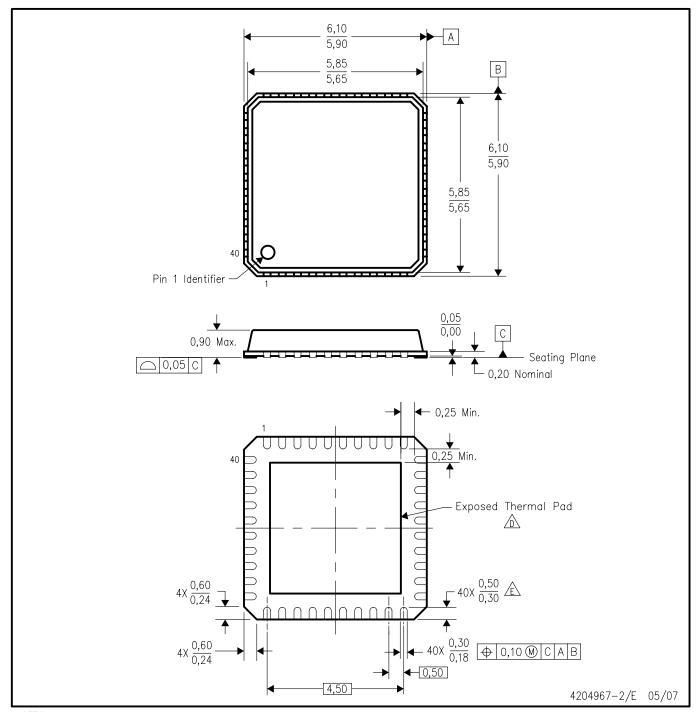
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



RTB (S-PQFP-N40)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions. Some products have selected lands extended past 0,50 length. See Product Data Sheet for details regarding specific land length exceptions.



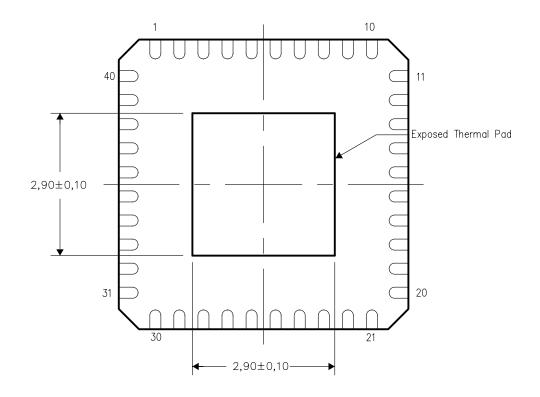


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No—Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

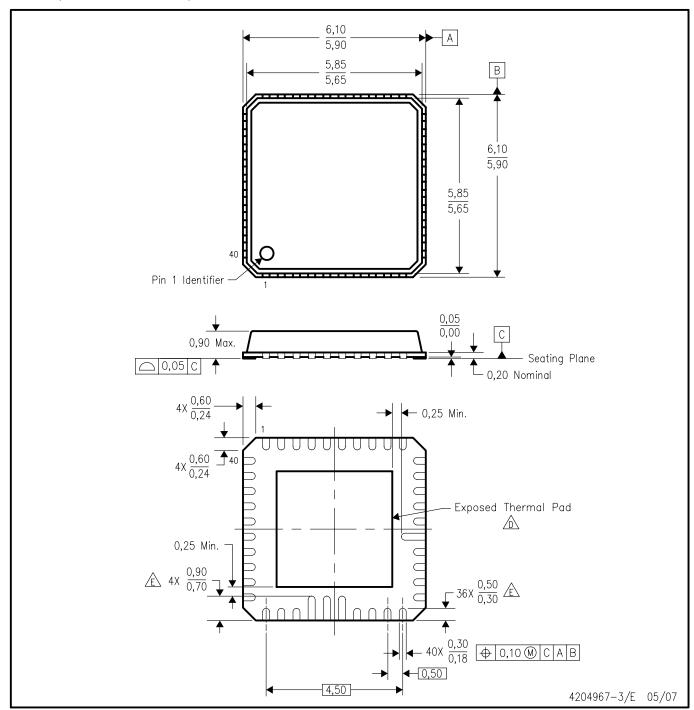


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RTB (S-PQFP-N40) *LONG LEAD OPTION* PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

Selected lands extended past 0,50 length.



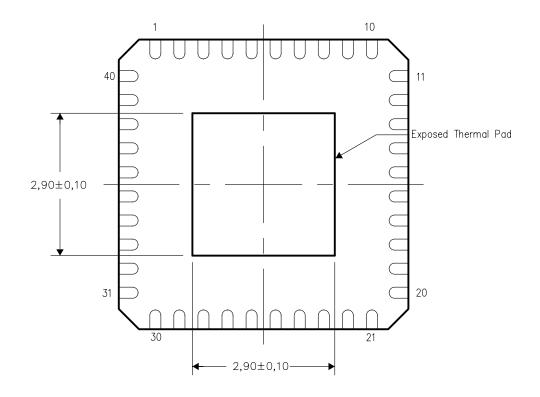


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No—Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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