TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor SCHS216D

November 1997 - Revised October 2003

Features

- Positive or Negative Edge Triggering
- Synchronous Internal Carry Propagation
- Fanout (Over Temperature Range)
 - Standard Outputs..... 10 LSTTL Loads
- Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, II \leq 1µA at VOL, VOH

Description

The CD74HC4518 is a dual BCD up-counter. The 'HC4520 and CD74HCT4520 are dual binary up-counters. Each device consists of two independent internally synchronous 4-stage counters. The counter stages are D-type flip-flops

Pinout

CD74HC4518, CD54HC4520, CD74HC4520, CD74HCT4520

High-Speed CMOS Logic Dual Synchronous Counters

having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or the negative-going transition of CLOCK. The counters are cleared by high levels on the MASTER RESET lines. The counter can be cascaded in the ripple mode by connecting Q_3 to the ENABLE input of the subsequent counter while the CLOCK input of the latter is held low.

Ordering Information

PART NUMBER	TEMP. RANGE (^o C)	PACKAGE
CD54HC4520F3A	-55 to 125	16 Ld CERDIP
CD74HC4518E	-55 to 125	16 Ld PDIP
CD74HC4520E	-55 to 125	16 Ld PDIP
CD74HC4520M	-55 to 125	16 Ld SOIC
CD74HC4520MT	-55 to 125	16 Ld SOIC
CD74HC4520M96	-55 to 125	16 Ld SOIC
CD74HCT4520E	-55 to 125	16 Ld PDIP
CD74HCT4520M	-55 to 125	16 Ld SOIC
CD74HCT4520MT	-55 to 125	16 Ld SOIC
CD74HCT4520M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.



1CP 1	U	16 V _{CC}
1E 2		15 2MR
1Q ₀ 3		14 2Q ₃
1Q ₁ 4		13 2Q ₂
1Q ₂ 5		12 2Q1
1Q3 6		11 2Q ₀
1MR 7		10 2E
GND 8		9 2CP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Functional Diagram



TRUTH TABLE

СР	E	MR	OUTPUT STATE
\uparrow	Н	L	Increment Counter
L	\downarrow	L	Increment Counter
\downarrow	Х	L	No Change
Х	↑ (L	No Change
↑ (L	L	No Change
Н	\downarrow	L	No Change
Х	Х	Н	Q_0 thru $Q_3 = L$

H = High State.

L = Low State.

 \uparrow = High-to-Low Transition.

 \downarrow = Low-to-High Transition.

X = Don't Care.

Absolute Maximum Ratings

DC Supply Voltage, V _{CC}
DC Input Diode Current, I _{IK}
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ±20mA
DC Output Diode Current, I _{OK}
For $V_0 < -0.5V$ or $V_0 > V_{CC} + 0.5V$
DC Output Source or Sink Current per Output Pin, IO
For $V_{O} > -0.5V$ or $V_{O} < V_{CC} + 0.5V$
DC V _{CC} or Ground Current, I _{CC} ±50mA

Operating Conditions

Temperature Range, T _A 55 ^o C to 125 ^o C Supply Voltage Range, V _{CC}
HC Types
HCT Types
DC Input or Output Voltage, VI, VO $\ldots \ldots \ldots $ 0V to V _{CC}
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^o C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150 ⁰ C
Maximum Storage Temperature Range	65 ⁰ C to 150 ⁰ C
Maximum Lead Temperature (Soldering 10s)	
(SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

			TEST CONDITIONS		25 ⁰ C			-40°C TO 85°C		-55 ⁰ C TO 125 ⁰ C			
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES	-						-	-			_		
High Level Input	VIH	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input	VIL	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V	
emee Loads			-0.02	6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output	1		-	-	-	-	-	-	-	-	-	V	
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V	
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V	
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V	
emee Loads					0.02	6	-	-	0.1	-	0.1	-	0.1
Low Level Output			-	-	-	-	-	-	-	-	-	V	
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V	
TTE LOAUS			5.2	6	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	lı	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA	
Quiescent Device Current	ICC	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA	

CD74HC4518, CD54HC4520, CD74HC4520, CD74HCT4520

DC Electrical Specifications	(Continued)
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PARAMETER		TEST CONDITIONS			25 ⁰ C			-40°C TO 85°C		-55 ⁰ C TO 125 ⁰ C		
	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES		-							-			
High Level Input Voltage	VIH	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	∆I _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
MR	1.2
СР	0.25
ENABLE	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25^oC.

Prerequisite for Switching Specifications

			25 ⁰ C			-40 ⁰ C 1	ГО 85 ⁰ С	-55°C TO 125°C		
PARAMETER	SYMBOL	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES										
Maximum Clock	f _{MAX}	2	6	-	-	5	-	4	-	MHz
Frequency		4.5	30	-	-	24	-	20	-	MHz
		6	35	-	-	28	-	24	-	MHz
CP Pulse Width	t _W	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR Pulse Width	t _W	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns

CD74HC4518, CD54HC4520, CD74HC4520, CD74HCT4520

			25 ⁰ C			-40°C 1	ГО 85 ⁰ С	-55 ⁰ C T		
PARAMETER	SYMBOL	V _{CC} (V)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNITS
Set-up Time,	t _{SU}	2	80	-	-	100	-	120	-	ns
Enable to CP		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Removal Time,	t _{REM}	2	0	-	-	0	-	0	-	ns
MR to CP		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Set-up Time,	tsu	2	80	-	-	100	-	120	-	ns
CP to Enable		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Removal Time,	t _{REM}	2	0	-	-	0	-	0	-	ns
MR to Enable		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
HCT TYPES	•					-				
Maximum Clock Frequency	f _{MAX}	4.5	25	-	-	20	-	17	-	MHz
Clock Pulse Width	t _W	4.5	20	-	-	25	-	30	-	ns
MR Pulse Width	t _W	4.5	20	-	-	25	-	30	-	ns
Set-up Time, Enable to CP	tsu	4.5	16	-	-	20	-	24	-	ns
Removal Time, MR tp Enable	^t REM	4.5	0	-	-	0	-	0	-	ns

Prerequisite for Switching Specifications (Continued)

Switching Specifications Input t_r , $t_f = 6ns$

		TEST		25°C		-40 ^o C TO 85 ^o C		-55°C TO 125°C			
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES											
Propagation Delay	t _{PLH,}	$C_L = 50 pF$	2	-	-	240	-	300	-	360	ns
CP to Q _n	t _{PHL}	$C_L = 50 pF$	4.5	-	-	48	-	60	-	72	ns
		C _L = 15pF	5	-	20	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	41	-	51	-	61	ns
Enable to Q _n	t _{PLH,}	C _L = 50pF	2	-	-	240	-	300	-	360	ns
	^t PHL	C _L = 50pF	4.5	-	-	48	-	60	-	72	ns
		C _L = 15pF	5	-	20	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	41	-	51	-	61	ns
MR to Q _n	t _{PLH,}	C _L = 50pF	2	-	-	150	-	190	-	225	ns
	^t PHL [′]	C _L = 50pF	4.5	-	-	30	-	38	-	45	ns
		C _L = 15pF	5	-	12	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	26	-	33	-	38	ns
Output Transition Time	t _{THL} , t _{TLH}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
		C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
		CL = 50pF	6			13		16		19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f _{MAX}	CL = 15pF	5		60						MHz
Power Dissipation Capacitance (Note 3, 4)	C _{PD}	C _L = 15pF	5	-	33	-	-	-	-	-	pF

		TEST		25 ⁰ C			-40°C TO 85 ⁰ C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES											
Propagation Delay											
CP to Q _n	t _{PLH,}	$C_L = 50 pF$	4.5	-	-	53	-	66	-	80	ns
	^t PHL	C _L = 15pF	5	-	22	-	-	-	-	-	ns
Enable to Q _n	t _{PLH,}	C _L = 50pF	4.5	-	-	55	-	69	-	83	ns
	^t PHL	C _L = 15pF	5	-	23	-	-	-	-	-	ns
MR to Q _n	t _{PLH,}	C _L = 50pF	4.5	-	-	35	-	44	-	53	ns
	^t PHL [′]	C _L = 15pF	5	-	14	-	-	-	-	-	ns
Output Transition Time	t _{THL} , t _{TLH}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f _{MAX}	CL = 15pF	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Note 3,4)	C _{PD}	-	5	-	33	-	-	-	-	-	pF

Switching Specifications Input t_r , $t_f = 6ns$ (Continued)

NOTES:

3. $C_{\mbox{PD}}$ is used to determine the dynamic power consumption, per counter.

4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.



Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



FIGURE 4. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC







NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 3. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH











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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8995401EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC4520F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HC4520F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC4518E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4518EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4520E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4520EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4520M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4520MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT4520EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT4520M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74HCT4520M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4520MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and pa

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD54HC4520, CD74HC4520 :

Catalog: CD74HC4520

Military: CD54HC4520

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4520M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4520M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

19-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4520M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4520M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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