

Data sheet acquired from Harris Semiconductor SCHS170B

November 1997 - Revised October 2003

High-Speed CMOS Logic Dual 4-Input Multiplexer

Features

- Common Select Inputs
- Separate Output-Enable Inputs
- Three-State Outputs
- Fanout (Over Temperature Range)
 - Standard Outputs......10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility,
 V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, I $_I \leq 1 \mu A$ at $V_{OL},\,V_{OH}$

Description

The CD74HC253 and CD74HCT253 are dual 4-to-1 line selector/multiplexers having three-state outputs. One of four sources for each section is selected by the common select inputs, S0 and S1. When the output enable $(\overline{10E}, \overline{20E})$ is HIGH, the output is in the high-impedance state.

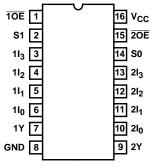
Ordering Information

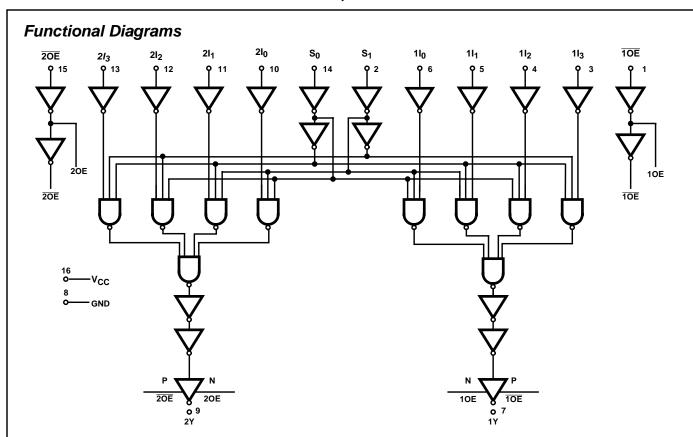
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC253E	-55 to 125	16 Ld PDIP
CD74HC253M	-55 to 125	16 Ld SOIC
CD74HC253MT	-55 to 125	16 Ld SOIC
CD74HC253M96	-55 to 125	16 Ld SOIC
CD74HCT253E	-55 to 125	16 Ld PDIP
CD74HCT253M	-55 to 125	16 Ld SOIC
CD74HCT253MT	-55 to 125	16 Ld SOIC
CD74HCT253M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD74HC253, CD74HCT253 (PDIP, SOIC) TOP VIEW





TRUTH TABLE

	INPUTS te 1)		DATA I	OUTPUT ENABLE	ОИТРИТ		
S1	S0	I ₀	I ₁	l ₂	l ₃	ŌĒ	Y
Х	Х	Х	Х	Х	Х	Н	Z
L	L	L	Х	Х	Х	L	L
L	L	Н	Х	Х	Х	L	Н
L	Н	Х	L	Х	Х	L	L
L	Н	Х	Н	Х	Х	L	Н
Н	L	Х	Х	L	Х	L	L
Н	L	Х	Х	Н	Х	L	Н
Н	Н	Х	Х	Х	L	L	L
Н	Н	Х	X	Х	Н	L	Н

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance (Off). NOTE:

1. Select inputs S1 and S0 are common to both sections.

Absolute Maximum Ratings

DC Supply Voltage, V _{CC} 0.5V to	7V
DC Input Diode Current, I _{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	mΑ
DC Output Diode Current, I _{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	mΑ
DC Drain Current, per Output, I _O	
For -0.5V < V _O < V _{CC} + 0.5V	mΑ
DC Output Source or Sink Current per Output Pin, IO	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	mΑ
DC V _{CC} or Ground Current, I _{CC}	nΑ

Thermal Information

Thermal Resistance (Typical, Note 2)	θ _{JA} (°C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	
Maximum Storage Temperature Range6	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T _A 55°C to 125°C Supply Voltage Range, V _{CC}
HC Types
HCT Types
DC Input or Output Voltage, V _I , V _O 0V to V _{CC}
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TES CONDI				/cc 25°C			O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES	HC TYPES											
High Level Input	V _{IH}	-	-	2	1.5	i	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	•	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	V _{OH}	OH VIH or VIL	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
Owied Eddas			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
112 20005			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Owo Educa			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output			-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-6	4.5	-	-	0.26	-	0.33	-	0.4	V
			-7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	Ι _Ι	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μА

DC Electrical Specifications (Continued)

			TEST CONDITIONS						25°C		-40°C 1	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS			
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μА			
HCT TYPES															
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V			
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V			
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V			
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V			
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V			
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V			
Input Leakage Current	lį	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μА			
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μА			
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 3)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μА			
Three-State Leakage Current	l _{OZ}	V _{IL} or V _{IH}	V _O = V _{CC} or GND	5.5	-	-	±0.5	-	±5	-	±10	μА			

NOTE:

3. For dual-supply systems theoretical worst case ($V_I = 2.4V$, $V_{CC} = 5.5V$) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
1l _O - 1l ₃ , 2l _O -2l ₃	0.4
1E _O , 2E _O , S ₀ , S ₁	1

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

		TEST	V _{CC}		25°C		-40 ⁰ 85	С ТО °С		C TO 5°C	
PARAMETER	SYMBOL	YMBOL CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES	-										
Propagation Delay	,	C _L = 50pF	2	-	-	175	-	220	-	265	ns
Select to Outputs	^t PHL		4.5	-	-	35	-	44	-	53	ns
		C _L =15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	45	ns

Switching Specifications Input t_r , t_f = 6ns (Continued)

		TEST	v _{cc}		25°C		-40°C TO 85°C		-55°C TO 125°C		
PARAMETER SYMBOL		CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Data to Outputs	t _{PLH,}	C _L = 50pF	2	-	-	175	-	220	-	265	ns
	t _{PHL}		4.5	-	-	35	-	44	-	53	ns
		C _L =15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	45	ns
Disable Delay Times	t _{PHZ} , t _{PLZ}	C _L = 50pF	2	-	-	150	-	190	-	225	ns
		C _L = 50pF	4.5	-	-	30	-	38	-	45	ns
		CL = 15pF	5	-	12	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	26	-	33	-	38	ns
Enable Delay Times	t _{PZH} ,	C _L = 50pF	2	-	-	110	-	140	-	165	ns
	tPZL	CL = 50pF	4.5	-	-	22	-	28	-	33	ns
		CL = 15pF	5	-	9	-	-	-	-	-	ns
		CL = 50pF	6	-	-	19	-	24	-	28	ns
Output Transition Times	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	Cl	-	-	-	-	10	-	10	-	10	pF
Three-State Output Capacitance	СО	-	-	-	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	46	-	-	-	-	-	pF
HCT TYPES					•						
Propagation Delay Select to Outputs	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	_	-	40	-	50	-	60	ns
		C _L =15pF	5	-	16	-	-		-	-	ns
Data to Outputs	t _{PLH} ,	C _L = 50pF	4.5	-	-	38	-	48	-	57	ns
	t _{PHL}	C _L =15pF	5	-	16	-	-	-	-	-	ns
Disable Delay Times	t _{PLH} ,	C _L = 50pF	4.5	-		30	-	38	-	45	ns
	t _{PHL}	C _L =15pF	5	-	12	-	-	-	-	-	ns
Enable Delay Times	t _{PZH} ,	C _L = 50pF	4.5	-	-	30	-	38	-	45	ns
	t _{PZL}	C _L =15pF	5	-	12	-	-	-	-	-	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	C _{IN}	-	-	-	-	10	-	10	-	10	pF
Three-State Output Capacitance	СО	-	-	-	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	52	-	-	-	-	-	pF

^{4.} $C_{\mbox{\scriptsize PD}}$ is used to determine the dynamic power consumption, per multiplexer.

^{5.} $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

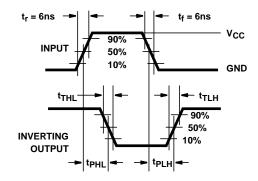


FIGURE 1. HC AND HCT TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC

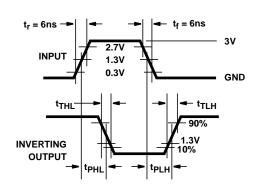


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

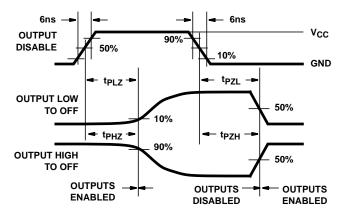


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

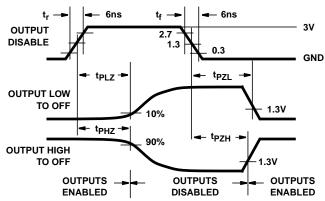
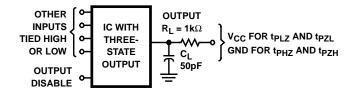


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT







PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HC253E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC253EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC253M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC253ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC253MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC253MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC253MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC253MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT253EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT253M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT253MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

 $^{^{(1)}}$ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

23-Apr-2007

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

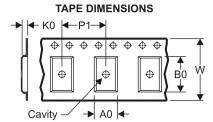
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



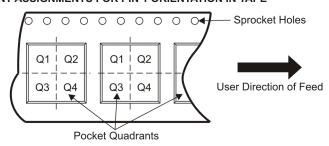
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

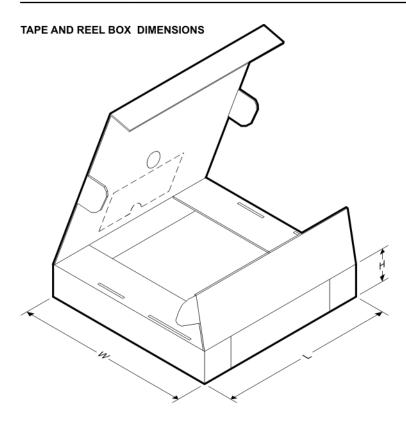
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT253M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT253M96	SOIC	D	16	2500	333.2	345.9	28.6

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE

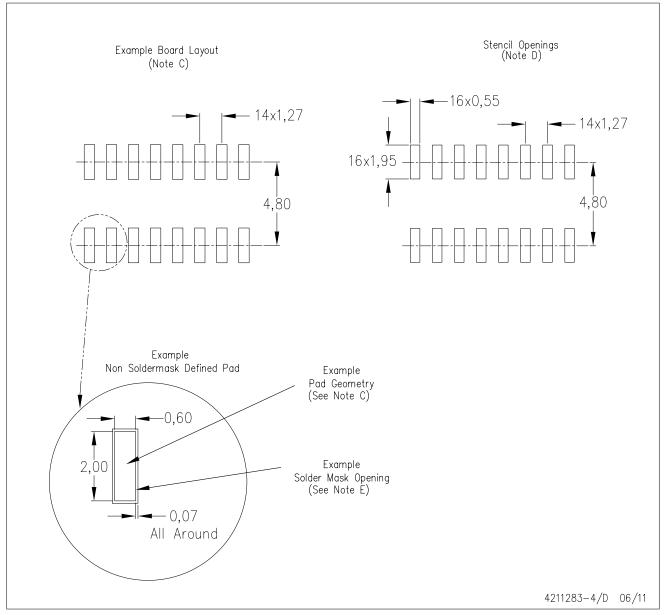


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications			
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications		
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers		
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps		
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy		
DSP	dsp.ti.com	Industrial	www.ti.com/industrial		
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical		
Interface	interface.ti.com	Security	www.ti.com/security		
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense		
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive		
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video		
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps		
RF/IF and ZigBee® Solutions	www.ti.com/lprf				

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated

e2e.ti.com

TI E2E Community Home Page