

Dual 4-Input Multiplexer, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay
 - 6.3ns at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- $\pm 24mA$ Output Drive Current
 - Fanout to 15 FAST™ ICs
 - Drives 50 Ω Transmission Lines

Description

The CD74AC253 and 'ACT253 dual 4-input multiplexers that utilize Advanced CMOS Logic technology. One of the four sources for each section is selected by the common Select inputs, S0 and S1. When the Output Enable (1OE or 2OE) is HIGH, the output is in the high-impedance state.

Ordering Information

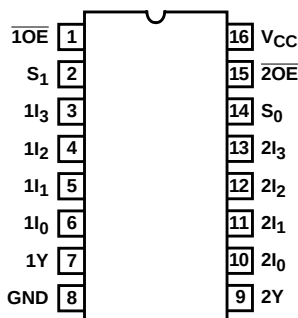
PART NUMBER	TEMP. RANGE ($^{\circ}C$)	PACKAGE
CD74AC253E	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld PDIP
CD74AC253M	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld SOIC
CD54ACT253F3A	-55 to 125	16 Ld CERPDP
CD74ACT253E	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld PDIP
CD74ACT253M	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld SOIC

NOTES:

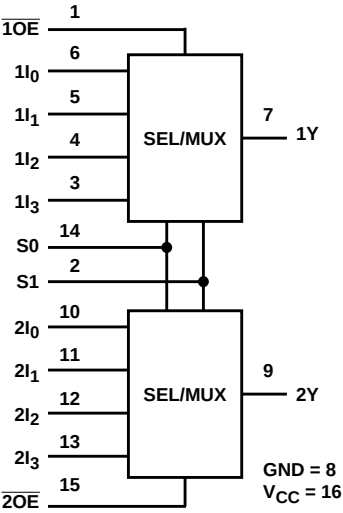
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinout

CD54ACT253
(CERPDP)
CD74AC253, CD74ACT253
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

SELECT INPUTS		DATA INPUTS				ENABLE INPUTS	OUTPUT
S1	S0	nl ₀	nl ₁	nl ₂	nl ₃	$\overline{nOE}$	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S1 and S0 are common to both sections. H = High level, L = Low inputs, X = Don't care, Z = High impedance.

CD74AC253, CD54/74ACT253

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 6V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 50mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 50mA$
 DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3) $\pm 100mA$

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} ($^{\circ}C/W$)
 PDIP Package
 SOIC Package
 Maximum Junction Temperature (Plastic Package) $150^{\circ}C$
 Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$

Operating Conditions

Temperature Range, T_A $-55^{\circ}C$ to $125^{\circ}C$
 Supply Voltage Range, V_{CC} (Note 4)
 AC Types 1.5V to 5.5V
 ACT Types 4.5V to 5.5V
 DC Input or Output Voltage, V_I , V_O 0V to V_{CC}
 Input Rise and Fall Slew Rate, dt/dv
 AC Types, 1.5V to 3V 50ns (Max)
 AC Types, 3.6V to 5.5V 20ns (Max)
 ACT Types, 4.5V to 5.5V 10ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
- Unless otherwise specified, all voltages are referenced to ground.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V _{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V _{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V

CD74AC253, CD54/74ACT253

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Three-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	μA
Quiescent Supply Current MSI	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μA
ACT TYPES											
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Three-State or Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	μA
Quiescent Supply Current MSI	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

CD74AC253, CD54/74ACT253

ACT Input Load Table

INPUT	UNIT LOAD
S0, S1, nI ₀ , nI ₁	1
nOE	0.83

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input t_r , t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V _{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, S0, S1, to Y	t _{PLH} , t _{PHL}	1.5	-	-	227	-	-	250	ns
		3.3 (Note 9)	7.2	-	25	7	-	28	ns
		5 (Note 10)	5.2	-	18.2	5	-	20	ns
Propagation Delay, nI to Y	t _{PLH} , t _{PHL}	1.5	-	-	151	-	-	166	ns
		3.3	4.8	-	16.9	4.7	-	18.6	ns
		5	3.4	-	12.1	3.3	-	13.3	ns
Propagation Delay, Output Enable, Output Disable to Y	t _{PLZ} , t _{PHZ} , t _{PZL} , t _{PZH}	1.5	-	-	131	-	-	144	ns
		3.3	4.5	-	15.7	4.3	-	17.3	ns
		5	3	-	10.5	2.9	-	11.5	ns
Three-State Output Capacitance	C _O	-	-	-	15	-	-	15	pF
Input Capacitance	C _I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C _{PD} (Note 11)	-	-	107	-	-	107	-	pF
ACT TYPES									
Propagation Delay, S0, S1, to Y	t _{PLH} , t _{PHL}	5 (Note 10)	5.7	-	20	5.5	-	22	ns
Propagation Delay, nI to Y	t _{PLH} , t _{PHL}	5	4.6	-	16.4	4.5	-	18	ns
Propagation Delay, Output Enable, Output Disable to Y	t _{PLZ} , t _{PHZ} , t _{PZL} , t _{PZH}	5	3.2	-	11.5	3.2	-	12.6	ns
Three-State Output Capacitance	C _O	-	-	-	15	-	-	15	pF
Input Capacitance	C _I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C _{PD} (Note 11)	-	-	107	-	-	107	-	pF

NOTES:

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per multiplexer.
 AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
 ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

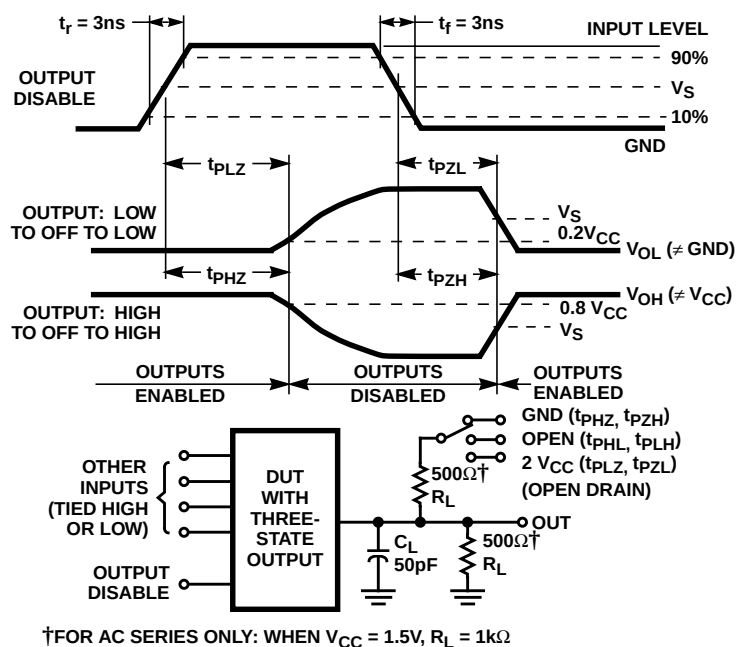


FIGURE 1. THREE-STATE PROPAGATION DELAY WAVEFORMS AND TEST CIRCUIT

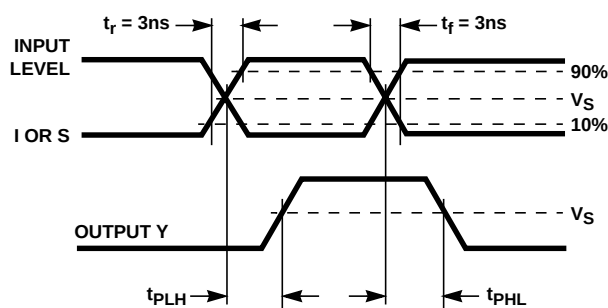
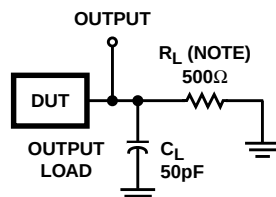


FIGURE 2. PROPAGATION DELAY TIMES



NOTE: For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

FIGURE 3. PROPAGATION DELAY TIMES

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