

CD40175B Types

CMOS Quad 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

Features:

- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Output compatible with two HTL loads, two low power TTL loads, or one low power Schottky TTL load
- Functional equivalent to TTL 74175
- Standardized symmetrical output characteristics

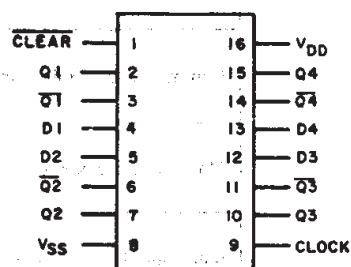
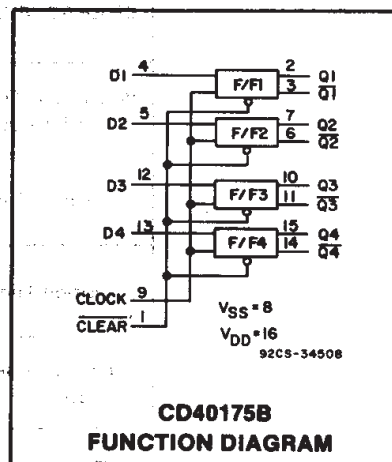
Applications:

- Shift registers
- Buffer/storage registers
- Pattern generators

■ CD40175B consists of four identical D-type flip-flops. Each flip-flop has an independent DATA D input and complementary Q and \bar{Q} outputs. The CLOCK and CLEAR inputs are common to all flip-flops. Data are transferred to the Q outputs on the positive-going transition of the clock pulse. All four flip-flops are simultaneously reset by a low level on the CLEAR input.

These devices can function as shift register elements or as T-type flip-flops for toggle and counter applications.

The CD40175B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



V_{DD} = PIN 16
 V_{SS} = PIN 8

92CS-34507

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal)

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to +20V

DC INPUT CURRENT, ANY ONE INPUT -0.5V to $V_{DD} + 0.5$ V

POWER DISSIPATION PER PACKAGE (P_D): ± 10 mA

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package-Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max +265°C

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RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	—	3	18	V
Data Setup Time t_{SU}	5	120	—	ns
	10	50	—	ns
	15	40	—	ns
Data Hold Time t_H	5	80	—	ns
	10	40	—	ns
	15	30	—	ns
Clock Input Frequency f_{CL}	5	—	2	MHz
	10	dc	5	MHz
	15	—	6.5	MHz
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	—	15	μs
	10	—	15	μs
	15	—	15	μs
Clock Input Pulse Width t_{WL}, t_{WH}	5	250	—	ns
	10	100	—	ns
	15	75	—	ns
Clear Pulse Width t_{WL}	5	200	—	ns
	10	80	—	ns
	15	60	—	ns
Clear Removal Time t_{REM}	5	250	—	ns
	10	100	—	ns
	15	80	—	ns

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

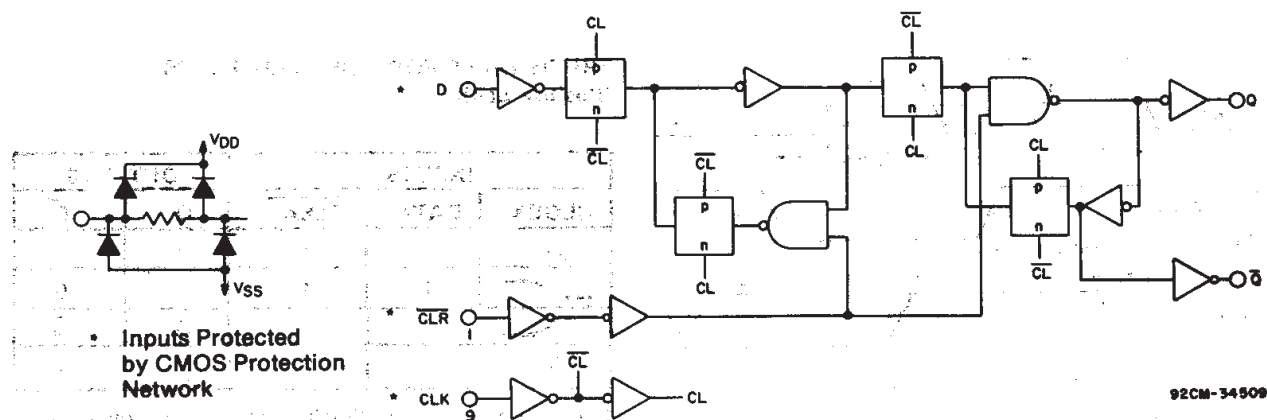


Fig. 1 - Logic diagram (1 of 4 flip-flops).

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
					Vo (V)	VIN (V)	VDD (V)	-55	-40	+85	+125	
		Min.	Typ.	Max.								
Quiescent Device Current Max. I _{DD}		—	0, 5	5	1	1	30	30	—	0.02	1	μA
		—	0, 10	10	2	2	60	60	—	0.02	2	
		—	0, 15	15	4	4	120	120	—	0.02	4	
		—	0, 20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current Min. I _{OL}		0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
		0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
		1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min. I _{OH}		4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
		2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
		9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
		13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level Max. V _{OL}		—	0, 5	5	0.05				—	0	0.05	V
		—	0, 10	10	0.05				—	0	0.05	
		—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min. V _{OH}		—	0, 5	5	4.95				4.95	5	—	V
		—	0, 10	10	9.95				9.95	10	—	
		—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage Max. V _{IL}		0.5,4.5	—	5	1.5				—	—	1.5	V
		1, 9	—	10	3				—	—	3	
		1.5,13.5	—	15	4				—	—	4	
Input High Voltage Min. V _{IH}		0.5,4.5	—	5	3.5				3.5	—	—	V
		1, 9	—	10	7				7	—	—	
		1.5,13.5	—	15	11				11	—	—	
Input Current Max. I _{IIN}		—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

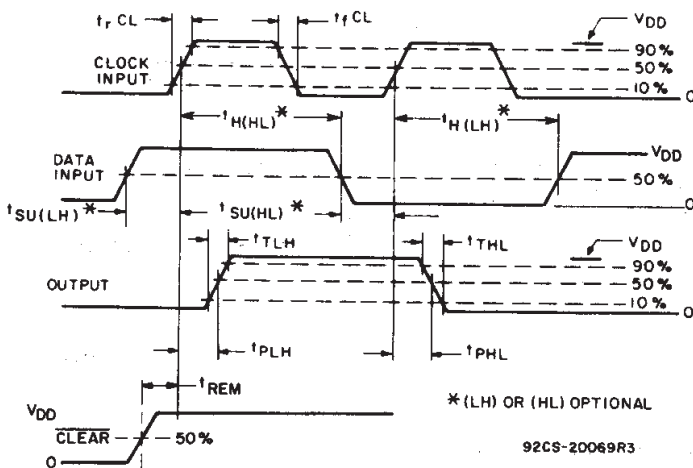


Fig. 2 - Definition of setup, hold, propagation delay, and removal times.

TRUTH TABLE FOR 1 OF 4 FLIP-FLOPS (Positive Logic)

INPUTS			OUTPUTS	
CLOCK	DATA	CLEAR	Q	\overline{Q}
	0	1	0	1
	1	1	1	0
	X	1	Q	\overline{Q}
X	X	0	0	1

1=High Level

X=Don't Care

0=Low Level

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Transition Time t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Propagation Delay Time Clock to Q Output t_{PHL}, t_{PLH}	5	—	220	400	
	10	—	90	160	
	15	—	70	120	
Propagation Delay Time $\overline{\text{CLEAR}}$ to Q Output t_{PHL}	5	—	325	500	
	10	—	130	200	
	15	—	100	150	
Minimum Pulse Width Clock t_{WH}	5	—	110	250	
	10	—	45	100	
	15	—	35	75	
$\overline{\text{Clear}}$ t_{WL}	5	—	100	200	
	10	—	40	80	
	15	—	30	60	
Maximum Clock Frequency f_{CL}	5	2	4.5	—	MHz
	10	5	11	—	
	15	6.5	14	—	
Maximum Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	15	—	—	μs
	10	15	—	—	
	15	15	—	—	
Minimum Data Setup Time t_{SU}	5	—	60	120	ns
	10	—	25	50	
	15	—	20	40	
Minimum Data Hold Time t_H	5	—	40	80	
	10	—	20	40	
	15	—	15	30	
Minimum $\overline{\text{Clear}}$ Removal Time \ddagger t_{REM}	5	—	125	250	
	10	—	50	100	
	15	—	40	80	
Input Capacitance C_{IN}	—	—	5	7.5	pF

\ddagger $\overline{\text{CLEAR}}$ signal must be high prior to positive-going transition of CLOCK pulse.

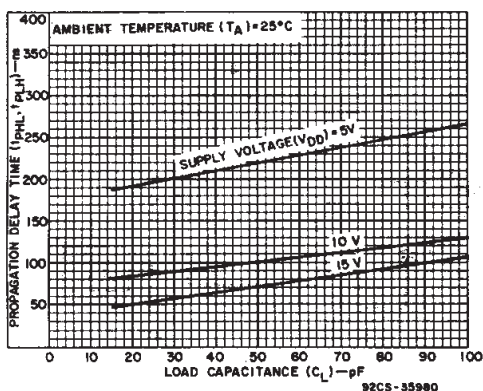


Fig. 3 - Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

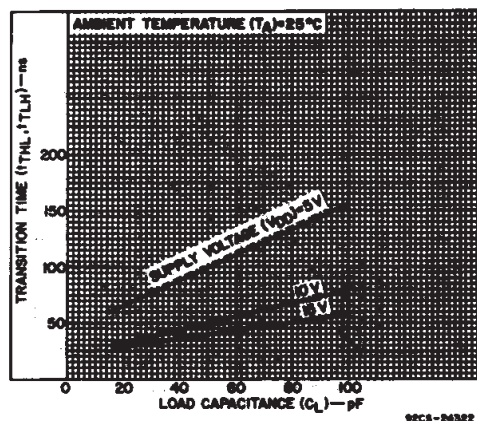


Fig. 4 - Typical transition time as a function of load capacitance.

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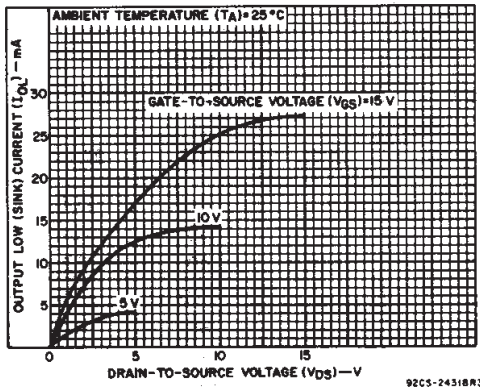


Fig. 5 - Typical output low (sink) current characteristics.

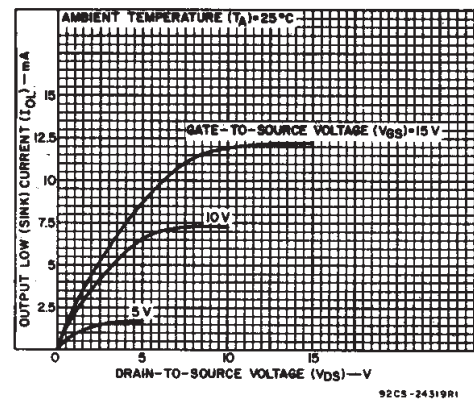


Fig. 6 - Minimum output low (sink) current characteristics.

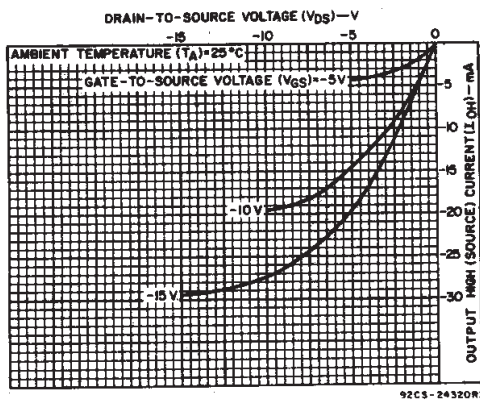


Fig. 7 - Typical output high (source) current characteristics.

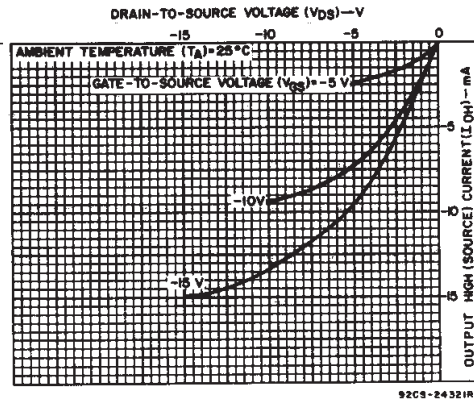


Fig. 8 - Minimum output high (source) current characteristics.

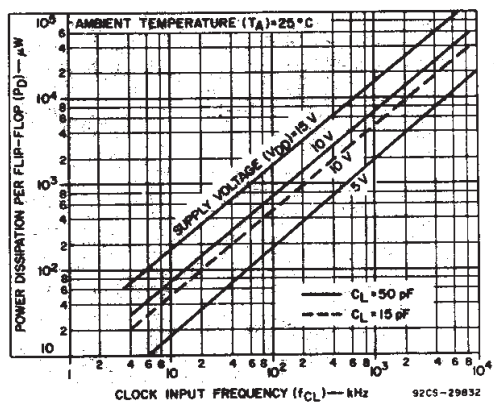


Fig. 9 - Typical dynamic power dissipation as a function of CLOCK frequency.

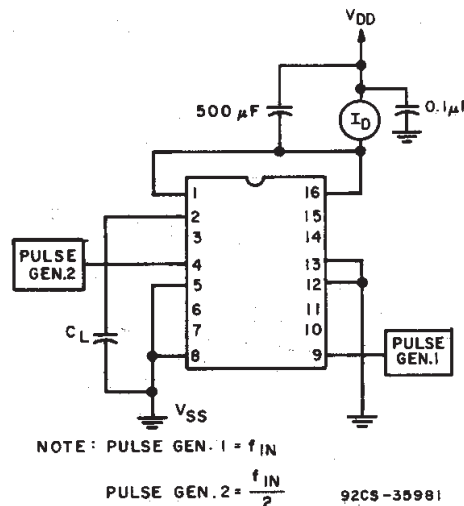


Fig. 10 - Dynamic power dissipation test circuit.

CD40175B Types

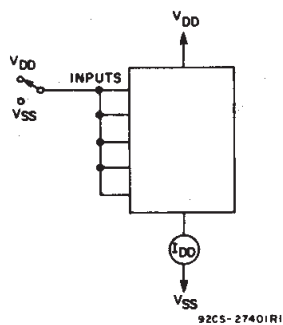


Fig. 11 - Quiescent device current test circuit.

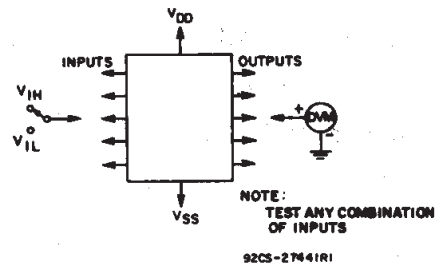


Fig. 12 - Noise immunity test circuit.

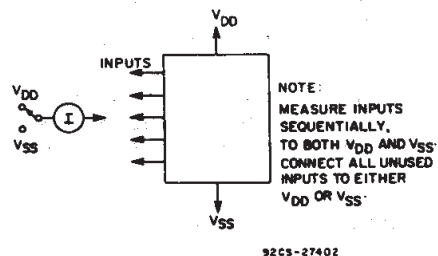
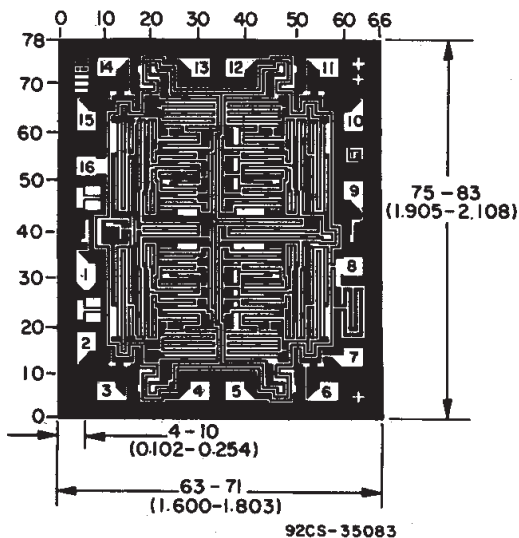


Fig. 13 - Input leakage current test circuit.



Dimensions and pad layout for CD40175BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD40175BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40175BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40175BF3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD40175BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40175BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

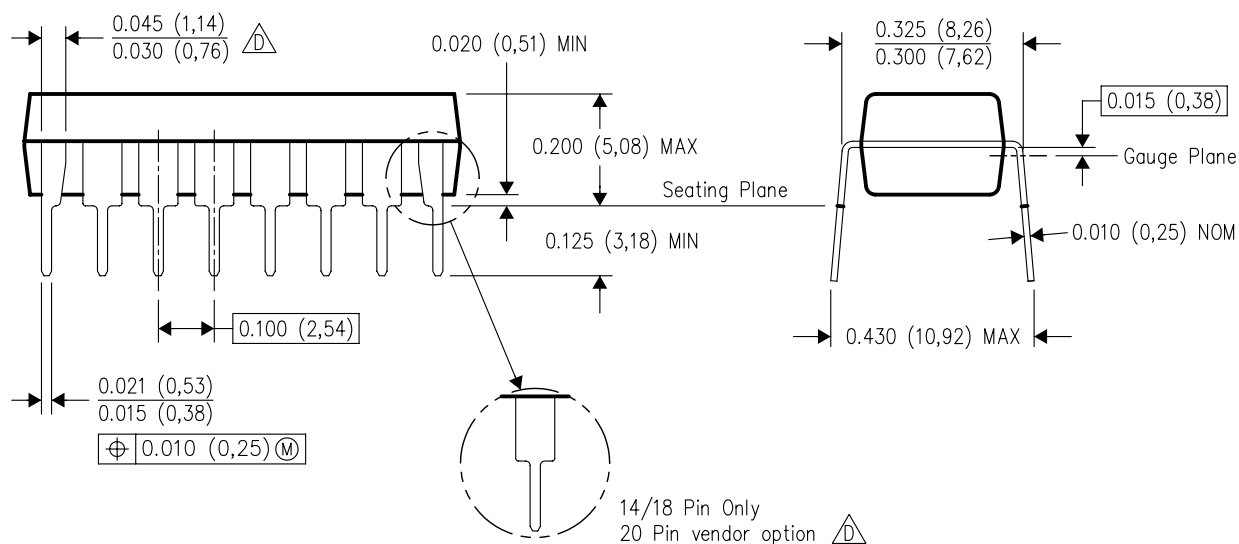
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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