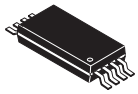


SLUS607 − MAY 2004

HIGH-PERFORMANCE BATTERY MONITOR IC WITH COULOMB COUNTER, VOLTAGE AND, TEMPERATURE MEASUREMENT

FEATURES

- **Communicates Directly With the Integrated HDQ Engine in TI OMAP™ Processor**
- **Multifunction Monitoring Integrated Circuit Designed to Work With an Intelligent Host Controller :**
  - **Provides State of Charge Information for Rechargeable Batteries**
  - **Provides Accurate Battery Voltage and Temperature Measurement**
- **High Accuracy Coulometric Charge and Discharge Current Integration With Automatic Offset Compensation**
- **11-Bit Analog-to-Digital Converter Reports Battery Voltage With Gain and Offset Correction**
- **Differential Current Sense**
- **32 Bytes of General Purpose RAM**
- **96 Bytes of Flash (Including 32 Bytes of Shadow Flash)**
- **8 Bytes of ID ROM**
- **Internal Temperature Sensor Eliminates the Need for an External Thermistor**
- **Programmable Digital Input/Output Port**
- **High-Accuracy Internal Timebase Eliminates External Crystal Oscillator**
- **Low Power Consumption:**
  - **Operating : 30 μA**
  - **Sleep: 1 μA**
  - **Hibernate: 600 nA**
- **Single-Wire HDQ Serial Interface**
- **Packaging: 8-LEAD TSSOP**

DESCRIPTION

The bq26221 is an advanced battery monitoring device designed to accurately measure the charge and discharge currents in rechargeable battery packs. Intended for pack integration, the bq26221 contains all the necessary functions to form the basis of a comprehensive battery capacity management system in portable applications such as cellular phones, PDAs, or other portable products.

The bq26221 works with the host controller in the portable system to implement the battery management system. The host controller is responsible for interpreting the bq26221 data and communicating meaningful battery data to the end-user or power management system.

This device provides 64 bytes of general-purpose flash memory, 8 bytes of ID ROM and 32 bytes of flash-backed RAM for data storage. The nonvolatile memory can maintain formatted battery monitor information, identification codes, warranty information, or other critical battery parameters during periods when the battery is temporarily shorted or deeply discharged.

PW PACKAGE
(TOP VIEW)

ORDERING INFORMATION†

T_A	PACKAGE	PART NUMBER	TOP MARKING
−20°C to 70°C	TSSOP	bq26221PW	**26221**

† PW (TSSOP−8) package is available taped and reeled. Add R suffix to device type (e.g. bq26221PWR) to order quantities of 2000 devices per reel for TSSOP-8.

ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)(1)

	bq26221	UNIT
Supply voltage (VCC with respect to GND)	−0.3 to +7.0	V
Input voltage, SRP and SRN, RBI, GPIO and BAT (all with respect to GND)	−0.3 V to V_{CC} + 0.3 V	
Input voltage, HDQ (with respect to GND)	−0.3 to +7.0	
Output current (GPIO)	5	mA
Output current (HDQ)	5	
Operating free-air temperature range, T_A	−20°C to 70°C	°C
Storage temperature range, T_{stg}	− 65°C to 150°C	
Lead temperature (soldering, 10 s)	300	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.8	4.5	V
$V_{(POR)}$	Power-on reset voltage	1.9	2.45	V
T_A	Operating ambient temperature	−20	70	°C

dc electrical characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(OP)}$	Supply current	V_{CC} = 4.3 V, flash programming not active		30	37	µA
$I_{(SLEEP)}$	Sleep current	V_{CC} = 4.3 V, flash programming not active		1	5	µA
$I_{(HIBERNATE)}$	Hibernate current	0 < V_{CC} < V_{POR}			600	nA
$I_{CC(PROG)}$	Flash programming supply current	V_{CC} = 5.5		21	30	mA
$I_{CC(ERASE)}$	Flash erase supply current	V_{CC} = 5.5		21	30	mA
$I_{(RBI)}$	Register back-up current	RBI pin only, 1.2 V< V_{CC} < $V_{(POR)}$			25	nA
I_{OL}	Digital output low sink current, GPIO and HDQ pins	VOL = 0.4 V			1	mA
V_{IL}	Digital input low, GPIO and HDQ pins				0.7	V
V_{IH}	Digital input high, GPIO and HDQ pins	V_{CC} < 4.2 V	1.7			V
		V_{CC} > 4.2 V	1.9			V
R_{BAT}	BAT input impedance		10			MΩ
R_{SR}	SRP, SRN input impedance	0.2 V < ($V_{(SRP)}$ − $V_{(SRN)}$) < V_{CC}	10			MΩ

timer characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$E_{(TMR)}$	Timer accuracy error		−4%		4%	

temperature register characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(RES)}$	Reported temperature resolution				0.25		°K
$E_{(T)}$	Reported temperature accuracy	BQ26221PW	TSSOP package	−4		4	°K

voltage ADC specification, over recommended operating temperature and supply voltage, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Least significant bit (LSB)(1)	2.6 V ≤ VBAT ≤ 4.5 V		2.44		mV
Integral nonlinearity (INL)	2.6 V ≤ VBAT ≤ 4.5 V, Vcc=VBAT	−4		+4	LSB
Differential nonlinearity (DNL)	2.6 V ≤ VBAT ≤ 4.5 V, Vcc=VBAT	−1		+1	LSB
Offset error	2.6 V ≤ VBAT ≤ 4.5 V, Vcc=VBAT	−3		+14	LSB
Maximum error	2.6 V ≤ VBAT ≤ 4.5 V, Vcc=VBAT	−9		+15	LSB

NOTE 1. For a more detailed explantion of parameters refer to the application note, *Understanding Data Converters*, TI Literature No. SLAA013.

VFC characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(SR)}$	Input voltage $V_{SRP} - V_{SRN}$		−100		100	mV
$G_{(VFC)}$	Charge/discharge gain	Temperature = 25 °C, V_{CC} = 3.6	90.0	93.5	97.0	Hz/V
$G_{(VCC)}$	Supply voltage gain coefficient	−100 mV < ($V_{(SRP)} - V_{(SRN)}$) < 100 mV		0.5		%/V
$G_{(TCO)}$	Temperature gain coefficient			0.005		%/°C
INL	Integrated nonlinearity	−100 mV < ($V_{(SRP)} - V_{(SRN)}$) < 100 mV		0.2%	0.5%	
$V_{(COS)}$	Auto compensated offset	2.8 V ≤ V_{CC} ≤ 4.2 V	−20	−1	20	µV

flash memory characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention				5	Years
	Flash programming write-cycles		10,000			Cycles
$t_{(BYTEPROG)}$	Byte programming time				90	µs
$t_{(BLCKPROG)}$	RAM-to-flash block programming time	60 µs + 30 µs/byte			1020	
$t_{(BLKERASE)}$	Block-erase time	60 µs + 30 µs/byte			1020	

standard serial communication (HDQ) timing specification over recommended operating temperature and supply voltage (unless otherwise noted). See Figures 1 and 2.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(B)}$	Break timing		190			µs
$T_{(BR)}$	Break recovery		40			
$T_{(CYCH)}$	Host bit window		190			
$T_{(HW1)}$	Host sends 1		0.5		50	
$T_{(HW0)}$	Host sends 0		92		145	
$T_{(RSPS)}$	bq26221 to host response		190		320	
$T_{(CYCB)}$	bq26221 bit window		190		250	
$T_{(start-detect)}$	(1)		5			ns
$T_{(DW1)}$	bq26221, sends 1		32		50	µs
$T_{(DW0)}$	bq26221, sends 0		80		145	

NOTE 1. The HDQ engine of the bq26221 interpret a 5 ns or longer glitch on HDQ as a bit start. A sufficient number of glitches at 5 ns or longer could result in incorrect data being written to the device. The HDQ line should be properly deglitched to ensure that this does not occur.

PARAMETER MEASUREMENT INFORMATION

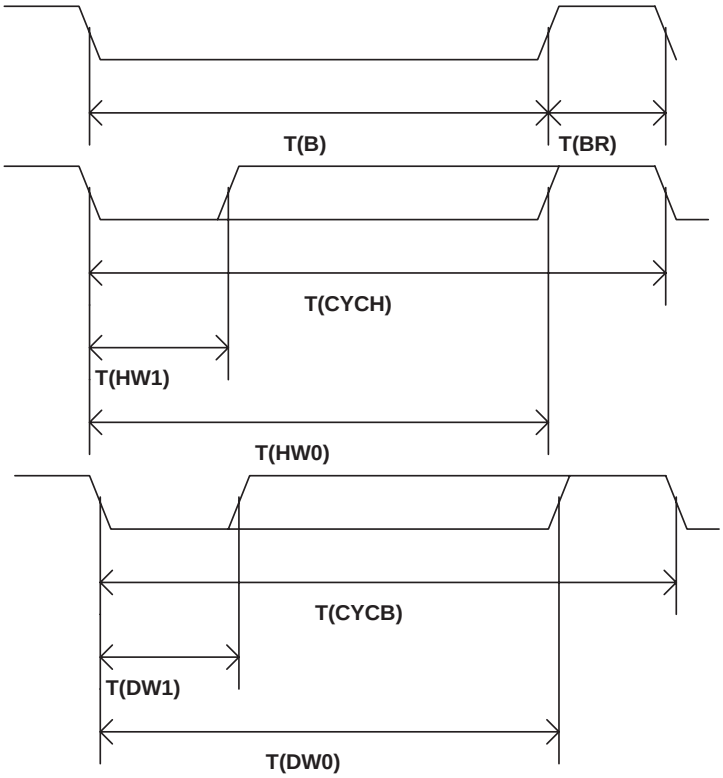


Figure 1. HDQ Timing Diagram

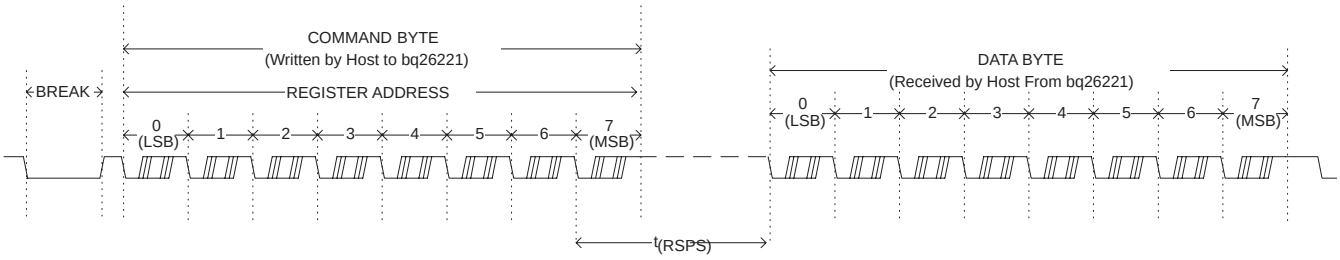
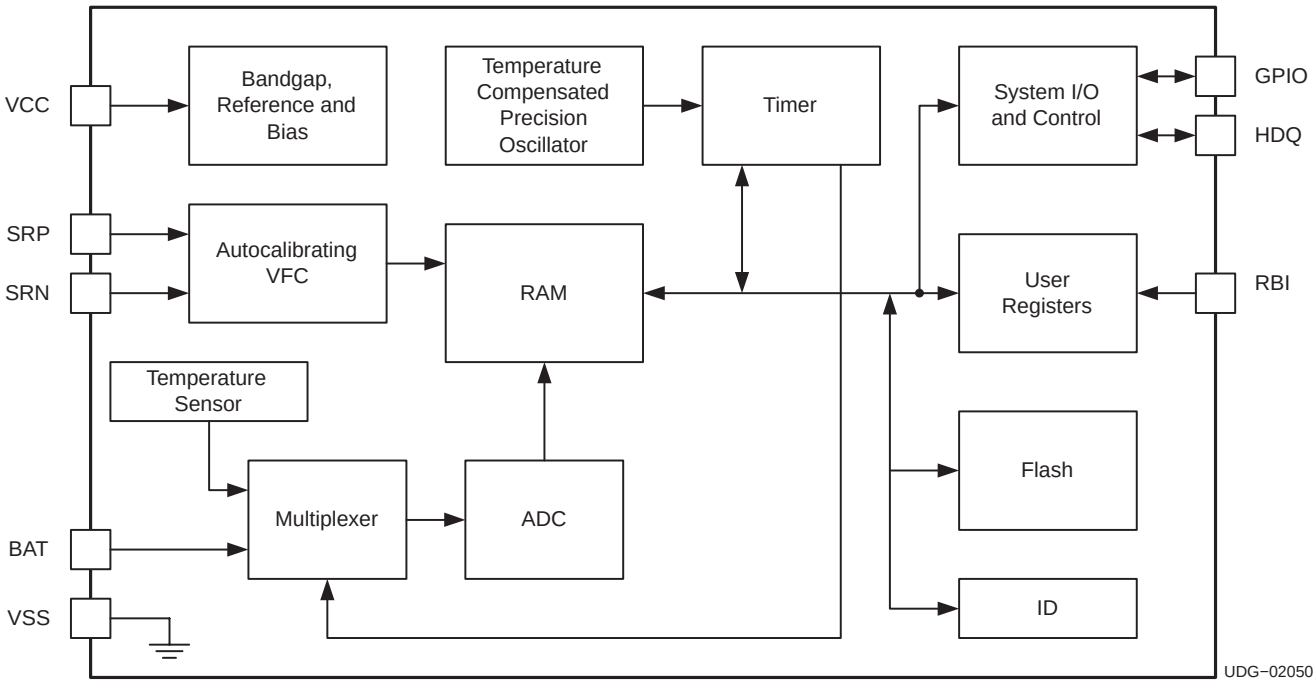


Figure 2. Typical Communication with the bq26221

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	No.		
BAT	5	I	Battery voltage sense input. This pin is used for sensing and measuring the battery voltage.
RBI	1	I	Register backup input. The RBI input pin is used with a storage capacitor or external supply to provide backup potential to the internal RAM and registers while V_{CC} is < $V_{(POR)}$.
GPIO	8	I/O	General-purpose input/output pin. GPIO is a general-purpose programmable input or output port whose state is controlled via the HDQ serial communications interface.
HDQ	4	I/O	Single-wire HDQ interface. HDQ is a single-wire serial communications interface port. This bidirectional input/output communicates the register information to the host.
SRN	6	I	Current sense input 2. The bq26221 interprets charge and discharge activity by monitoring and integrating the voltage drop, V_{SR}, across pins SRP and SRN. The SRN input connects to the sense resistor and the negative terminal of the pack. $V_{SRP} < V_{SRN}$ indicates discharge, and $V_{SRP} > V_{SRN}$ indicates charge.
SRP	7	I	Current sense input 1. The bq26221 interprets charge and discharge activity by monitoring and integrating the voltage drop, V_{SR}, across pins SRP and SRN. The SRP input connects to the sense resistor and the negative terminal of the battery. $V_{SRP} < V_{SRN}$ indicates discharge, and $V_{SRP} > V_{SRN}$ indicates charge.
VCC	2	I	Supply voltage
VSS	3	−	Ground

APPLICATION INFORMATION

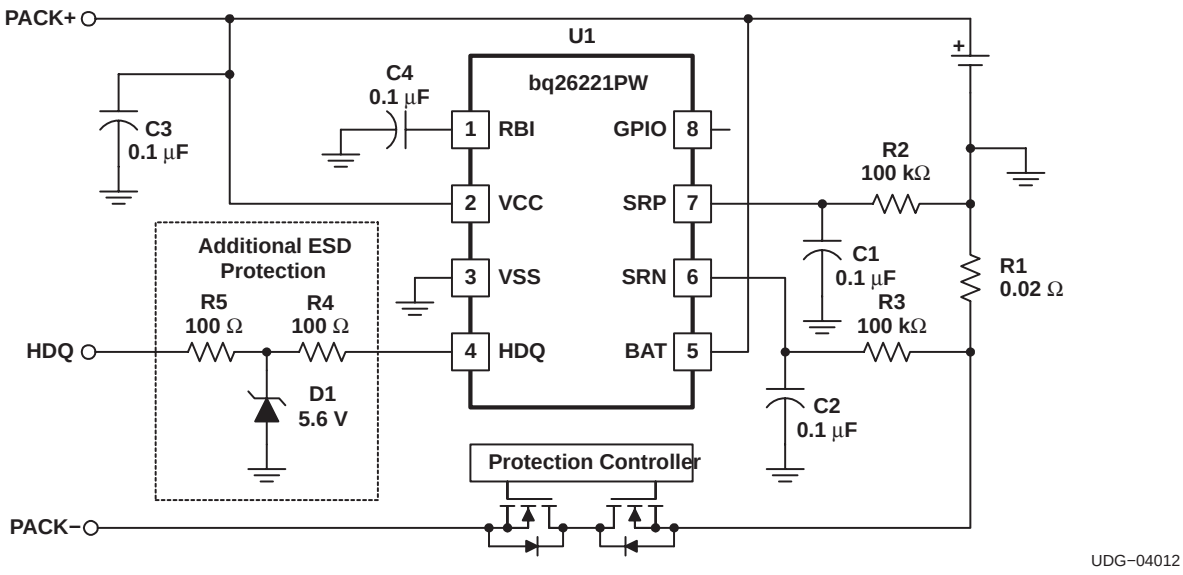


Figure 3. Typical Application Circuit for a Single-Cell Li-Ion Application

functional description

The bq26221 measures the voltage drop across a low-value series current-sense resistor between the SRP and SRN pins using a voltage-to-frequency converter. The cell voltage is sensed between the BAT and VSS pins. All data is placed into various internal counter and timer registers. Using information from the bq26221, the system host can determine the battery state-of-charge, estimate self discharge, and calculate the average charge and discharge currents. During pack storage periods, the use of an internal temperature sensor doubles the self-discharge count rate every 10°C above 25°C. The VFC offset is automatically compensated for in the charge and discharge counter registers.

Access to the registers and control of the bq26221 is accomplished through a single-wire interface through a register mapped command protocol. This protocol includes placing the device in the low-power mode, hardware-register reset, programming flash from RAM, and transferring flash data to RAM.

The bq26221 can operate directly from a single Li-Ion cell as long as V_{CC} is between 2.8 V and 4.5 V.

APPLICATION INFORMATION

charge and discharge count operation

Table 1 shows the main counters and registers of the bq26221.

The bq26221 accumulates charge and discharge counts into two count registers, the charge count register (CCR) and the discharge count register (DCR). Charge and discharge counts are generated by sensing the voltage difference between SRP and SRN. The CCR or DCR independently counts, depending on the signal between pins SRP and SRN.

During discharge, the DCR and the discharge time counter (DTC) are active. If $(V_{(SRP)} - V_{(SRN)})$ is less than 0, (indicating a discharge activity), the DCR counts at a rate equivalent to one count per 3.0 μVH, and the DTC counts at a rate of 1.138 counts per second (4096 counts = 1 hour). For example, if no rollover of the DTC register is incipient, a negative 24.42-mV signal produces 8000 DCR counts and 4096 DTC counts each hour. The amount of charge removed from the battery is easily calculated.

During charge, the CCR and the charge time counter (CTC) are active. If $(V_{(SRP)} - V_{(SRN)})$ is greater than 0, (indicating a charge), the CCR counts at a rate equivalent to one count per 3.0 μVH, and the CTC counts at a rate of 1.138 counts per seconds. In this case a 24.42-mV signal produces 8000 CCR counts and 4096 CTC counts (assuming no rollover) each hour.

The DTC and the CTC are 16-bit registers, with roll over beyond FFFFH. If a rollover occurs, the corresponding bit in the MODE register is set, and the counter increments at 1/256 of the normal rate (16 counts per hour). While in normal operation, the internal RAM and flash registers of the bq26221 may be accessed over the HDQ pin.

For self-discharge calculation, the self-discharge count register (SCR) counts at a rate of one count every hour at a nominal 25°C. The SCR count rate doubles approximately every 10°C up to 60°C. The SCR count rate is halved every 10°C below 25°C down to 0°C. The value in SCR is useful in estimating the battery self-discharge based on capacity and storage temperature conditions.

Table 4 shows the bq26221 register memory map. The remaining memory can store user-specific information such as chemistry, serial number, and manufacturing date.

sleep mode operation

The bq26221 begins low-power operation in response to the host issuing the sleep command. Before entering the low-power state, the host processor writes the command to transfer the registers to flash. After the sleep command is sent and the charge/discharge activity is less than the value indicated by the WOE bits shown in Table 2, the chip clock is powered down and data acquisitions functions cease except for self-discharge detection. During device sleep the bq26221 periodically wakes briefly to maintain the self-discharge registers. The bq26221 wakes on either a low-to-high or high-to-low transition on the HDQ pin.

Table 3 shows which registers are active during normal operation, sleep, and hibernate.

Table 1. bq26221 Counters

NAME	DESCRIPTION	RANGE	RAM SIZE (BITS)
DCR	Discharge count register	$(V_{(SRP)} - V_{(SRN)})$ < VSS (Max. =−100 mV) 3.0 μV/LSB	16
CCR	Charge count register	$(V_{(SRP)} - V_{(SRN)})$ > VSS (Max. = 100 mV) 3.0 μV/LSB	16
SCR	Self-discharge count register	1 count/hour at 25°C	16
DTC	Discharge time counter	1 count/0.8789 s (default) 1 count/225 s if STD is set	16
CTC	Charge time counter	1 count/0.8789 s (default) 1 count/225 s if STC is set	16

APPLICATION INFORMATION

Table 2. WOE Thresholds

$WOE_{3–1}$ (HEX)	V_{WOE} (mV)
0h	n/a
1h	3.516
2h	1.758
3h	1.172
4h	0.879
5h	0.703
6h	0.586
7h	0.502

Table 3. Operational States

MODE	ACTIVE REGISTERS
Normal	CCR, DCR, CTC, DTC, SDR
Sleep	SDR
Hibernate	No active registers

hibernate mode operation

The bq26221 enters hibernate mode when Vcc drops below the POR threshold, $V_{(POR)}$. In this mode, the bq26221 draws current from the RBI pin to maintain RAM data. The bq26221 exits hibernate mode only when Vcc is raised above the POR threshold.

current sense offset calibration and compensation

The bq26221 automatically and continuously compensates for $V_{(SRP)} - V_{(SRN)}$ offset. No host calibration or compensation is required.

gas gauge control registers

The host maintains the charge and discharge and the self-discharge count registers (CCR, CTC, DCR, DTC, and SCR). To facilitate this maintenance, the bq26221 CLR register resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq26221 completes the reset, the corresponding bit in the CLR register is automatically reset to 0. Clearing the DTC or CTC registers clears the MODE register bits STC/STD and sets the CTC/DTC count rates to the default value of 1.138 counts per second.

device temperature measurement

The bq26221 reports die temperature in units of °K through register pair TMPH−TMPL. Refer to the TMP register description for more details.

APPLICATION INFORMATION

battery voltage measurement

The bq26221 senses the battery voltage on the BAT pin and reports it through register pair BATH−BATL. The BATH (address = 0x72 – bits 0 through 2) and the BATL low-byte register (address = 0x71) contain the result of ADC conversion on the battery voltage. The voltage is expressed in an 11-bit binary format with an LSB step size of 2.44 mV. Bit 2 of BATH register represents the MSB and bit 0 of the BATL represent the LSB. The full-scale voltage for this measurement is 5 V and is optimized for direct sensing in single-cell Li-Ion or Li-pol applications (see Figure 3).

Note that Bits 3 through 7 of the BATH register store the offset information for the voltage ADC. The most significant bit is the sign-bit followed by 4 bits of offset data.

Also note that LSB gain correction factor, in μV, is stored in address 0x79 (byte 1 of the ID ROM) in 2's complement. The host is responsible for applying the LSB gain correction factor and offset to the ADC measurements.

Correct V_{BAT} = V_{BAT} × (2.44 + LSB correction factor) − offset

example 1: (If real LSB = + 2.45mV and offset = +80 mV)

in address 0x79 ⇒ `0000 1010` (in binary) 2's complement

in BATH (0x72) ⇒ `0101 0XXX` (in binary) signed magnitude

To calculate the correct V_{BAT}:

LSB correction factor = +10 μV = +0.01 mV

offset = +10 × 8 mV = 80 mV

Correct V_{BAT} (in mV) = V_{BAT} × (2.44 + 0.01) − 80

example 2: (If real LSB = +2.43 mV and offset = −80 mV

in address 0x79 ⇒ `1111 0110` (in binary), 2's complement

in BATH (0x72) ⇒ `1101 0XXX` (in binary), signed magnitude

To calculate the correct V_{BAT}:

LSB correction factor = −10 μV= −0.01 mV

offset = −10 × 8 mV = −80 mV

Correct V_{BAT} (in mV) = V_{BAT} × (2.44 − 0.01) − (−80)

APPLICATION INFORMATION

register interface

Information is exchanged between host system and the bq26221 through the data-register interface. See Table 4 below. The register set consists of a 122-location address space of 8-bit bytes segmented into

- 8 bytes of factory programmed ID ROM
- 32 bytes of flash shadowed RAM
- 64 bytes of general purpose flash
- 18 special function registers

Table 4. Memory Map

HDQ ADDRESS	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x78−0x7F	IDROM	8 bytes of factory-programmed ROM and gain correction factor for BATH and BATL							
0x73−0x77	−	Reserved							
0x72	BATH	BV−SIGN	BVOS3	BVOS2	BVOS1	BVOS0	Battery voltage (bits 8 through 10)		
0x71	BATL	Battery voltage (bits 0 through 7)							
0x70	FPA	Flash program address byte							
0x6F	FPD	Flash program data byte							
0x6E	DCRH	Discharge count register-high byte							
0x6D	DCRL	Discharge count register-low byte							
0x6C	CCRH	Charge count register-high byte							
0x6B	CCRL	Charge count register-low byte							
0x6A	SCRH	Self-discharge count register-high byte							
0x69	SCRL	Self−discharge count register-low byte							
0x68	DTCH	Discharge timer counter register-high byte							
0x67	DTCL	Discharge timer count register-low byte							
0x66	CTCH	Charge timer counter register-high byte							
0x65	CTCL	Charge timer counter register-low byte							
0x64	MODE	GPIEN	STAT	STC	STD	WOE2	WOE1	WOE0	POR
0x63	CLR	RSVD	RSVD	RSVD	CTC	DTC	SCR	CCR	DCR
0x62	FCMD	Flash/control command register							
0x61	TEMPH	Temperature-high byte (bits 0 through 2 only, other bits are reserved)							
0x60	TEMPL	Temperature-low byte							
0x40−0x5F	Flash	Page 2, 32 bytes of flash							
0x20−0x3F	Flash	Page 1, 32 bytes of flash							
0x00−0x1F	RAM/flash	Page 0, 32 bytes of flash shadowed RAM							

APPLICATION INFORMATION

memory

ID ROM

Locations 0x7F through 0x78 contain the factory programmed ID ROM and also the LSB gain correction factor for the voltage analog to digital converter. The format for this register is described in Table 5.

Table 5. ID ROM Command Code Summary

BYTE	RAM LOCATION	INFORMATION
7	0x7F	Device code 0x22
6	0x7E	0x00
5	0x7D	Random
4	0x7C	Random
3	0x7B	Random
2	0x7A	Random
1	0x79	Gain correction factor
0	0x78	Random

NOTE: For additional information please contact Texas Instruments.

flash-shadowed RAM

The host system has direct access to read and modify 32 bytes of RAM. These 32 bytes are shadowed by 32 bytes of flash to provide nonvolatile storage of battery conditions. The information stored in RAM is transferred to flash, and the information stored in flash is transferred to RAM by writing a single command into the flash command register (FCMD). When a power-on-reset occurs, page 0 of flash is transferred to RAM. For more details, refer to the *flash command register* section.

user-flash memory

In addition to the flash-shadowed RAM, the bq26221 has 64 bytes of user-flash. The user-flash can store specific battery pack parameters, such as charge per VFC pulse, battery chemistry, and self-discharge rates.

flash programming

The two banks of direct user-flash are programmed one byte at a time, but the single bank of flash-shadowed RAM can be programmed one page at a time or by writing the RAM-to-flash transfer code into the flash command register (FCMD). This programming is performed by writing the desired code into the flash command register, FCMD (address 0x62), the host may transfer data between flash and RAM, page erase the flash or place the device into the low power mode. For more details, refer to the *flash command register* section. Summaries of the flash command codes are shown in Table 6.

Table 6. Flash Command Code Summary

COMMAND CODE (HEX)	DESCRIPTION
0x0F	Program byte
0x40	Erase page 0 flash
0x41	Erase page 1 flash
0x42	Erase page 2 flash
0x45	Transfer page 0 RAM to page 0 flash
0x48	Transfer page 0 flash to page 0 RAM
0xF6	Power down

APPLICATION INFORMATION

single-byte programming

To program an individual byte in flash, the byte of data is first written into the FPD register while the address to be programmed is written into the FPA register. The program byte command, 0x0F, is then written to the FCMD. The result of this sequence is that the contents of the FPD register is logically ANDed with the contents of the flash address pointed to by the FPA register.

RAM-to-flash transfer

The content of the flash that shadows the user RAM is logically ANDed to the RAM contents when the RAM-to-flash transfer command is sent. If new data is to be written over old data, then it is necessary to first erase the flash page that is being updated and restore all necessary data.

communicating with the bq26221

The bq26221 includes a single-wire HDQ serial data interface. Host processors, configured for either polled or interrupt processing, use the interface to access various bq26221 registers. The HDQ pin requires an external pull-up resistor. The interface uses a command-based protocol, where the host processor sends a command byte to the bq26221. The command directs the bq26221 either to store the next eight bits of data received to a register specified by the command byte, or, to output the eight bits of data from a register specified by the command byte.

The communication protocol is asynchronous return-to-one and is referenced to VSS. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5 Kbits/s. The least-significant bit of a command or data byte is transmitted first. Data input from the bq26221 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART, (universal asynchronous receiver transmitter), also communicates with the bq26221.

If a communication time out occurs (for example, if the host waits longer than $t_{(CYCB)}$ for the bq26221 to respond or if this is the first access command), then a BREAK should be sent by the host. The host may then resend the command. The bq26221 detects a BREAK when the HDQ pin is driven to a logic-low state for a time $t_{(B)}$ or greater. The HDQ pin then returns to its normal ready-high logic state for a time $t_{(BR)}$.The bq26221 is then ready for a command from the host processor.

The return-to-one data-bit frame consists of three distinct sections:

1. The first section starts the transmission by either the host or the bq26221 taking the HDQ pin to a logic-low state for a period equal to $t_{(HW1)}$ or $t_{(DW1)}$.
2. The next section is the actual data transmission, where the data should be valid by a period equal to $t_{(HW1)}$ or $t_{(DW1)}$, after the negative edge that starts communication. The data should be held for $t_{(HW0)}$ and $t_{(DW0)}$ periods to allow the host or bq26221 to sample the data bit.
3. The final section stops the transmission by returning the HDQ pin to a logic-high state by at least a period equal to $t_{(DW0)}$ or $t_{(HW0)}$ after the negative edge used to start communication. The final logic-high state should be held until a period equal to $t_{(CYCH)}$ or $t_{(CYCB)}$, to allow time to ensure that the bit transmission ceased properly.

APPLICATION INFORMATION

The serial communication timing specification and illustration sections give the timings for data and break communication. Communication with the bq26221 always occurs with the least significant bit being transmitted first. Figure 4 shows an example of a communication sequence to read the bq26221 DCRH register.

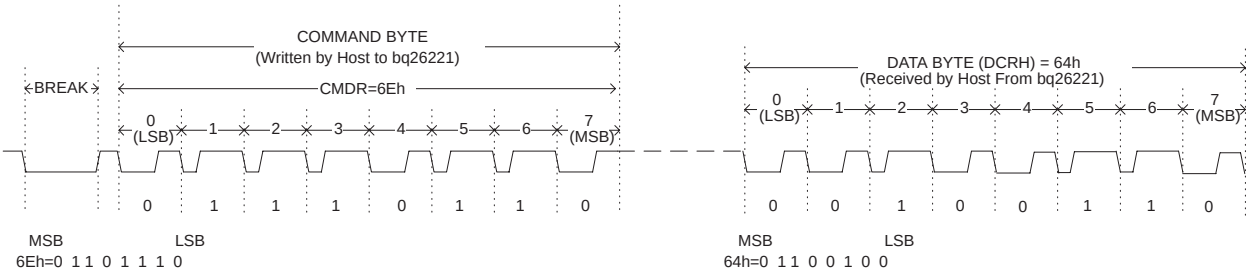


Figure 4. bq26221 Communication Sequence

command byte

The command byte of the bq26221 consists of eight contiguous valid command bits. The command byte contains two fields: W/R Command and address. The W/R bit of the command register determines whether the command is a read or a write command while the address field containing bit AD6−AD0 indicates the address to be read or written. The command byte values are shown in Table 7.

Table 7. Command Byte Values

COMMAND BYTE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
W/R	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 8. Command Byte Definitions

W/R	Indicates whether the command byte is a read or write command. A 1 indicates a write command and that the following eight bits should be written to the register specified by the address field of the command byte, while a 0 indicates that the command is a read. On a read command, the bq26221 outputs the requested register contents specified by the address field portion of the command byte.
AD6−AD0	The seven bits labeled AD6−AD0 containing the address portion of the register to be accessed.

bq26221 registers

register maintenance

The host system is responsible for register maintenance. (See Table 4.) To facilitate this maintenance, the bq26221 clear register (CLR) resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq26221 completes the reset, the corresponding bit in the CLR register automatically resets to 0, saving the host an extra write/read cycle. Clearing the DTC register clears the STD bit and sets the DTC count rate to the default value of one count per 0.8789 s. Clearing the CTC register clears the STC bit and sets the CTC count rate to the default value of one count per 0.8789 s.

APPLICATION INFORMATION

register descriptions

battery voltage offset registers (BATH)

Bits 3 through 7 of the BATH register (address = 0x72) store the offset information for the voltage ADC. The most significant bit is the sign bit followed by 4 bits of offset data. Each count of offset represents 8 mV. The host is responsible for subtracting the offset for the measurement from the uncorrected value found in BATH and BATL registers. This is a signed magnitude number with Bit 7 being the sign bit. A 1 in Bit 7 means that the number is negative.

battery voltage registers (BATH/BATL)

The BATH (address = 0x72 – bits 0 through 2) and the BATL low-byte register (address = 0x71) contain the result of ADC conversion on the battery voltage. The voltage is expressed in an 11-bit binary format with an LSB step size of 2.44 mV. Bit 3 of BATH register represents the MSB and bit 0 of the BATL represent the LSB.

flash program address register (FPA)

The FPA byte register (address = 0x70) points to the flash address location that is programmed when the program flash command is issued. This byte is used with the FPD and FCMD register to program an individual byte in flash memory.

flash program data register (FPD)

The FPD byte register (address = 0x6F) contains the data to be programmed into the flash address location pointed to by the contents of the FPA register. When the program flash command is issued, the contents of the FPD register are ANDed with the contents of the byte pointed to by the FPA and then stored into that location.

discharge count registers (DCRH/DCRL)

The DCRH high-byte register (address = 0x6E) and the DCRL low-byte register (address = 0x6D) contain the count of the discharge, and are incremented whenever $V_{SR} < V_{SS}$ These registers continue to count beyond FFFFH, so proper register maintenance by the host system is necessary. The CLR register forces the reset of both the DCRH and DCRL to zero.

charge count registers (CCRH/CCRL)

The CCRH high-byte register (address = 0x6C) and the CCRL low-byte register (address = 0x6B) contain the count of the charge, and are incremented whenever $V_{SR} > V_{SS}$. These registers continue to count beyond FFFFH, so proper register maintenance should be done by the host system. The CLR register forces the reset of both the CCRH and CCRL to zero.

self-discharge count registers (SCRH/SCRL)

The SCRH high-byte register (address = 0x6A) and the SCRL low-byte register (address = 0x69) contain the self-discharge count. This register is continually updated in both the normal operating and sleep modes of the bq26221. The counts in these registers are incremented based on time and temperature. The SCR counts at a rate of one count per hour at 20°C to 30°C. The count rate doubles every 10°C up to a maximum of 16 counts/hour at temperatures above 60°C. The count rate halves every 10°C below 20°C to 30°C to a minimum of one count/8 hours at temperature below 0°C. These registers continue to count beyond FFFFH, so proper register maintenance should be done by the host system. The CLR register forces the reset of both the SCRH and SCRL to zero. During device sleep the bq26221 periodically wake for a brief amount of time to maintain the self-discharge registers.

APPLICATION INFORMATION

discharge time count registers (DTCH/DTCL)

The DTCH high-byte register (address = 0x68) and the DTCL low-byte register (address = 0x67) determine the length of time the $V_{SR} < V_{SS}$ indicating a discharge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the DTCH/DTCL register continues to count beyond FFFFH, the STD bit is set in the MODE/WOE register, indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour.

Note: If a second rollover occurs, STD is cleared. Access to the bq26221 should be timed to clear DTCH/DTCL more often than every 170 days. The CLR register forces the reset of both the DTCH and DTCL to zero.

charge-time count registers (CTCH/CTCL)

The CTCH high-byte register (address = 0x66) and the CTCL low-byte register (address = 0x65) determine the length of time the $V_{SR} > V_{SS}$, indicating a charge activity. The counts in these registers are incremented at a rate of 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond FFFFH, the STC bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour.

Note: If a second rollover occurs, STC is cleared. Access to the bq26221 should be timed to clear CTCH/CTCL more often than every 170 days. The CLR register forces the reset of both the CTCH and CTCL to zero.

mode register (MODE)

The MODE register (address 0x64) contains the GPIEN, STAT, STC, STD, POR and wake-up enable information as described in Table 9.

Table 9. MODE Register Values

MODE BITS							
7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
GPIEN	STAT	STC	STD	WOE2	WOE1	WOE0	POR

Table 10. MODE Register Definitions

GPIEN	GPIEN bit (bit 7) sets the state of the GPIO pin. A 1 configures the GPIO pin as input, while a 0 configures the GPIO pin as open-drain output. This bit is set to 0 on power-on-reset.
STAT	STAT bit (bit 6) sets the state of the open drain output of the GPIO pin (when configured as output by bit 7). A 1 turns off the open drain output while a 0 turns the output on. This bit is set to 1 on power-on-reset.
STC & STD	The slow time charge (STC) and slow time discharge (STD) flags indicate if the CTC or DTC registers have rolled over beyond FFFFH. STC set to 1 indicates a CTC rollover; STD set to 1 indicates a DTC rollover.
WOE[2.0]	The wake-up output enable (WOE) bits (bits 3, 2 and 1) indicate the voltage level required between SRP and SRN so that the bq26221 enters sleep mode after a power down command is issued. Whenever $\lvert V_{SRP} - V_{SRN} \rvert < V_{WOE}$, the bq26221 enters sleep mode after the power down command has been issued. On bq26221 power-on-reset these bits are set to 1. Setting all of these bits to zero is valid, but result in immediate sleep. Refer to Table 3 for the various WOE values.
POR	POR bit (bit 0) indicates a power-on-reset has occurred. This bit is set when V_{CC} has gone below the POR level. This bit can be also set and cleared by the host, but has no functionality if set by host.

APPLICATION INFORMATION

clear register (CLR)

The bits in the CLR register (address 0x63) clear the DCR, CCR, SCR, DTC, and CTC registers, reset the bq26221 by forcing a power-on-reset and setting the state of the STAT pin as described in Table 11.

Table 11. CLR Register

CLR BITS							
7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
RSVD	RSVD	RSVD	CTC	DTC	SCR	CCR	DCR

Table 12. CLR Register Definitions

RSVD	RSVD bits (bits 5, 6 and 7) are reserved for future use and should be written to 0 by the host.
CTC	CTC bit (bit 4) clears the CTCH and CTCL registers and the STC bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the CTC bit is cleared. This bit is cleared on power-on-reset.
DTC	DTC bit (bit 3) clears the DTCH and DTCL registers and the STD bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the DTC bit is cleared. This bit is cleared on power-on-reset.
SCR	SCR bit (bit 2) clears both the SCRH and SCRL registers. Writing a 1 to this bit clears the SCRH and SCRL register. After these registers are cleared, the SCR bit is cleared. This bit is cleared on power-on-reset.
CCR	CCR bit (bit 1) clears both the CCRH and CCRL registers. Writing a 1 to this bit clears the CCRH and CCRL registers. After these registers are cleared, the CCR bit is cleared. This bit is cleared on power-on-reset.
DCR	DCR bit (bit 0) clears both the DCRH and DCRL registers. Writing a 1 to this bit clears the DCRH and DCRL registers. After these registers are cleared, the DCR bit is cleared. This bit is cleared on power-on-reset.

flash command register (FCMD)

The FCMD register (address 0x62) is the flash command register and programs a single flash byte-location, perform flash page erase, transfer RAM to flash and flash to RAM, enter sleep mode, and power-down. These functions are performed by writing the desired command code to the FCMD register. After the bq26221 has finished executing the issued command, the flash command register is cleared.

Table 13. FCMD Register Definitions

0x0F	Program byte command code. This code ANDs the contents of the FPD register with the contents of flash byte location pointed to by the contents of the FPA register.
0x40	Erase page 0 command code. This code erases all the bytes of flash from address 0x00 to 0x1F.
0x41	Erase page 1 command code. This code erases all the bytes of flash from address 0x20 to 0x3F.
0x42	Erase page 2 command code. This code erases all the bytes of flash from address 0x40 to 0x5F.
0x45	RAM-to-flash transfer code. This code programs the contents of the RAM into Page 0 flash, addresses 0x00 though 0x1F.
0x48	Flash-to-RAM transfer code. This code copies the contents of the page 0 flash into RAM.
0xF6	Power-down code. This code places the bq26221 into the sleep mode when the conditions are met as indicated by the WOE bits in the MODE/WOE register. The part remains in sleep mode until a high-to-low or low-to-high transition occurs on the HDQ pin.

APPLICATION INFORMATION

temperature registers (TMPH, TMPL)

The TMPH (address 0x61) and the TMPL registers (address 0x60) reports die temperature in hex format in units of 0.25°K.The temperature is reported as 11 bits of data, using all 8 bits of the TMPL low register and the 3 bits of the TMPH register. The temperature should be read as the concatenation of TMPH [2:0] and TMPL [7:0], 0.25°K/LSB. The 5 MSBs of TMPH, TMPH [7:3], are cleared on POR and are reserved. The 5 bits should also be masked off when reading the temperature, to ensure that incorrect data is not used when calculating the temperature.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ26221PW	ACTIVE	TSSOP	PW	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ26221PWG4	ACTIVE	TSSOP	PW	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ26221PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ26221PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

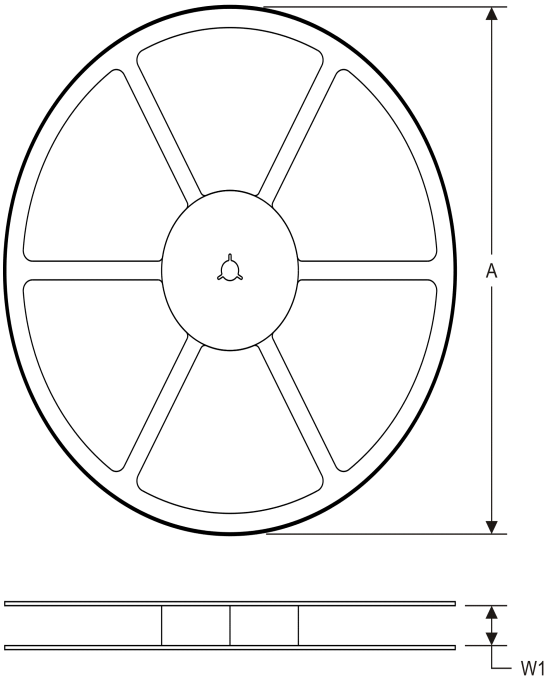
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

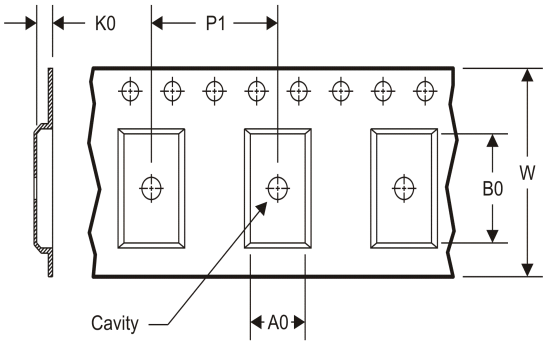
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



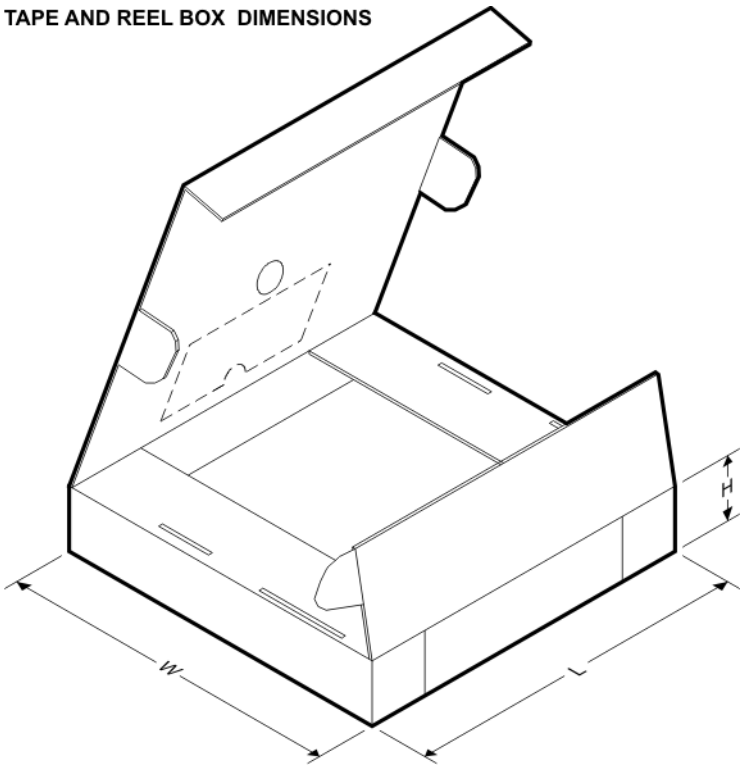
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ26221PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

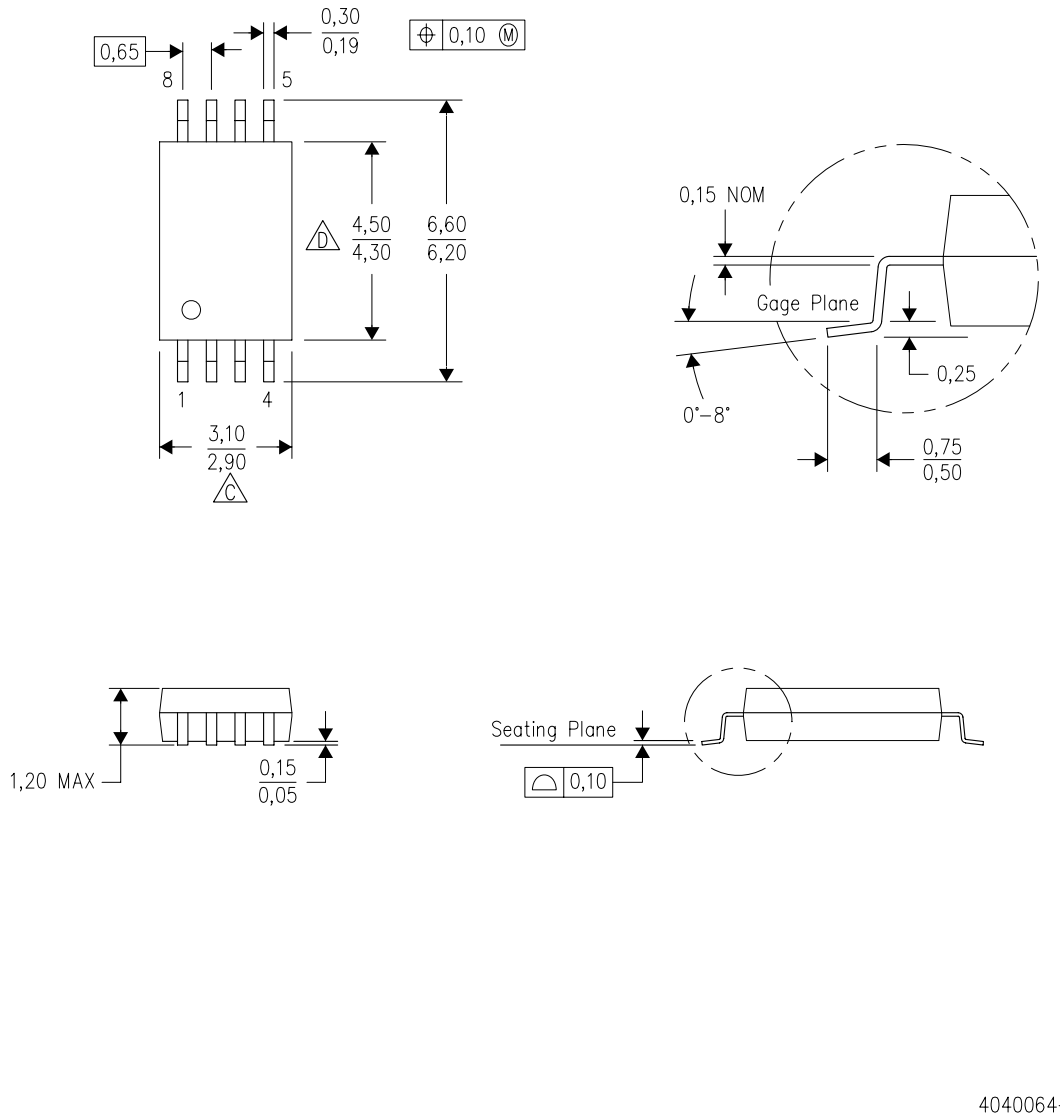
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ26221PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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