

Over-Voltage and Over-Current Charger Front-end Protection IC With Integrated Charging FET

Check for Samples: [bq24350](#) [bq24352](#)

FEATURES

- **Robust Protection**
 - Input Over-Voltage Protection
 - Input Over-Current Protection
 - Accurate Battery Over-Voltage Protection
 - Thermal Shutdown
 - Output Short-Circuit Protection
- **Integrated Charging FET**
- **LDO Mode Operation**
- **Current Limited Power Supply for Host Controller**

- **Soft-Start to Prevent Inrush Currents**
- **Soft-Stop to Prevent Voltage Spikes**
- **30V Maximum Input Voltage**
- **Supports Up to 1A Load Current**
- **Small 2mm × 2mm 8pin SON Package**

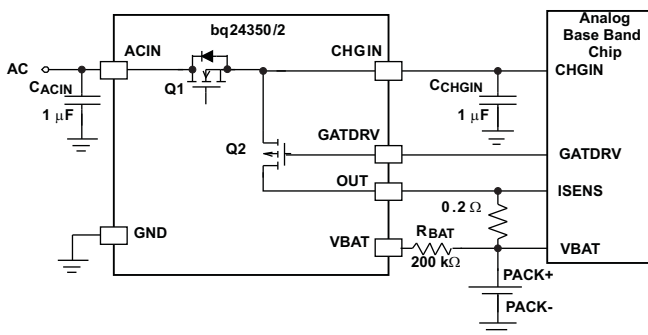
APPLICATIONS

- **Mobile Phones**
- **Low-Power Handheld Devices**

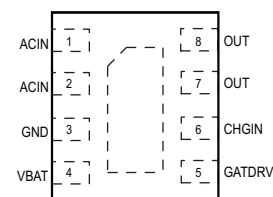
DESCRIPTION

The bq24350/2 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage and the battery voltage. In case of an input over-voltage condition, the IC will turn off the internal power FET after a blanking time. If the battery voltage rises to unsafe levels during charging process, power is removed from the system. If the input current exceeds the over current threshold for a limited time, the IC will turn off the output power. The integrated charging FET can regulate the charge voltage and current according to the control from the host. The device can also provide a voltage source with over voltage and over current protection for host controller.

TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

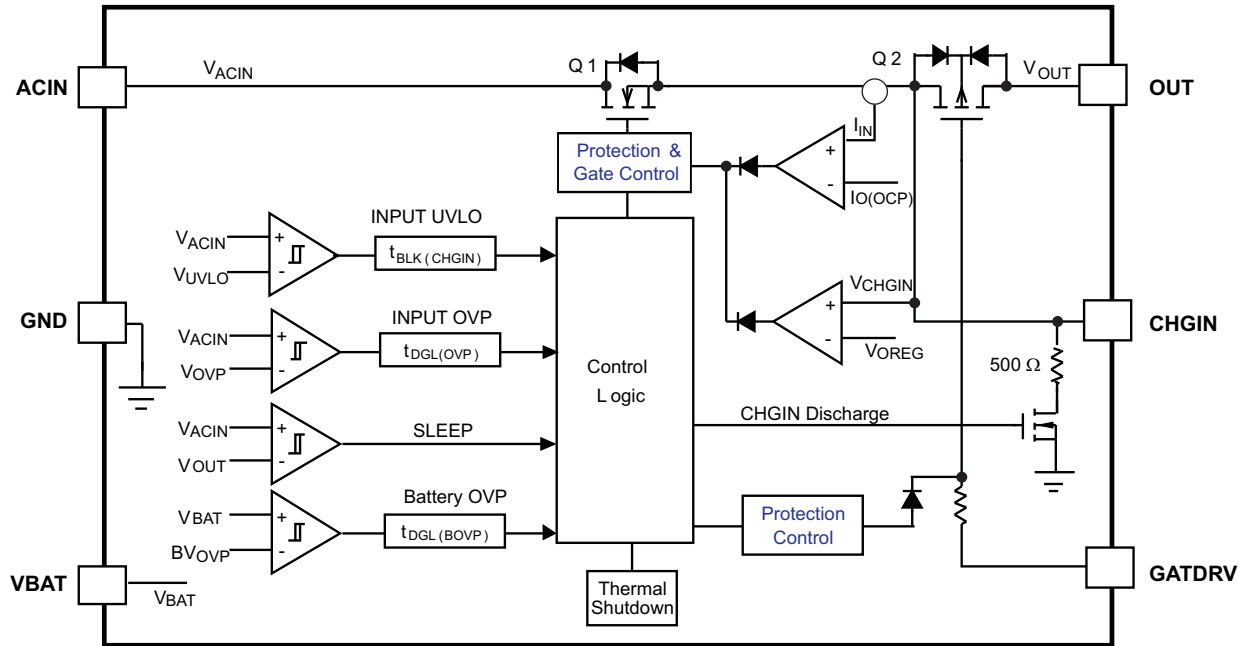
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED FUNCTION BLOCK DIAGRAM



PIN FUNCTIONS

PIN			
NAME	NUMBER	I/O	DESCRIPTION
ACIN	1,2	I	Power Supply Input, connect to an external DC supply. Connect an external 1µF ceramic capacitor (minimum) to GND.
OUT	7,8	O	Output terminal to the charging system.
VBAT	4	I	Battery voltage sense input. Connected to pack positive terminal through a resistor. Connected to ground if battery OVP function is not used.
GATDRV	5	I	P-FET gate drive input, connected to gate drive pin of the host charger controller
CHGIN	6	O	Output power pin for power input of host charger controller. Connect an external ceramic bypass capacitor (1.0µF minimum) to GND.
GND	3	–	Ground terminal
Thermal PAD			There is an internal electrical connection between the exposed thermal pad and the GND pin of the device. The thermal pad must be connected to the same potential as the GND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times.

ORDERING INFORMATION

PART NUMBER	MARKING	MEDIUM	QUANTITY	PACKAGE	INPUT OVP THRESHOLD
bq24350DSGR	OAJ	Tape and Reel	3000	2mm x 2mm SON	6.17 V
bq24350DSGT	OAJ	Tape and Reel	250	2mm x 2mm SON	6.17 V
bq24352DSGR	OCY	Tape and Reel	3000	2mm x 2mm SON	7.1 V
bq24352DSGT	OCY	Tape and Reel	250	2mm x 2mm SON	7.1 V

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNIT
Input voltage	ACIN (with respect to GND)	–0.3 V to 30 V
Output voltage	OUT, CHGIN (with respect to GND)	–0.3 V to 7V
Input voltage	VBAT, GATDRV (with respect to GND)	–0.3 V to 7 V
Input current	ACIN	–1.8 A ⁽²⁾ to 1.4 A
Junction temperature, T _J		–40°C to 150°C
Storage temperature, T _{STG}		–65°C to 150°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
- (2) Reverse current is specified for a maximum of 50 hours at T_J < 150°C.

PACKAGE DISSIPATION RATINGS

PACKAGE	PACKAGE DRAWING	R _{θJC}	R _{θJA}
SON-8	DSG	5°C/W	75°C/W

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNITS
V _{ACIN}	ACIN voltage range	4.4	15	V
I _{ACIN}	Current, ACIN pin		1	A
T _J	Junction Temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

Refer to the typical application circuit shown in [Figure 1](#). These specifications apply over ACIN=5V, T_J = -40~125°C, unless otherwise specified. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACIN						
V _{UVLO}	Under-voltage lock-out threshold	ACIN: 3V → 2V, ACIN falling	1.8	1.95	2.1	V
		ACIN: 2V → 3V, ACIN rising	2.5			
t _{BLK(CHGIN)}	Input power on blanking time	VACIN rising to CHGIN rising		10		ms
I _{DD}	Operating current	No load on OUT and CHGIN pin			500	μA
INPUT TO OUTPUT CHARACTERISTICS						
	On resistance from ACIN to OUT	I _{OUT} = 1.0A, ACIN=5V, GATDRV=0V		415	685	mΩ
	On resistance from ACIN to CHGIN	I _{CHGIN} = 1.0A, ACIN=5V, I _{OUT} =0A		250	495	mΩ
INPUT OVER-VOLTAGE PROTECTION (OVP)						
V _{OVP}	CHGIN voltage in LDO mode	ACIN=5.9V, GATDRV=CHGIN, I _{CHGIN} =0 to 1A.	5.33	5.5	5.66	V
V _{OVP}	Input OVP threshold, bq24350	VACIN rising	6	6.17	6.35	V
	Input OVP threshold, bq24352		6.9	7.1	7.3	
V _{HYS-OVP}	Input OVP recovery hysteresis, bq24350	VACIN: 7.5V → 5V	250	300	350	mV
	Input OVP recovery hysteresis, bq24352		100	150	200	
t _{DGL(OVP)}	Input OVP deglitch time	VACIN rising to CHGIN falling		256		μs
t _{REC(OVP)}	Input OVP recovery time	VACIN falling below V _{OVP} to CHGIN rising		8.2		ms
INPUT OVER CURRENT LIMITING AND PROTECTION (OCP)						
I _{O(OCP)}	OCP threshold		1.02	1.2	1.38	A
t _{DGL(OCP)}	OCP blanking time			8.2		ms
t _{REC(OCP)}	OCP recovery time			131		ms
BATTERY OVER-VOLTAGE PROTECTION						
BV _{OVP}	Battery OVP threshold	VBAT rising	4.3	4.35	4.4	V
V _{HYS-BOVP}	Battery OVP hysteresis	VBAT falling	200	250	300	mV
I _{VBAT}	VBAT pin leakage current	VBAT=4.25V, series connection of a 200kΩ resistor, T _J = 25°C			10	nA
t _{DGL(BOVP)}	Battery OVP deglitch time	VBAT rising to CHGIN falling		8.2		ms
t _{REC(BOVP)}	Battery OVP recovery time	VBAT falling below BV _{OVP} to CHGIN rising		131		ms
CHGIN						
V _{SEXT}	Sleep mode exit threshold and CHGIN turn on threshold, ACIN-VOUT	ACIN rising, VOUT = 4.2 V	24	90	160	mV
V _{SENTRY}	Sleep mode entry threshold and CHGIN turn off threshold, ACIN-VOUT	ACIN falling, VOUT = 4.2 V	10	55	105	mV
I _{DDSLP}	Sleep Mode supply current	OUT = 4.2 V, GATDRV = 4.2 V, ACIN = VSS			10	μA
R _{DIS}	CHGIN discharge resistor			500		Ω
	Leakage current from OUT to CHGIN	OUT = 4.2 V, GATDRV = 4.2 V, CHGIN = 0 V, ACIN = 0 V, T _J = 85°C			1	μA
INTEGRATED P-FET PARAMETERS						
V _t	Threshold Voltage, CHGIN-GATDRV.	CHGIN=5V, OUT=3.6V, I _{OUT} =10mA	500	680	800	mV
I _g	GATDRV pin leakage current			0.1	1	μA
I _{off}	Off state leakage current at OUT pin.	ACIN=5V, GATDRV=CHGIN, OUT=0V		1		μA
R _{onp}	On Resistance of P-FET (from CHGIN to OUT)	I _{OUT} = 1.0A, ACIN=5V, GATDRV=0V		165	225	mΩ
G _m	Forward Transconductance	ACIN=5V, I _{OUT} =5mA, GATDRV=3.5V		27		mA/V
C _g	Input capacitance at the GATDRV pin	CHGIN=GATDRV=5V		104		pF
THERMAL PROTECTION						
T _{J(OFF)}	Thermal shutdown threshold	Junction temperature rising	140	150	160	°C

ELECTRICAL CHARACTERISTICS (continued)

Refer to the typical application circuit shown in [Figure 1](#) . These specifications apply over ACIN=5V, $T_J = -40\sim 125^\circ\text{C}$, unless otherwise specified. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{J(\text{OFF-HYS})}$ Thermal shutdown hysteresis	Junction temperature falling		20		$^\circ\text{C}$

TYPICAL APPLICATION CIRCUIT

ACIN=5V, ICHARGE=1A, VBAT=4.2V

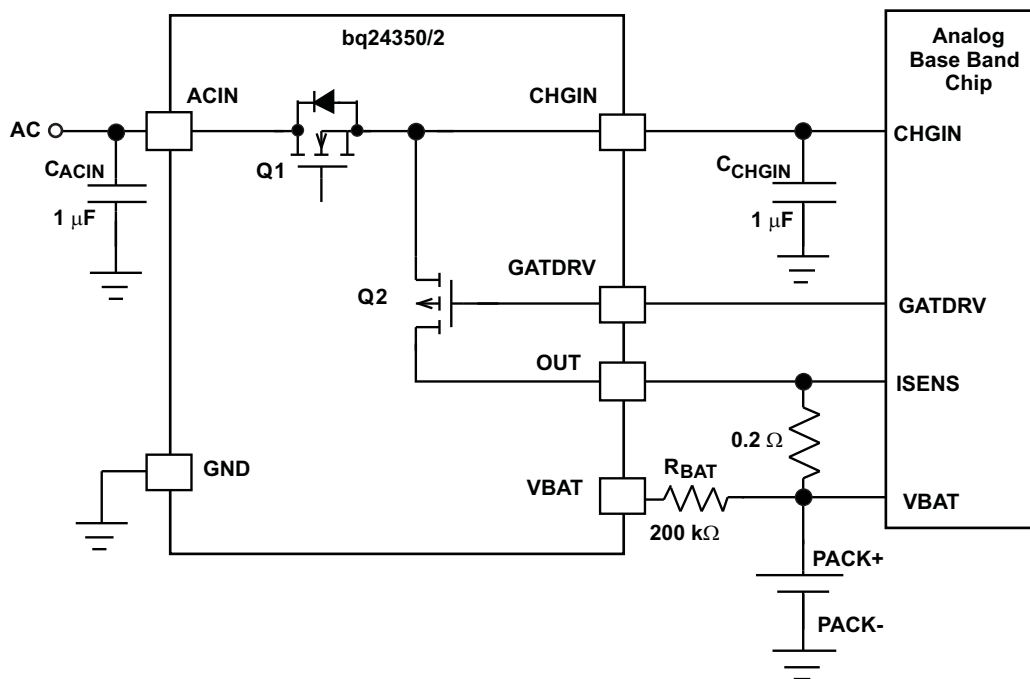


Figure 1. Host Controlled One-Cell Charger Application Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

Using circuit shown in typical application circuit [Figure 1](#), $T_A = 25^\circ\text{C}$, unless otherwise specified.

ACIN RAMP UP

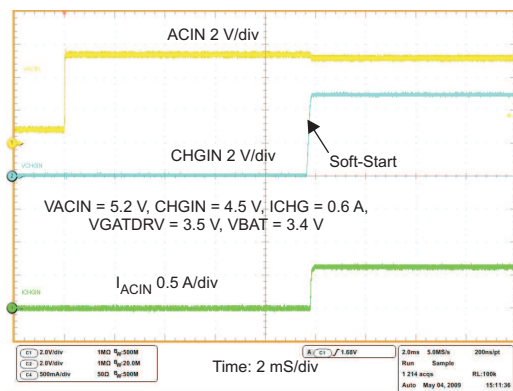


Figure 2.

ACIN RAMP DOWN

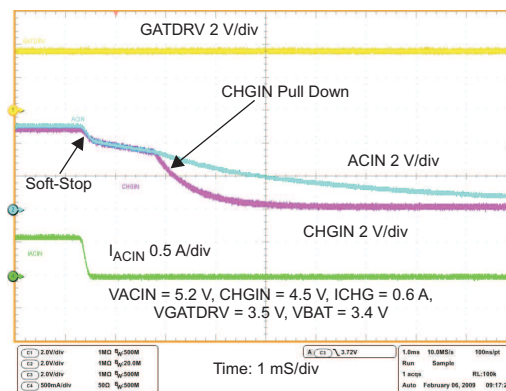


Figure 3.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

ACIN OVP (BLANKING TIME)

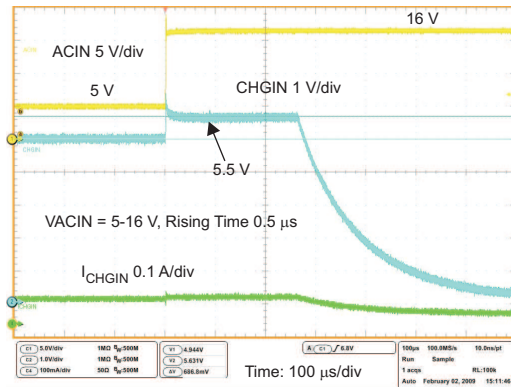


Figure 4.

ACIN OVP

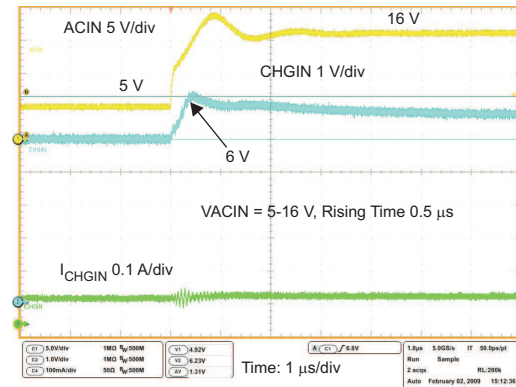


Figure 5.

ACIN OVP

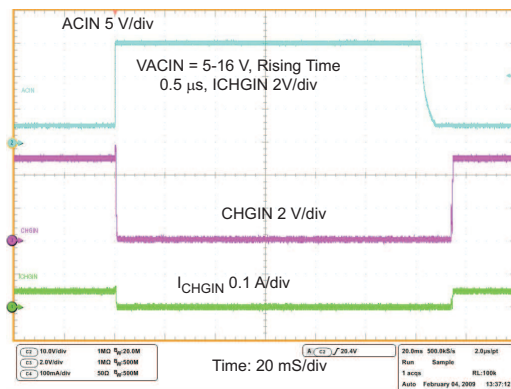


Figure 6.

CHGIN OCP

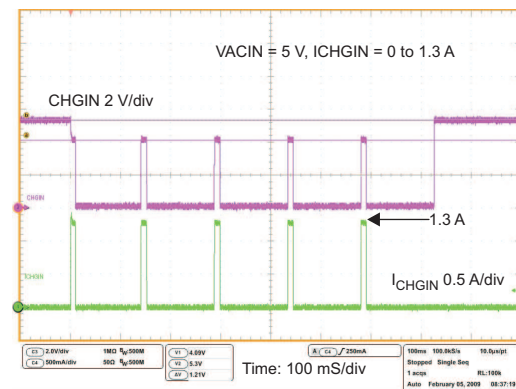


Figure 7.

CHGIN OCP

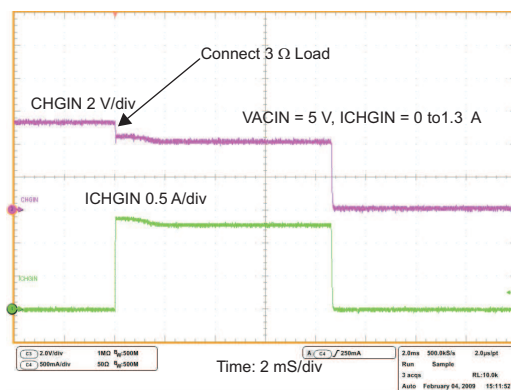


Figure 8.

BATTERY OVP

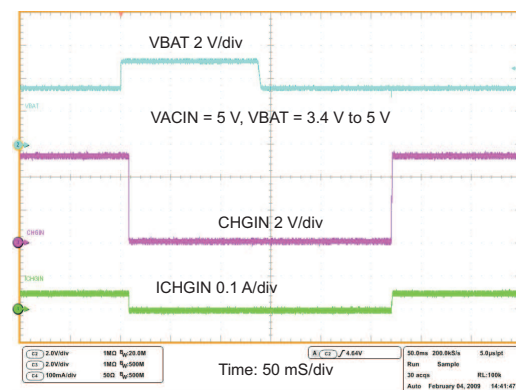


Figure 9.

BATTERY OVP

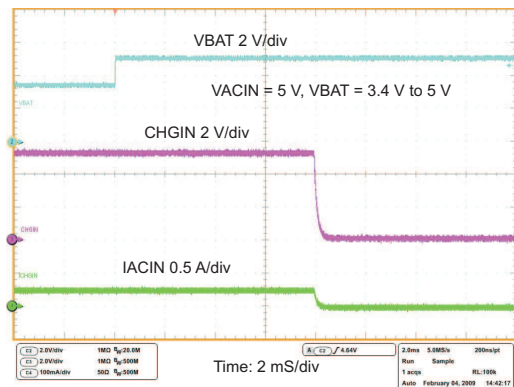


Figure 10.

Rdson vs Vgs

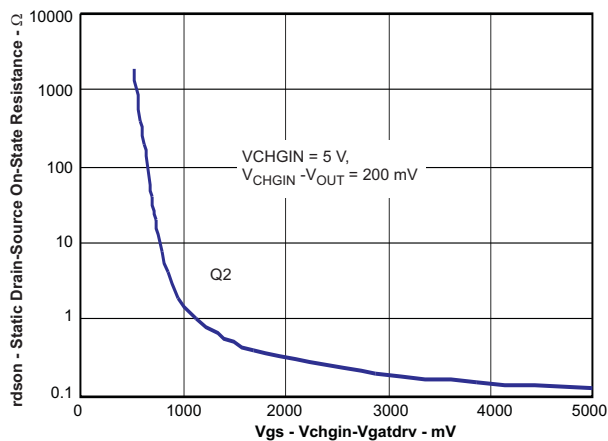


Figure 11.

FET ON RESISTANCE vs TEMPERATURE

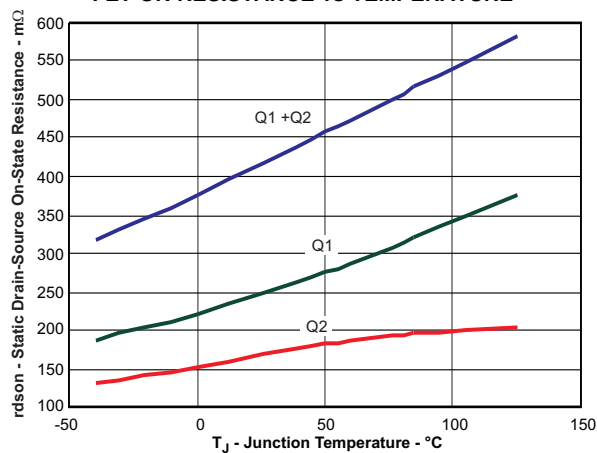


Figure 12.

During the charging process for portable devices, input voltage spikes usually happen when the AC/DC adaptor is plugged in, or charge current is cut off quickly under fault conditions, such as input OVP, OCP or battery OVP and so on. The over voltage stress may damage the analog baseband chip which has lower voltage rating due to its increased complexity. Therefore, over voltage protection is needed for the safe operation of portable devices. Another challenge arises from the charge circuit that uses external charging FET in series with a reverse blocking diode as the charging device. The battery may not be fully charged when input voltage is low due to the additional diode voltage drop. bq24350/2 will provide the solution for above problems since it has input OVP, OCP, battery OVP function, together with integrated charging FET which will eliminate the reverse blocking diode in the previously mentioned charge circuit, as shown in [Figure 1](#).

The bq24350/2 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage and the battery voltage. In case of an input over-voltage condition, the IC will turn off the internal power FET after a blanking time. If the battery voltage rises to unsafe levels during charging process, power is removed from the system. If the input current exceeds the over current threshold for a limited time, the IC will turn off the output power. The integrated charging FET can regulate the charge voltage and current according to the control from the host. The device can also provide a voltage source with over voltage and over current protection for host controller.

POWER DOWN

The device remains in power down mode when the input voltage at the ACIN pin is below the under-voltage threshold V_{UVLO} . The FET Q1 and Q2 connected between ACIN and OUT pins are off.

POWER-ON RESET

The device resets when the input voltage at the ACIN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{BLK(CHGIN)}$ for the input voltage to stabilize. If, after $t_{BLK(CHGIN)}$, the input voltage and battery voltage are in normal range, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input, where the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit. Once the soft-start sequence starts, the IC monitors the load current. If the load current is larger than $I_{O(OCF)}$ for more than $t_{DGL(OCF)}$, FET Q1 and Q2 are switched off. The IC then repeats the power-on sequence after $t_{REC(OCF)}$.

When a short-circuit is detected at power-on and Q1 is switched off, to prevent the input voltage from spiking up due to resonance between the inductance of the input cable and the input capacitor, Q1 is turned off slowly by reducing its gate-drive gradually, resulting in a “soft-stop”.

SLEEP MODE

When ACIN falls to below sleep mode entry threshold (V_{SENTRY}), the device operates in sleep mode and turns off Q1 and Q2 by internal circuit regardless of the gate drive signal from GARDRV pin. The device exits sleep mode when ACIN rising to above sleep mode exit threshold (V_{SEXIT}). In this way, the device behaves like a diode and no external reverse blocking diode is needed in the application circuit.

OPERATING

The device continuously monitors the input voltage, the input current and the battery voltage as described in detail below:

Input Over-Voltage Protection and LDO Mode Operation

The CHGIN output of the IC operates similar to a linear regulator. Figure 13 shows the typical input OVP performance. When the ACIN input voltage is less than $V_{O(REG)}$, and above the V_{UVLO} , the CHGIN output voltage tracks the input voltage with a voltage drop caused by $R_{DS(on)}$ of the protection FET Q1. When the ACIN input voltage is greater than $V_{O(REG)}$ plus the $R_{DS(on)}$ drop of Q1, and less than V_{OVP} , the CHGIN output voltage is regulated to $V_{O(REG)}$, and this is also referred as LDO mode operation. If the input voltage rises above V_{OVP} , the internal FET Q1 and Q2 are turned off after a blanking time of $t_{DGL(OVP)}$, removing power from the circuit. When the input voltage drops below $V_{OVP} - V_{HYS-OVP}$, and is still above V_{UVLO} , the FET Q1 and Q2 are turned on again after a deglitch time of $t_{REC(OVP)}$, which ensures that the input supply is stabilized when the IC starts up again.

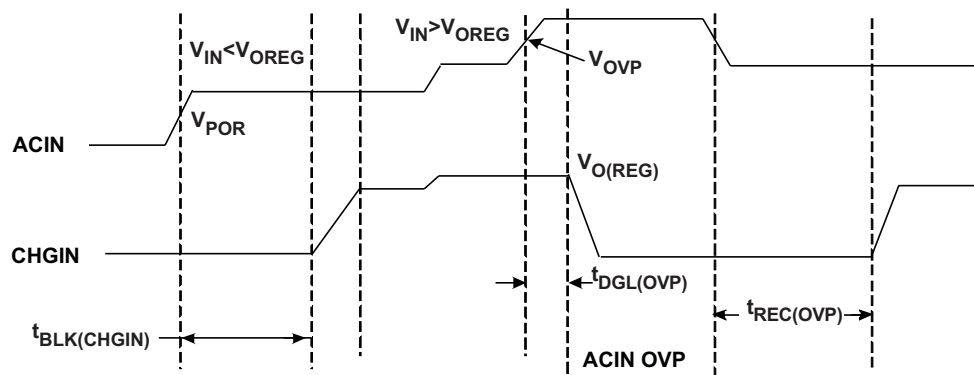


Figure 13. Input OVP Timing Diagram

Over Current Limiting and Protection

The device includes a low drop out linear current regulator. This current regulator uses Q1 as the controlling

power device. Once the soft start sequence starts, the input current is limited to the Over Current Protection (OCP) threshold, $I_{O(OC)}$. If the input current through the IC attempts to exceed the OCP threshold, the switch Q1 is opened only enough to maintain the current at the OCP level. If the current limiting condition is maintained longer than the deglitch time, $t_{DGL(OC)}$, both the switch Q1 and Q2 are opened completely, as shown in Figure 14. In this fault case, the switch Q1 is turned off slowly, typically taking 100 μ S.

Once the OCP feature has been activated, the switch Q1 and Q2 will remain off for the OCP recovery time, $t_{REC(OC)}$. Following this time the switch will turn on, using soft start sequence. If the current through the IC remains below the OCP threshold, the switch will remain closed and normal operation resumes. If the current through the IC attempts to exceed the OCP threshold again, the operation described above repeats.

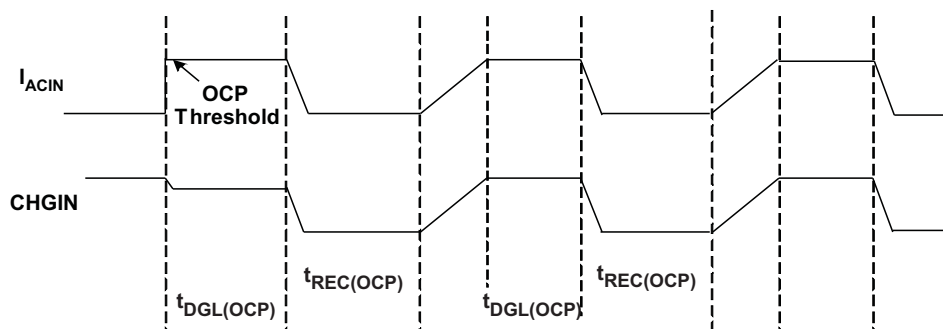


Figure 14. Charge Current OCP Timing Diagram

Battery Over-Voltage Protection

The battery over-voltage threshold, BV_{OVP} , is internally set to 4.35V. If the battery voltage exceeds the BV_{OVP} threshold, the FET Q1 and Q2 are turned off after a deglitch time of $t_{DGL(BOVP)}$. The FET is turned on once the battery voltage drops to $BV_{OVP} - V_{HYS-BOVP}$ and remains below this threshold for $t_{REC(BOVP)}$, as shown in Figure 15. In this battery over-voltage fault case, Q1 is switched OFF gradually for a smooth transient response.

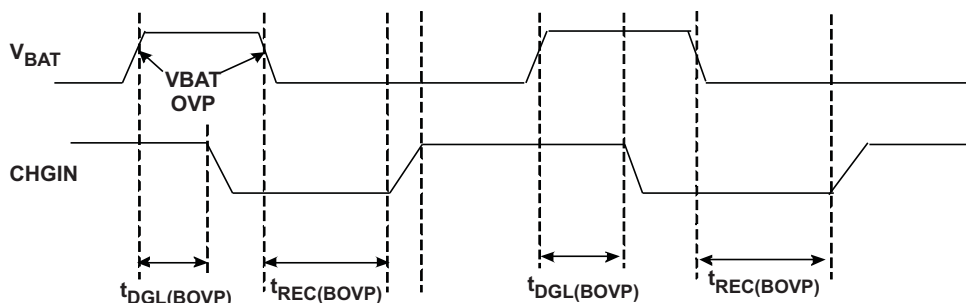


Figure 15. Battery OVP Timing Diagram

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 and Q2 are turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

APPLICATION INFORMATION

Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the ACIN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the device can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of failure of the IC. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current I_{VBAT} causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100k Ω to 470k Ω is a good compromise. In the case of IC failure, with R_{BAT} equal to 100k Ω , the maximum current flowing into the battery would be $(30V - 3V) \div 100k\Omega = 270\mu A$, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100k Ω would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT} = 1mV$. This is negligible compared to the internal tolerance of 50mV on the BV_{OVP} threshold.

If the Battery OVP function is not required, the VBAT pin should be connected to GND.

Selection of Input and Output Bypass Capacitors

The input capacitor C_{ACIN} is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{ACIN} prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1 μF be used at the input of the device. It should be located in close proximity to the ACIN pin.

C_{CHGIN} should also be a ceramic capacitor of at least 1 μF , located close to the CHGIN pin. C_{CHGIN} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

PCB Layout Guidelines

1. This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the maximum voltages expected to be seen in the system.
2. The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
3. C_{ACIN} and C_{CHGIN} should be located close to the IC. Other components like R_{BAT} should also be located close to the IC.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
BQ24350DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24350DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24352DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24352DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24350DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24350DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24352DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24352DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

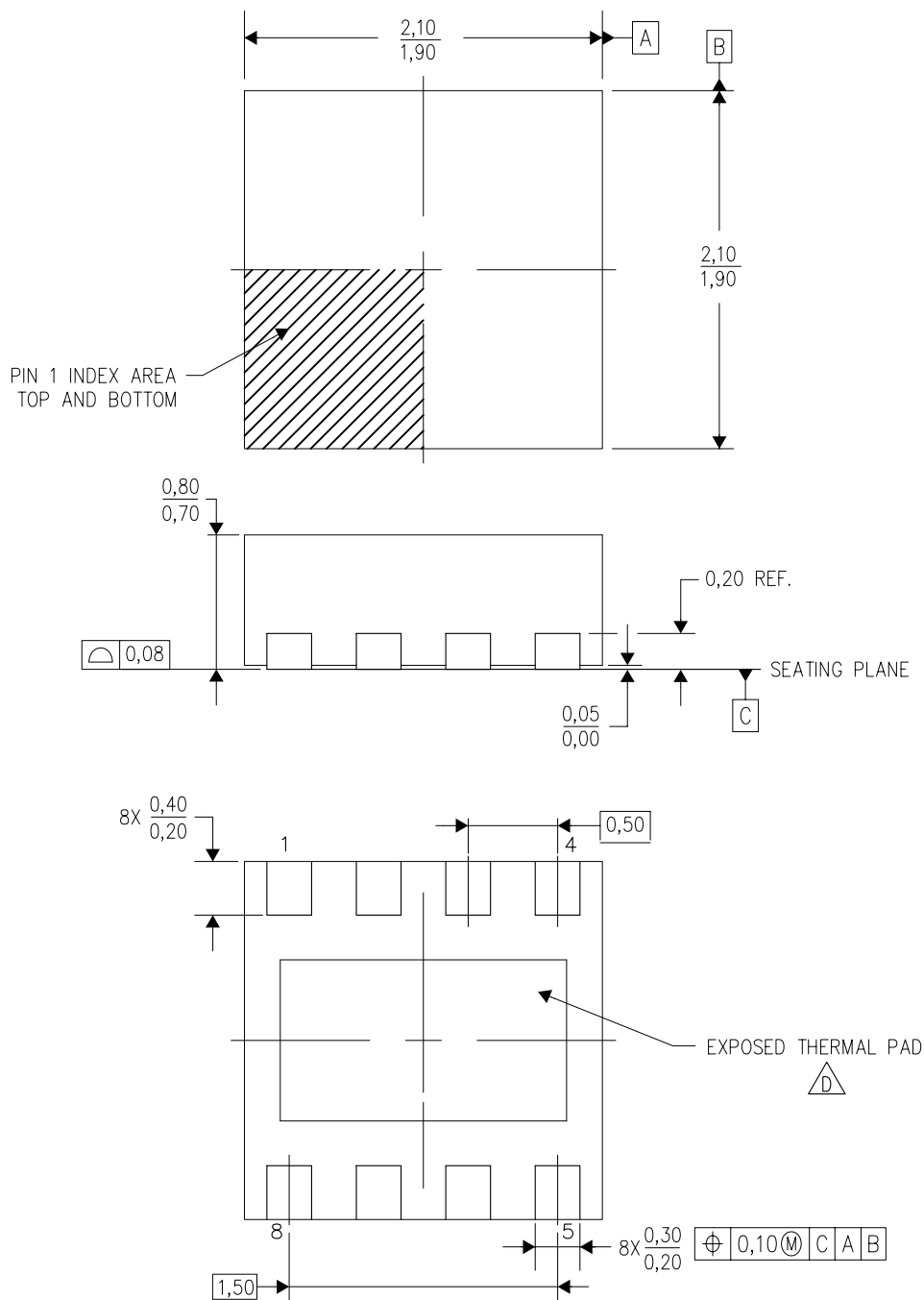


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24350DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24350DSGT	WSON	DSG	8	250	195.0	200.0	45.0
BQ24352DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24352DSGT	WSON	DSG	8	250	195.0	200.0	45.0

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4208210/B 10/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Quad Flatpack, No-Leads (QFN) package configuration.

 The package thermal pad must be soldered to the board for thermal and mechanical performance.

See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

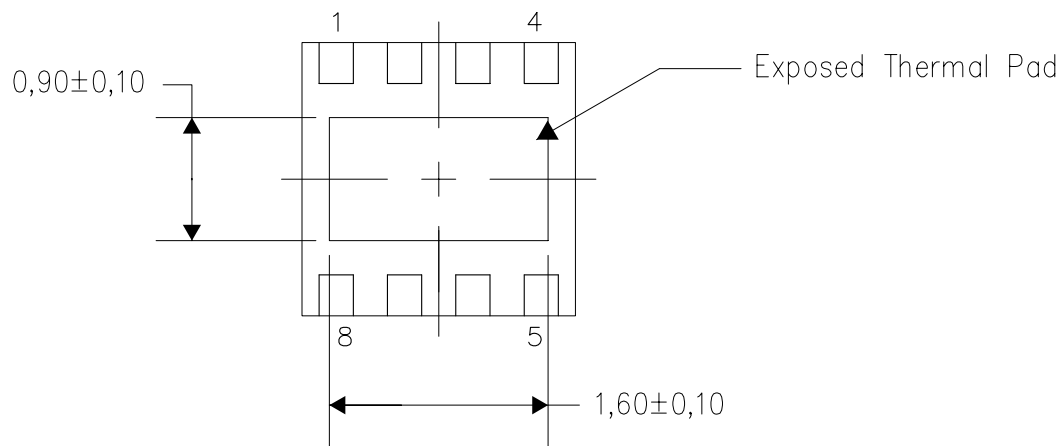
E. Falls within JEDEC MO-229.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

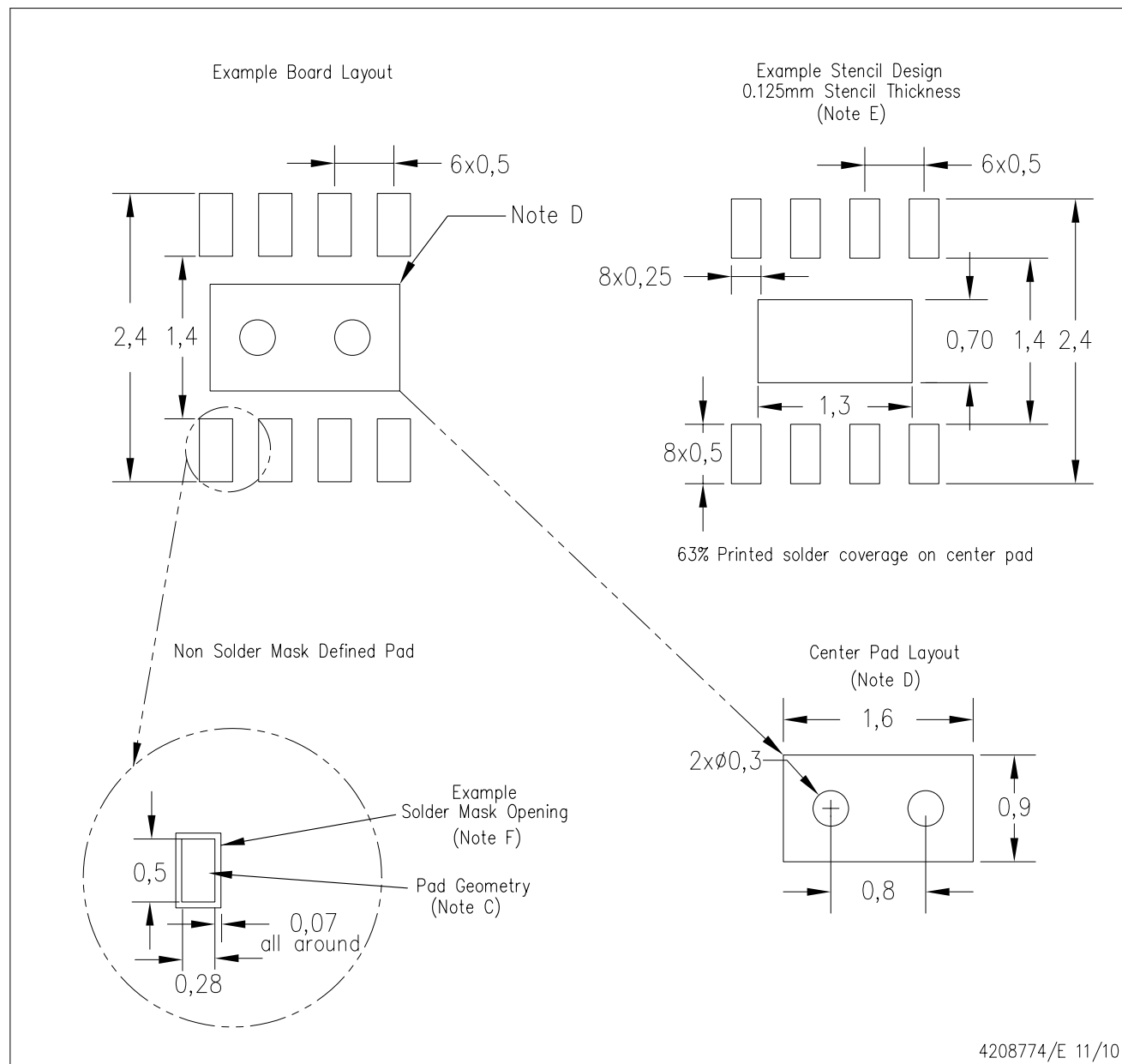
Exposed Thermal Pad Dimensions

4208347/E 11/10

NOTE: A. All linear dimensions are in millimeters

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated