

# Octal Channel 14-Bit, 80 MSPS High-SNR and Low-Power ADC

Check for Samples: [ADS5294](#)

## FEATURES

- **Maximum Sample Rate: 80 MSPS/14-Bit**
- **High Signal-to-Noise Ratio**
  - **75.5-dBFS SNR at 5 MHz/80 MSPS**
  - **78.2-dBFS SNR at 5 MHz/80 MSPS and Decimation Filter Enabled**
  - **84-dBc SFDR at 5 MHz/80 MSPS**
- **Low Power Consumption**
  - **58 mW/CH at 50 MSPS**
  - **77 mW/CH at 80 MSPS (2 LVDS Wire Per Channel)**
- **Digital Processing Block**
  - **Programmable FIR Decimation Filter and Oversampling to Minimize Harmonic Interference**
  - **Programmable IIR High Pass Filter to Minimize DC Offset**
  - **Programmable Digital Gain: 0 dB to 12 dB**
  - **2- or 4- Channel Averaging**
- **Flexible Serialized LVDS Outputs:**
  - **One or Two Wires of LVDS Output Lines per Channel Depending on ADC Sampling Rate**
  - **Programmable Mapping Between ADC Input Channels and LVDS Output Pins-Eases Board Design**
  - **Variety of Test Patterns to Verify Data Capture by FPGA/Receiver**
- **Internal and External References**
- **1.8V Operation for Low Power Consumption**
- **Low-Frequency Noise Suppression**
- **Recovery From 6-dB Overload within 1 Clock Cycle**
- **Package: 12-mm × 12-mm 80-Pin QFP**

## APPLICATIONS

- **Ultrasound Imaging**
- **Communication Applications**
- **Multi-channel Data Acquisition**

## DESCRIPTION

Using CMOS process technology and innovative circuit techniques, the ADS5294 is a low power 80MSPS 8-Channel ADC. Low power consumption, high SNR, low SFDR, and consistent overload recovery allow users to design high performance systems.

The ADS5294 has a digital processing block that integrates several commonly used digital functions for improving system performance. It includes a digital filter module that has built-in decimation filters (with low-pass, high-pass and band-pass characteristics). The decimation rate is also programmable (by 2, by 4, or by 8). This makes it useful for narrow-band applications, where the filters can be used conveniently to improve SNR and knock-off harmonics, while at the same time reducing the output data rate. The device includes an averaging mode where two channels (or even four channels) can be averaged to improve SNR.

Serial LVDS outputs reduce the number of interface lines and enable the highest system integration. The digital data from each channel ADC can be output over one or two wires of LVDS output lines depending on the ADC sampling rate. This 2-wire interface helps keep the serial data rate low, allowing low cost FPGA based receivers to be used even at high sample rate. The ADC resolution can be programmed to 12 bit or 14 bit through registers. A very unique feature is the programmable mapping module that allows flexible mapping between the input channels and the LVDS output pins. This helps greatly reduce the complexity of LVDS output routing and can potentially result in cheaper system boards by reducing the number of PCB layers.

The device integrates an internal reference trimmed to accurately match across devices. Best performance is expected to be achieved through the internal reference mode. The device can be driven with external references as well.

The device is available in a 12 mm × 12 mm 80-pin QFP. It is specified over a –40°C to 85°C operating temperature range. ADS5294 is completely pin-to-pin and register compatible to ADS5292.



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**ADS5294**

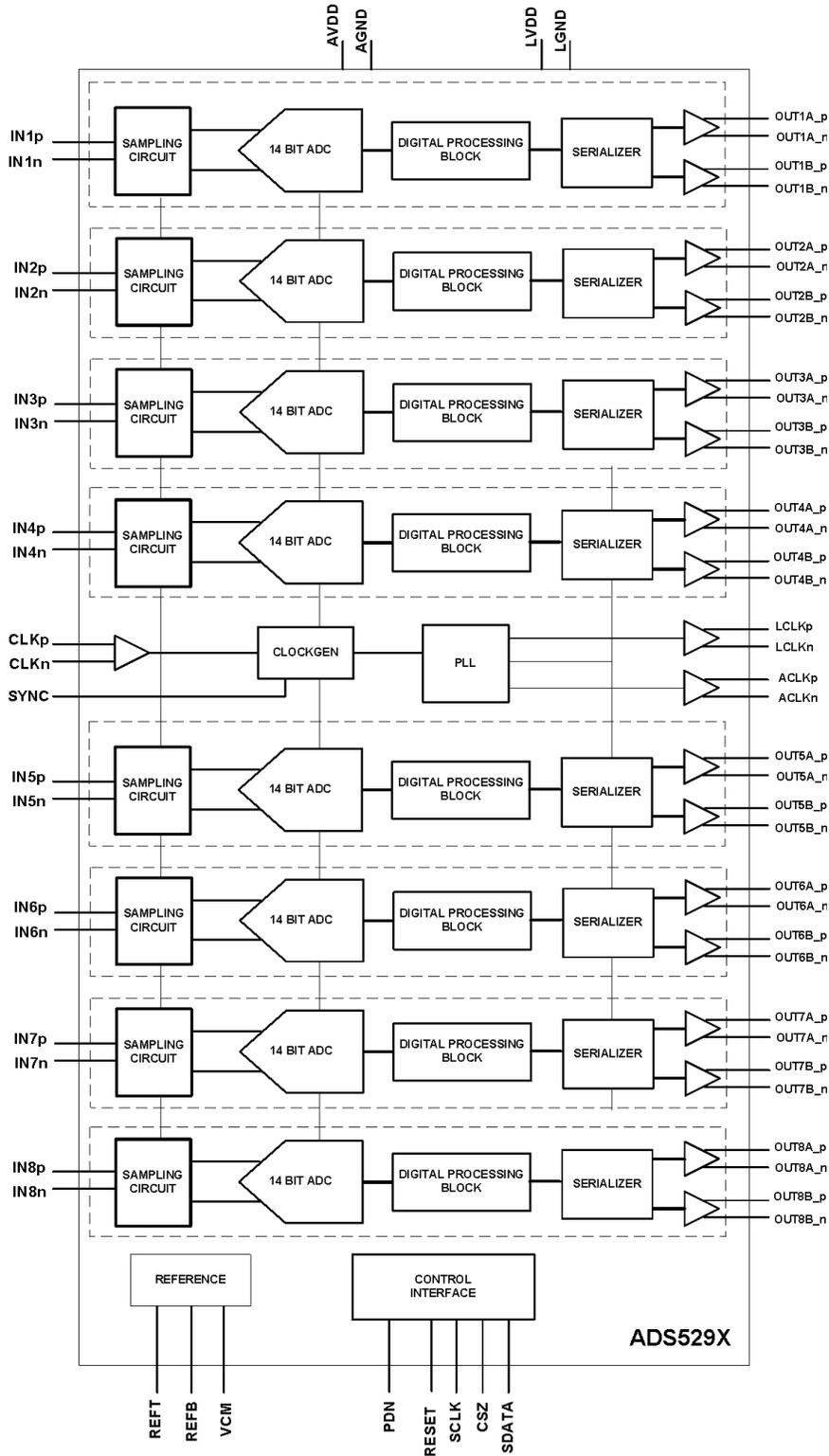
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

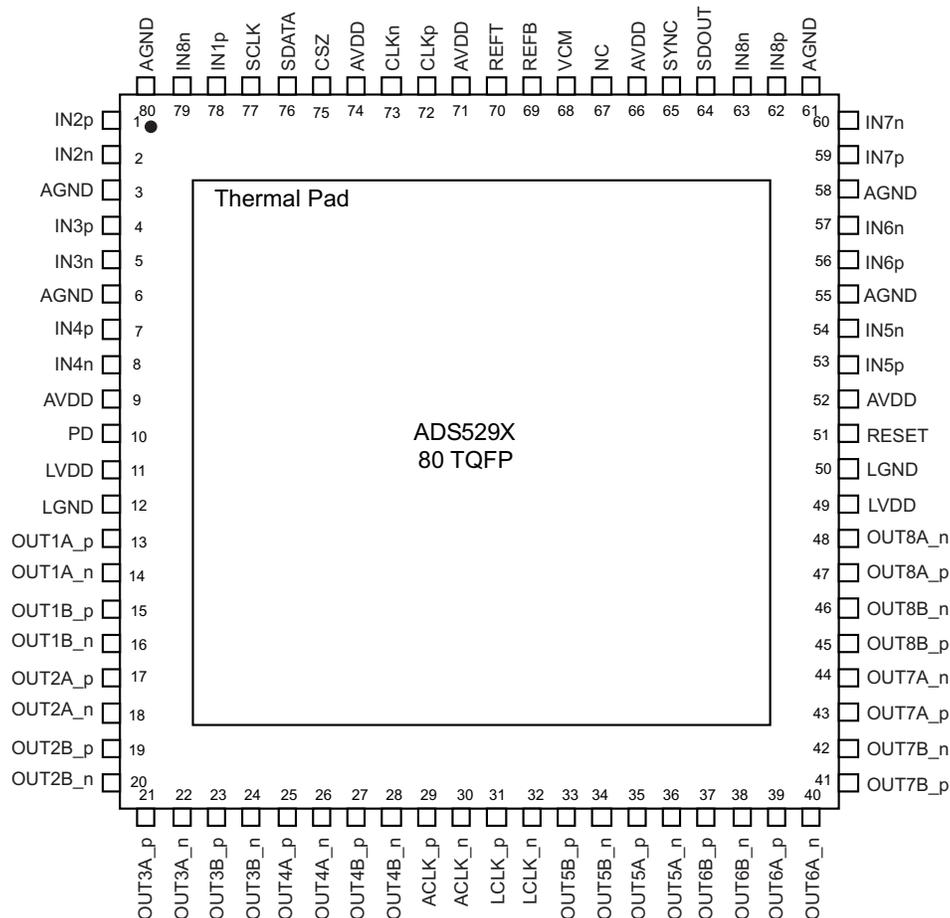


**Figure 1. Block Diagram**

**PACKAGING/ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	PACKAGE TYPE	OPERATING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5294	PFP	-40°C to 85°C	ADS5294IPFP	Tray, 480 (MOQ)
			ADS5294IPFPR	Tape and Reel, 1000
			ADS5294IPFPT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

**PIN CONFIGURATION**
**80-PIN TQFP WITH THERMAL PAD  
PFP PACKAGE (TOP VIEW)**

**PIN FUNCTIONS**

NUMBER OF PINS	PIN		DESCRIPTION
	NAME	NUMBER	
5	AVDD	9, 52, 66, 71, 74	Analog power supply, 1.8V
6	AGND	3, 6, 55, 58, 61, 80	Analog ground
1	VCM	68	Common-mode output pin, 0.95 V output. This pin can be configured as the external reference voltage (1.5 V) input pin as well. See Reg 0x42.
1	CLKN	73	Negative differential clock –Tie CLKN to GND for single-ended clock
1	CLKP	72	Positive differential clock
2	IN1P, IN1N	78, 79	Differential input signal, Channel 1
2	IN2P, IN2N	1, 2	Differential input signal, Channel 2
2	IN3P, IN3N	4, 5	Differential input signal, Channel 3

**PIN FUNCTIONS (continued)**

NUMBER OF PINS	PIN		DESCRIPTION
	NAME	NUMBER	
2	IN4P, IN4N	7, 8	Differential input signal, Channel 4
2	IN5P, IN5N	53, 54	Differential input signal, Channel 5
2	IN6P, IN6N	56, 57	Differential input signal, Channel 6
2	IN7P, IN7N	59, 60	Differential input signal, Channel 7
2	IN8P, IN8N	62, 63	Differential input signal, Channel 8
2	LCLKP, LCLKN	31, 32	Differential LVDS bit clock (7X)
2	ACLKP, ACLKN	29, 30	Differential LVDS frame clock (1X)
2	OUT1A_P, OUT1A_N	13, 14	Differential LVDS data output, wire 1, channel 1
2	OUT1B_P, OUT1B_N	15, 16	Differential LVDS data output, wire 2, channel 1
2	OUT2A_P, OUT2A_N	17, 18	Differential LVDS data output, wire 1, channel 2
2	OUT2B_P, OUT2B_N	19, 20	Differential LVDS data output, wire 2, channel 2
2	OUT3A_P, OUT3A_N	21, 22	Differential LVDS data output, wire 1, channel 3
2	OUT3B_P, OUT3B_N	23, 24	Differential LVDS data output, wire 2, channel 3
2	OUT4A_P, OUT4A_N	25, 26	Differential LVDS data output, wire 1, channel 4
2	OUT4B_P, OUT4B_N	27, 28	Differential LVDS data output, wire 2, channel 4
2	OUT5A_P, OUT5A_N	35, 36	Differential LVDS data output, wire 1, channel 5
2	OUT5B_P, OUT5B_N	33, 34	Differential LVDS data output, wire 2, channel 5
2	OUT6A_P, OUT6A_N	39, 40	Differential LVDS data output, wire 1, channel 6
2	OUT6B_P, OUT6B_N	37, 38	Differential LVDS data output, wire 2, channel 6
2	OUT7A_P, OUT7A_N	43, 44	Differential LVDS data output, wire 1, channel 7
2	OUT7B_P, OUT7B_N	41, 42	Differential LVDS data output, wire 2, channel 7
2	OUT8A_P, OUT8A_N	47, 48	Differential LVDS data output, wire 1, channel 8
2	OUT8B_P, OUT8B_N	45, 46	Differential LVDS data output, wire 2, channel 8
1	PD	10	Power down control input. Active High. The pin has an internal 220-kΩ pulldown resistor.
1	REFB	69	Negative reference input/ output
1	REFT	70	Positive reference input/ output
1	RESET	51	Active HIGH RESET input. The pin has an internal 220-kΩ pulldown resistor.
1	SCLK	77	Serial clock input. The pin has an internal 220-kΩ pulldown resistor.
1	SDATA	76	Serial data input. The pin has an internal 220-kΩ pulldown resistor.
1	SDOUT	64	Serial data readout. This pin is in the high-impedance state after reset. When the <READOUT> bit is set, the SDOOUT pin becomes active. This is a CMOS digital output running from the AVDD supply.
1	CSZ	75	Serial enable chip select – active low digital input
1	SYNC	65	Input signal to synchronize channels and chips when used with reduced output data rates.
2	LVDD	11, 49	Digital and I/O power supply, 1.8V
2	LGND	12, 50	Digital ground
1	NC	67	No Connection. Must leave floated

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	AVDD	-0.3	2.2	V
	LVDD	-0.3	2.2	V
Voltage	between AGND and LGND	-0.3	0.3	V
	at analog inputs	-0.3	min[2.2, AVDD+0.3]	V
	at digital inputs, CLKN, CLKP <sup>(2)</sup> , RESET, SCLK, SDATA, $\overline{CSZ}$	-0.3	min[2.2, AVDD+0.3]	V
	at digital outputs	-0.3	min[2.2, LVDD+0.3]	V
Maximum junction temperature (T <sub>J</sub> ), any condition			105	°C
Storage temperature range		-55	150	°C
Operating temperature range		-40	85	°C
ESD Ratings	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V

- (1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
- (2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKN is < |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		ADS5294	UNITS
		PPF (80 PINS)	
$\theta_{JA}$	Junction-to-ambient thermal resistance	30.8	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	6.3	
$\theta_{JB}$	Junction-to-board thermal resistance	8.3	
$\Psi_{JT}$	Junction-to-top characterization parameter	0.2	
$\Psi_{JB}$	Junction-to-board characterization parameter	8.2	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	0.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

**RECOMMENDED OPERATING CONDITIONS**

		MIN	TYP	MAX	UNIT
<b>SUPPLIES</b>					
AVDD	Analog supply voltage	1.7	1.8	1.9	V
LVDD	Digital supply voltage	1.7	1.8	1.9	V
<b>ANALOG INPUTS/OUTPUTS</b>					
Differential input voltage range		2			V <sub>PP</sub>
Input common-mode voltage		0.95±0.05			V
REF <sub>T</sub>	External reference mode	1.45			V
REF <sub>B</sub>	External reference mode	0.45			V
VCM	Common-mode voltage output	0.95			V
	External Reference mode Input	1.5			V
Maximum Input Frequency <sup>(1)</sup>		2 V <sub>PP</sub> amplitude		80	MHz
<b>CLOCK INPUTS</b>					
ADC Clock input sample rate		10		80	MSPS
Input Clock amplitude differential (V <sub>(CLKP)</sub> - V <sub>(CLKN)</sub> ) peak-to-peak		Sine wave, AC-coupled		0.2	1.5
		LVPECL, AC-coupled		0.2	1.6
		LVDS, AC-coupled		0.2	0.7
V <sub>IL</sub>	Input Clock CMOS single-ended (V <sub>(CLKP)</sub> )			<0.3	V
V <sub>IH</sub>				>1.5	V
Input clock duty cycle		35%	50%	65%	
<b>DIGITAL OUTPUTS</b>					
ACLKP and ACLKN outputs (LVDS), 1-wire interface		1x (sample rate)			MSPS
LCLKP and LCLKN outputs (LVDS), 1-wire interface		7x (sample rate)			MSPS
ACLKP and ACLKN outputs (LVDS), 2-wire interface		0.5x (sample rate)			MSPS
LCLKP and LCLKN outputs (LVDS), 2-wire interface		3.5x (sample rate)			MSPS
Maximum data rate, 2-wire interface		560			Mbps
Maximum data rate, 1-wire interface		700			Mbps
C <sub>LOAD</sub>	Maximum external capacitance from each output pin to LGND	5			pF
R <sub>LOAD</sub>	Differential load resistance between the LVDS output pairs	100			Ω
T <sub>A</sub>	Operating free-air temperature	-40		85	°C

(1) See the [Large and Small Signal Input Bandwidth](#) section.

## ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, -1 dBFS differential analog input, Sample rate = 80 MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC PERFORMANCE</b>						
SNR	Signal-to-noise ratio	f <sub>in</sub> = 10 MHz, 65 MSPS		75.6		dBFS
		f <sub>in</sub> = 5 MHz, T <sub>A</sub> = 25°C	72.8	75.5		dBFS
		f <sub>in</sub> = 5 MHz, Across temperatures	71.8			dBFS
		f <sub>in</sub> = 5 MHz, -60 dBFS Input signal amplitude		77.3		dBFS
		f <sub>in</sub> = 5 MHz, Decimation by two enabled		78.2		dBFS
		f <sub>in</sub> = 30 MHz		74.2		dBFS
		f <sub>in</sub> = 65 MHz		71.7		dBFS
SINAD	Signal-to-noise and distortion ratio	f <sub>in</sub> = 5 MHz		74.8		dBFS
		f <sub>in</sub> = 30 MHz		73.4		dBFS
		f <sub>in</sub> = 65 MHz		70		dBFS
ENOB	Effective number of bits	f <sub>in</sub> = 5 MHz		12.2		Bits
DNL	Differential nonlinearity	f <sub>in</sub> = 5 MHz	-0.96	±0.5	1.7	LSB
INL	Integral nonlinearity	f <sub>in</sub> = 5 MHz		2.2	5.5	LSB
SFDR	Spurious-free dynamic range	f <sub>in</sub> = 5 MHz	72	84		dBc
		f <sub>in</sub> = 30 MHz		81		dBc
		f <sub>in</sub> = 65 MHz		74		dBc
THD	Total harmonic distortion	f <sub>in</sub> = 5 MHz	70.5	82		dBc
		f <sub>in</sub> = 30 MHz		80		dBc
		f <sub>in</sub> = 65 MHz		73.5		dBc
HD2	Second-harmonic distortion	f <sub>in</sub> = 5 MHz	73	93		dBc
		f <sub>in</sub> = 30 MHz		88		dBc
		f <sub>in</sub> = 65 MHz		85		dBc
HD3	Third-harmonic distortion	f <sub>in</sub> = 5 MHz	72	84		dBc
		f <sub>in</sub> = 30 MHz		81		dBc
		f <sub>in</sub> = 65 MHz		74		dBc
	Worse spur excluding HD2, HD3	f <sub>in</sub> = 5 MHz		91		dBc
		f <sub>in</sub> = 30 MHz		83		dBc
		f <sub>in</sub> = 65 MHz		76		dBc
IMD3	Intermodulation distortion	f <sub>in</sub> = 8 MHz at -7 dBFS, f <sub>2</sub> = 10 MHz at -7 dBFS		84.5		dBc
	Overload recovery	Recovery to within 1% of full-scale for 6-dB overload with sine wave input		1		Clock Cycle
XTALK	Cross-talk	f <sub>in</sub> = 10 MHz, -1 dBFS signal applied on aggressor channel no signal applied on victim channel	far channel		90	dBc
			near channel		85	dBc
	Phase noise	5 MHz, 1 kHz off carrier		-138		dBc/Hz
<b>ANALOG INPUT / OUTPUT</b>						
	Differential input voltage range (0-dB gain)			2		V <sub>PP</sub>
R <sub>IN</sub>	Differential Input Resistance	At DC		2		kΩ
C <sub>IN</sub>	Differential Input Capacitance	At DC		3.2		pF
	Analog input bandwidth	With a 50 Ωsource impedance		550		MHz
	Analog input common-mode current (per input pin)			1.6		μA/MSPS
	VCM common-mode output voltage			0.95		V
	VCM output current capability			5		mA

**ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, Sample rate = 80 MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
	Offset error	Across devices and across channels within a device	–15		15	mV
	Temperature coefficient of offset error			<0.01		mV/ °C
E <sub>(GREF)</sub>	Gain error due to internal reference inaccuracy alone	Across devices	–2		2	%FS
E <sub>(GCHAN)</sub>	Gain error of channel alone			0.5		%FS
	Temperature coefficient of E <sub>(GCHAN)</sub>			<0.01		%FS/ °C
<b>POWER SUPPLY</b>						
Power consumption		80 MSPS, 14 Bit, 2-wire LVDS		77		mW/CH
		50 MSPS, 1-wire LVDS		58		mW/CH
		40 MSPS, 14 Bit, 1-wire LVDS		52		mW/CH
		10 MSPS, 14 Bit, 1-wire LVDS		33		mW/CH
		f <sub>in</sub> = 10 MHz, 80 MSPS, 14 Bit, Decimation filter = 2, 1-wire LVDS		100		mW/CH
AVDD		14 Bit, 80 MSPS		230	265	mA
		14 Bit, 65 MSPS		200		mA
		14 Bit, 40 MSPS		155		mA
LVDD		80 MSPS, 14 Bit, 2-wire LVDS		111	122	mA
		50 MSPS, 14 Bit, 1-wire LVDS		80		mA
		40 MSPS, 14 Bit, 1-wire LVDS		73		mA
		80 MSPS, 1 Bit, Decimation filter = 2, 1-wire LVDS		210		mA
Power-down power consumption		Partial Power Down (80 MSPS, 2-wire)		175		mW
		Complete Power Down			60	mW
	Power supply modulation ratio	Carrier = 5 MHz, f <sub>(PSRR)</sub> = 10 kHz, 50 mVpp on AVDD		35		dB
	Power supply rejection ratio	AC power supply rejection ratio f = 10 kHz		55		dB

## DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 1.8V, LVDD = 1.8V

PARAMETERS		CONDITION	MIN	TYP	MAX	UNITS
<b>DIGITAL INPUTS/OUTPUTS</b>						
V <sub>IH</sub>	Logic high input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels.	1.3			V
V <sub>IL</sub>	Logic low input voltage				0.4	V
I <sub>IH</sub>	Logic high input current	V <sub>HIGH</sub> = 1.8 V		6		μA
I <sub>IL</sub>	Logic low input current	V <sub>LOW</sub> = 0 V		< 0.1		μA
V <sub>OH</sub>	Logic high output voltage			AVDD - 0.1		V
V <sub>OL</sub>	Logic low output voltage			0.2		V
<b>LVDS OUTPUTS</b>						
V <sub>ODH</sub>	High-level output differential voltage	100 Ω external termination	245	350	405	mV
V <sub>ODL</sub>	Low-level output differential voltage	100 Ω external termination	-245	-350	-405	mV
V <sub>OCM</sub>	Output common-mode voltage		900	1100	1300	mV

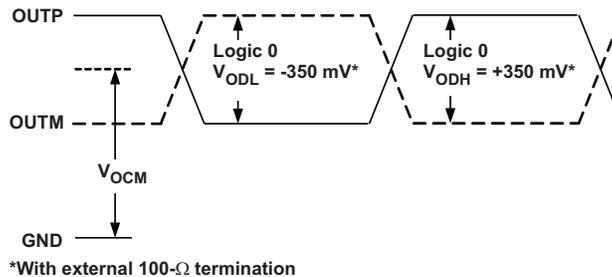


Figure 2. LVDS Output Voltage Levels

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## TIMING REQUIREMENTS<sup>(1)(2)(3)</sup>

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, sampling frequency = 80 MSPS, 14-bit, sine wave input clock = 1.5 Vpp clock amplitude, C<sub>LOAD</sub> = 5 pF, R<sub>LOAD</sub> = 100 Ω, unless otherwise noted. MIN and MAX values are across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, AVDD = 1.8 V, LVDD = 1.7 V to 1.9 V

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
t <sub>a</sub>	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs		4		ns
	Aperture delay variation	Across channels within the same device		±175		ps
		Across devices at the same temperature and LVDD supply		2.5		ns
t <sub>j</sub>	Aperture jitter RMS			320		fs rms
t <sub>d</sub>	Data latency	1-wire LVDS output interface		11		Clock cycles
		2-wire LVDS output interface		15		Clock cycles
t <sub>SU</sub>	Data setup time	80 MSPS, 2 wire LVDS, 7x serialization	0.34	0.57		ns
t <sub>H</sub>	Data hold time	80 MSPS, 2 wire LVDS, 7x serialization	0.55	0.8		ns
t <sub>PROP</sub>	Clock propagation delay	Input clock rising edge(zero cross) to frame clock rising edge(zero cross)	See <a href="#">Table 1</a> and <a href="#">Table 2</a>			
	Variation of t <sub>PROP</sub>	Between two devices at same temperature and LVDD supply		±0.75		ns
	LVDS bit clock duty cycle			48%		
t <sub>RISE</sub>	Data rise time	Rise time is from -100 mV to +100 mV, 10 ≤ Fs ≤ 80 MSPS		0.24		ns
t <sub>FALL</sub>	Data fall time	Fall time is from +100 mV to -100 mV, 10 ≤ Fs ≤ 80 MSPS		0.24		ns
t <sub>CLKRISE</sub>	Output clock rise time	Rise time is from -100 mV to +100 mV, 10 ≤ Fs ≤ 80 MSPS		0.20		ns
t <sub>CLKFALL</sub>	Output clock fall time	Fall time is from +100 mV to -100 mV, 10 ≤ Fs ≤ 80 MSPS		0.20		ns
t <sub>WAKE</sub>	Wake-up Time	Time to valid data after coming out of COMPLETE POWER-DOWN mode		100		μs
		Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)		5		μs

- (1) Timing parameters are ensured by design and characterization and not tested in production.
- (2) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- (3) Data valid refers to logic HIGH of 100 mV and logic LOW of -100 mV.

**Table 1. LVDS Timing at Different Sampling Frequencies - 2 Wire Interface, 7x Serialization <sup>(1)</sup>**

LVDS Output Rate (MSPS)	Setup Time ( $t_{su}$ ), ns			Hold Time ( $t_h$ ), ns			$t_{PROG} = (6/7) \times T + t_{delay}$ , ns <sup>(2)</sup>		
	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			$t_{PROG} = \text{delay from Input clock zero-cross rising edge to frame clock zero cross (rising edge)}$		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
$F_s = 1/T$									
80	0.34	0.57		0.55	0.8		8	9.5	11
65	0.35	0.64		0.8	1.1		8	9.5	11
50	0.7	0.9		1.2	1.5		8	9.5	11
40	1	1.3		1.6	1.85		8	9.5	11
30	1.7	2		2	2.3		8	9.5	11
20	2.9	3.2		3.2	3.5		8	9.5	11
10	6.5	6.7		6.7	7		8	9.5	11

(1) Bit clock and Frame clock jitter has been included in the Setup and hold timing.

(2) Values below correspond to  $t_{delay}$ , NOT  $t_{PROG}$

**Table 2. LVDS Timing at Different Sampling Frequencies - 1 Wire Interface, 14x Serialization <sup>(1)</sup>**

LVDS Output Rate (MSPS)	Setup Time ( $t_{su}$ ), ns			Hold Time ( $t_h$ ), ns			$t_{PROG} = (5/7) \times T + t_{delay}$ , ns <sup>(2)</sup>		
	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			$t_{PROG} = \text{delay from Input clock zero-cross rising edge to frame clock zero cross (rising edge)}$		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
$F_s = 1/T$									
50	0.28	0.48		0.28	0.6		7.5	9	10.5
40	0.5	0.68		0.54	0.8		7.5	9	10.5
30	0.62	0.8		1	1.25		7.5	9	10.5
20	1.2	1.4		1.6	1.9		7.5	9	10.5
10	3.1	3.3		3.3	3.5		7.5	9	10.5

(1) Bit clock and Frame clock jitter has been included in the Setup and hold timing.

(2) Values below correspond to  $t_{delay}$ , NOT  $t_{PROG}$

LVDS TIMING DIAGRAM

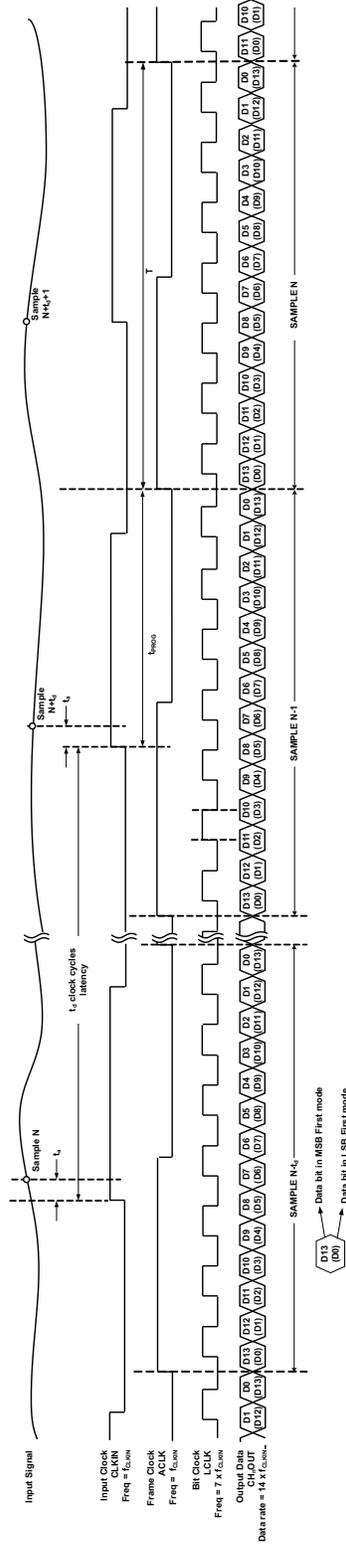


Figure 3. 14-Bit 1 wire LVDS Timing Diagram

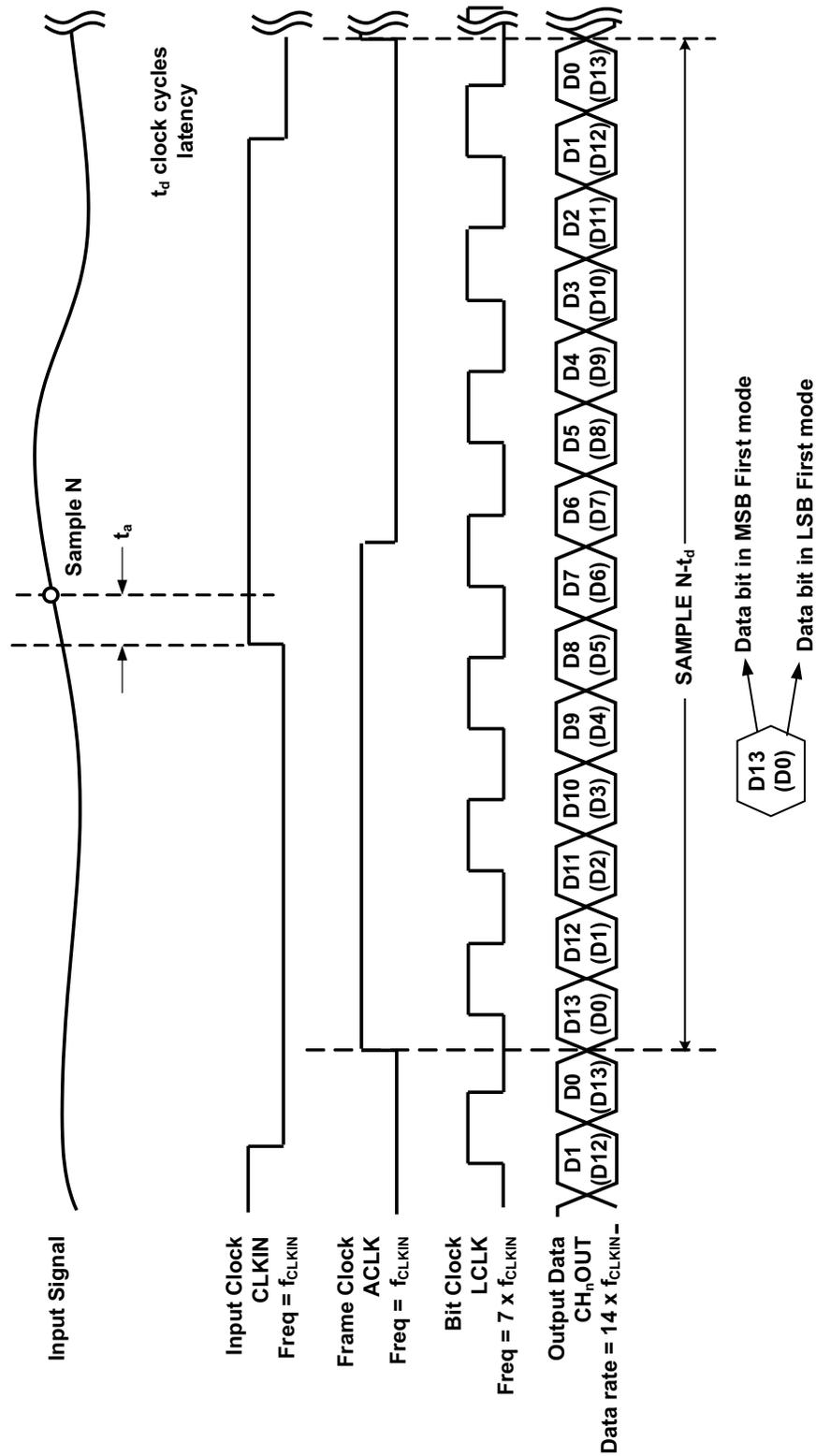


Figure 4. Enlarged 1 wire LVDS Timing Diagram (14bit)

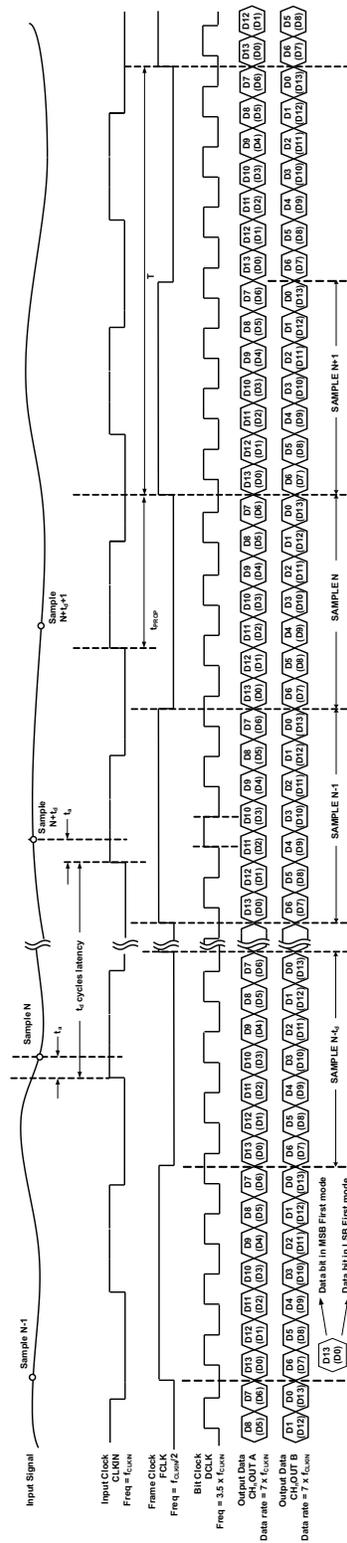


Figure 5. 14-Bit 2-wire LVDS Timing Diagram

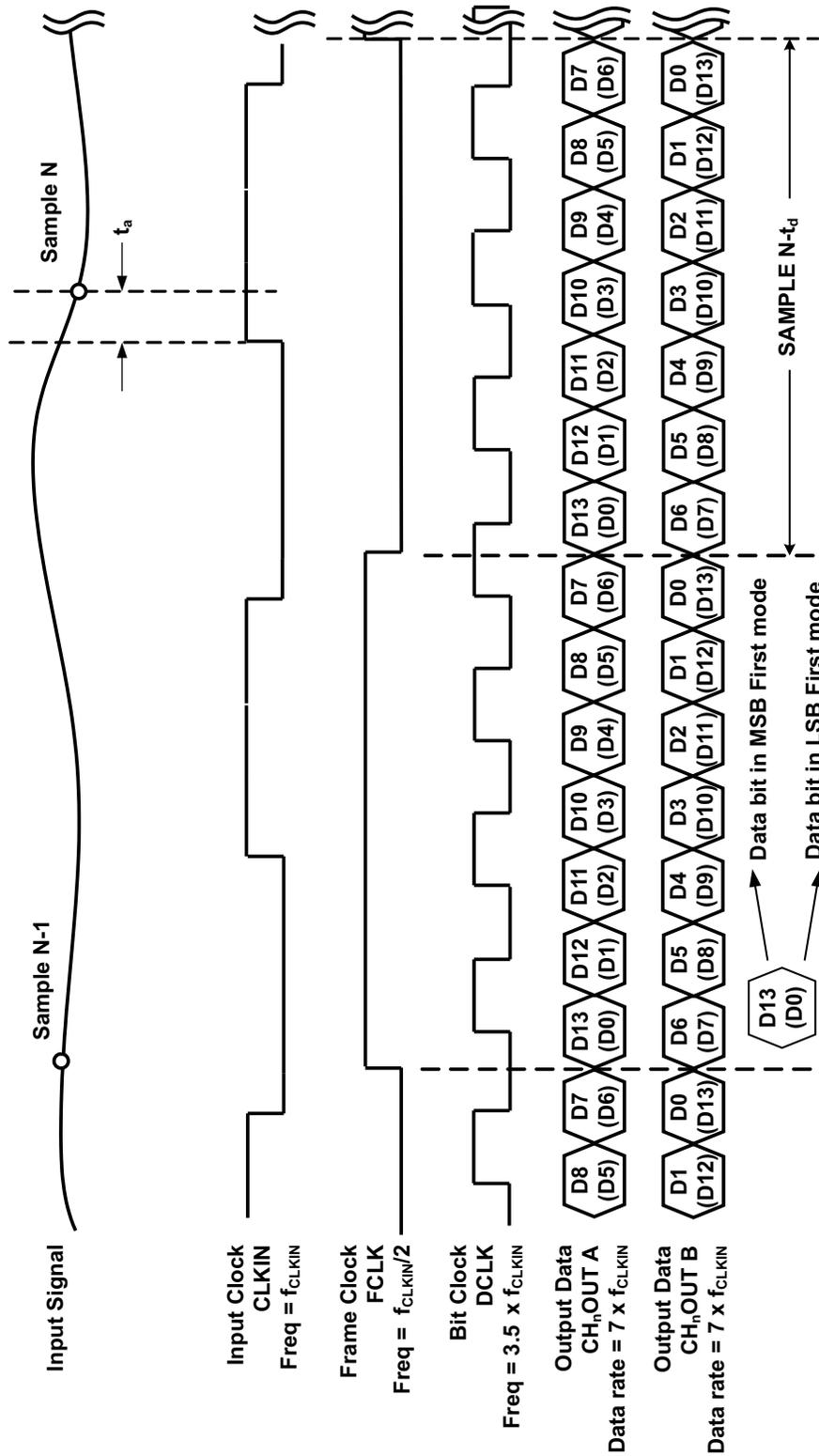
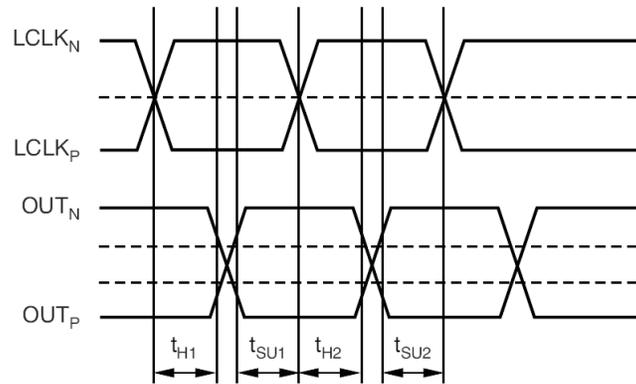


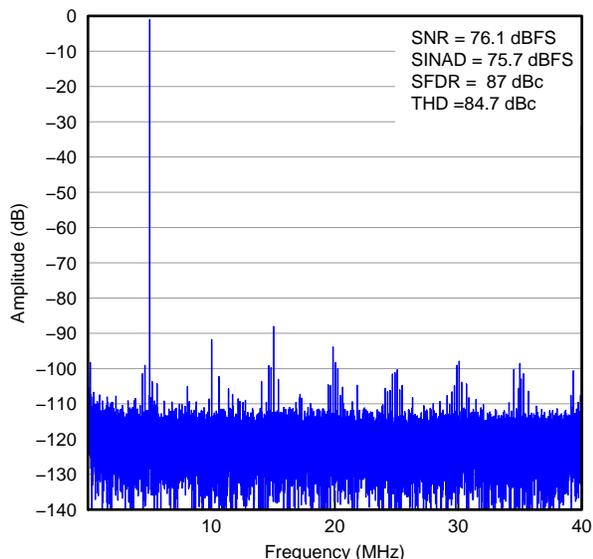
Figure 6. Enlarged 2 wire LVDS Timing Diagram (14bit)



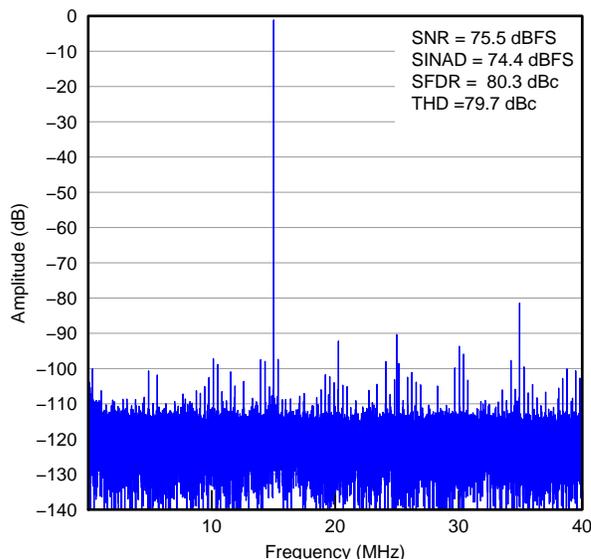
**Figure 7. Definition of Setup and Hold Times  $t_{SU} = \min(t_{SU1}, t_{SU2})$ ;  $t_H = \min(t_{H1}, t_{H2})$**

**TYPICAL CHARACTERISTICS**

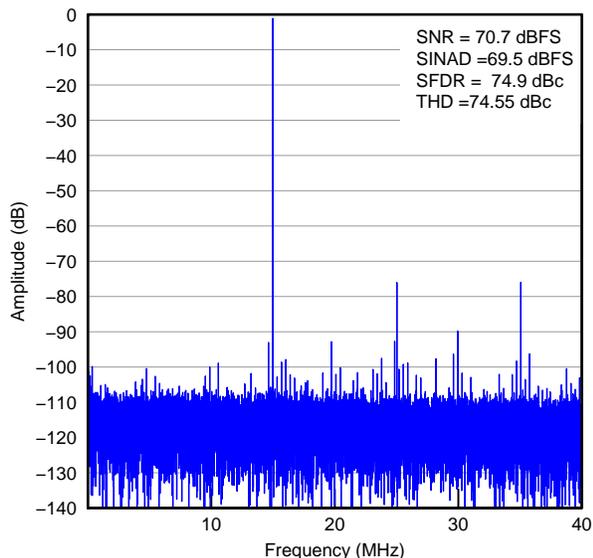
Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.



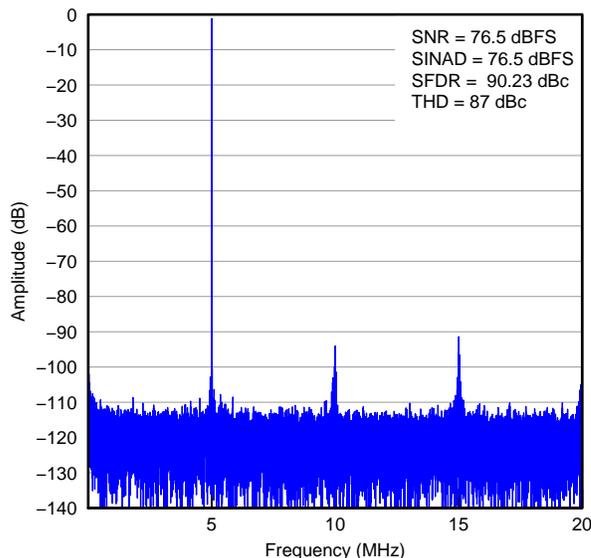
**Figure 8. FFT for 5 MHz Input Signal, Sample Rate = 80 MSPS**



**Figure 9. FFT for 15 MHz Input Signal, Sample Rate = 80 MSPS**



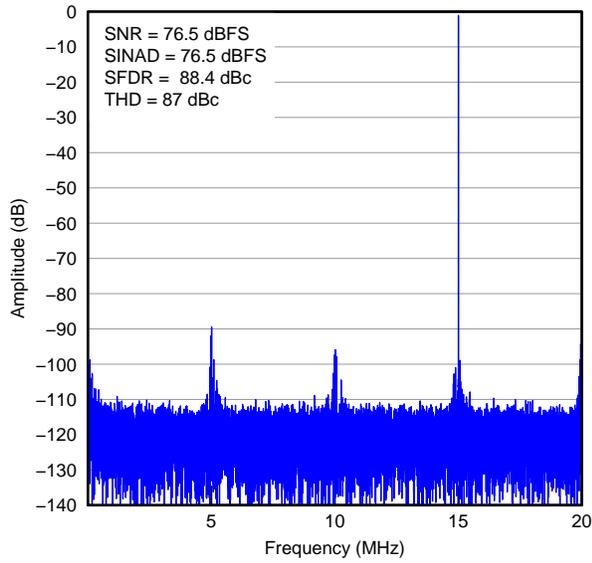
**Figure 10. FFT for 65 MHz Input Signal, Sample Rate = 80 MSPS**



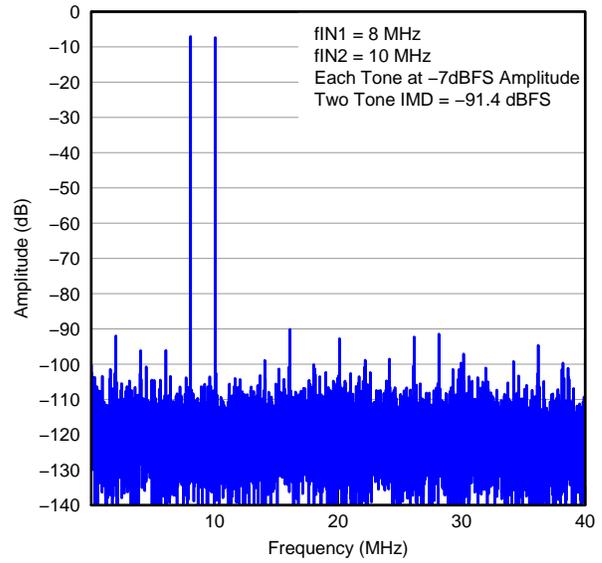
**Figure 11. FFT for 5 MHz Input Signal, Sample Rate = 40 MSPS**

**TYPICAL CHARACTERISTICS (continued)**

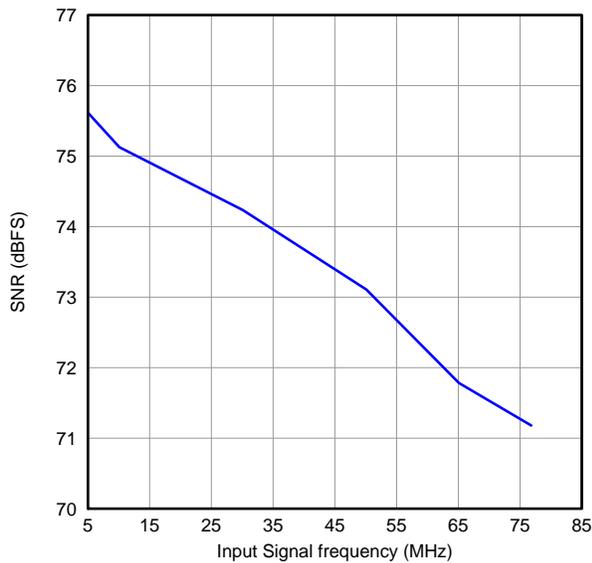
Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.



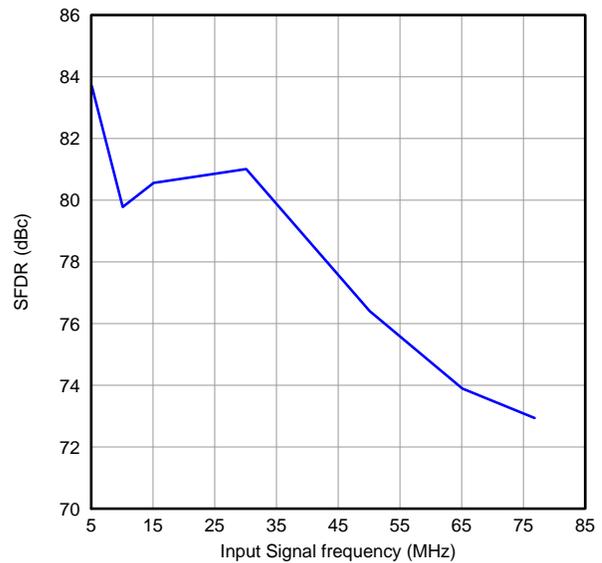
**Figure 12. FFT for 15 MHz Input Signal, Sample Rate = 40 MSPS**



**Figure 13. Two Tone Intermodulation**



**Figure 14. Signal To-Noise Ratio vs. Input Signal Frequency**



**Figure 15. Spurious-Free Dynamic Range vs. Input Signal Frequency**

**TYPICAL CHARACTERISTICS (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

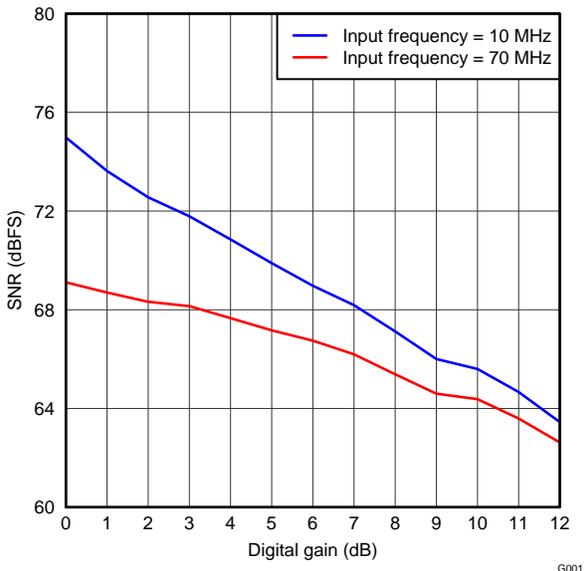


Figure 16. SNR vs. Digital Gain

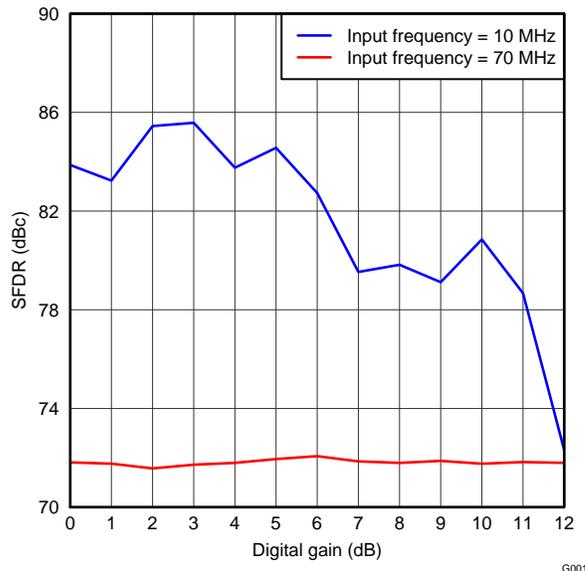


Figure 17. SFDR vs. Digital Gain

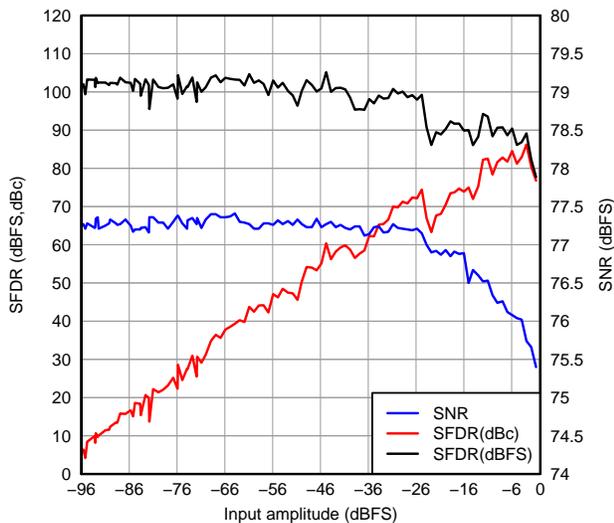


Figure 18. Performance vs. Input Amplitude

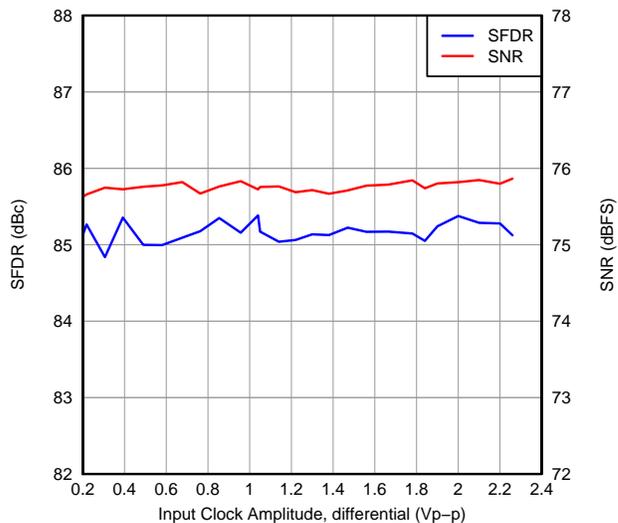


Figure 19. Performance vs. Clock Input Amplitudes

**TYPICAL CHARACTERISTICS (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

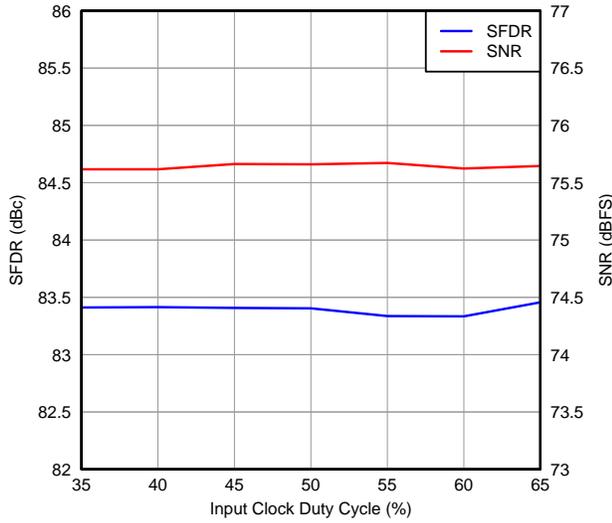


Figure 20. Performance vs. Input Clock Duty Cycle

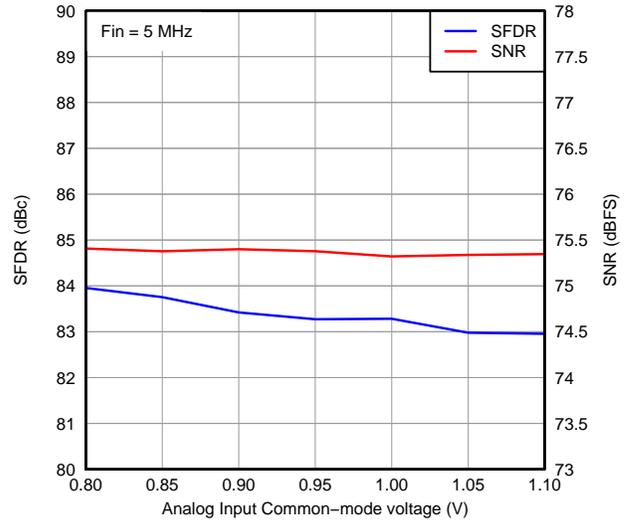


Figure 21. Performance vs. Input VCM

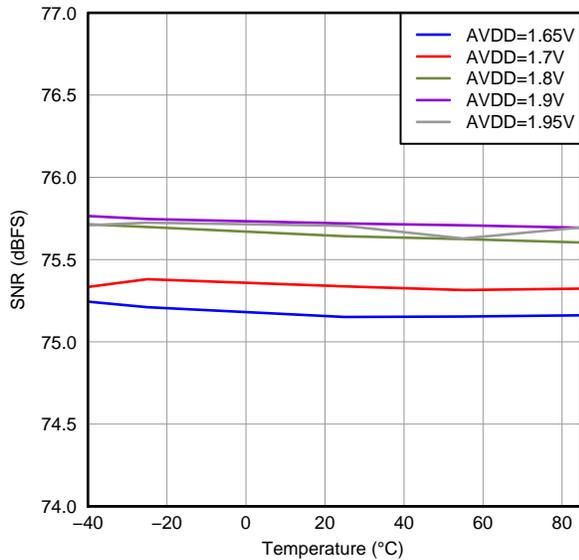


Figure 22. Signal -To-Noise Ratio vs. Temperature

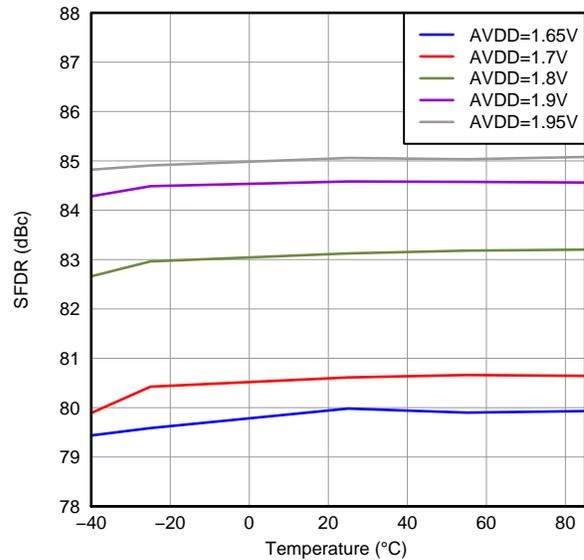


Figure 23. Spurious-Free Dynamic Range vs. Temperature

**TYPICAL CHARACTERISTICS (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

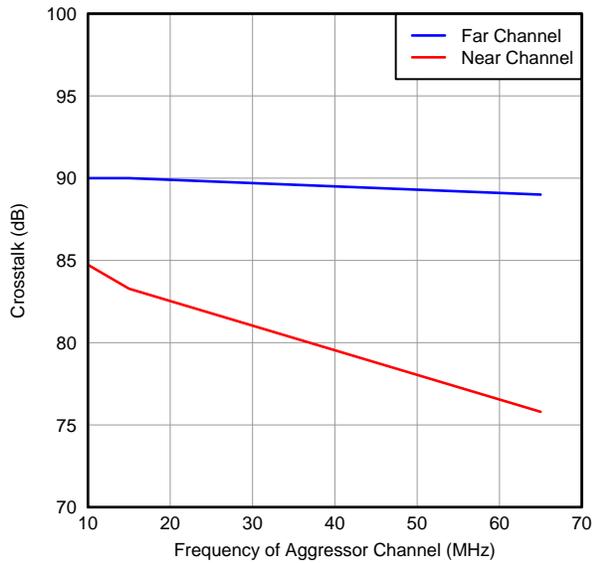


Figure 24. Crosstalk vs. Frequency

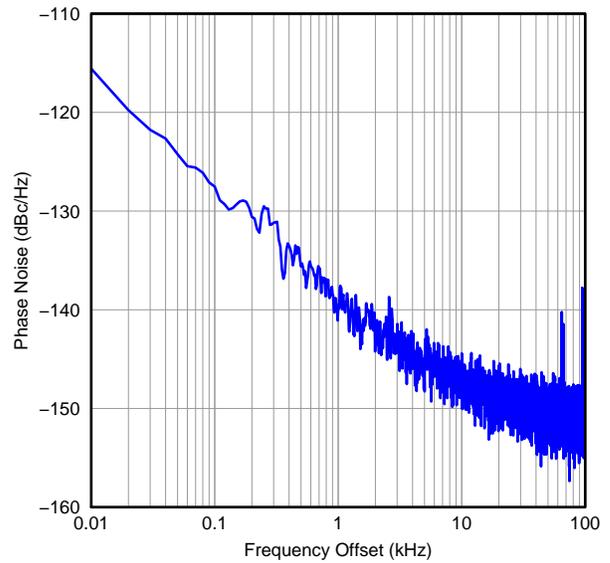


Figure 25. Phase Noise for 5 MHz Input Signal, Sample Rate = 80 MSPS

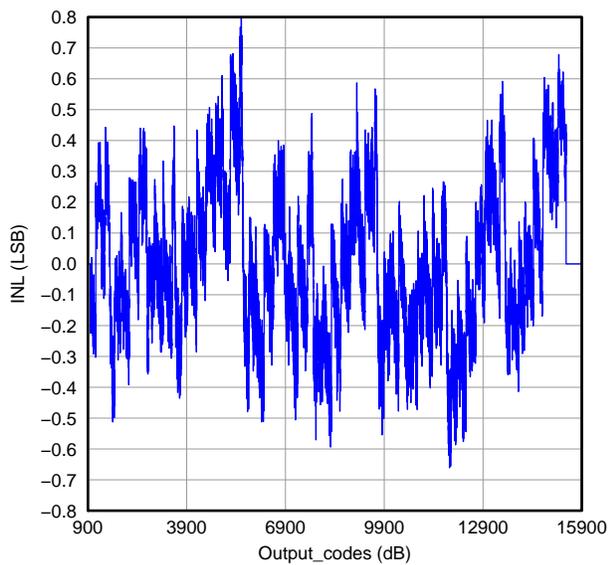


Figure 26. Integral Non-Linearity

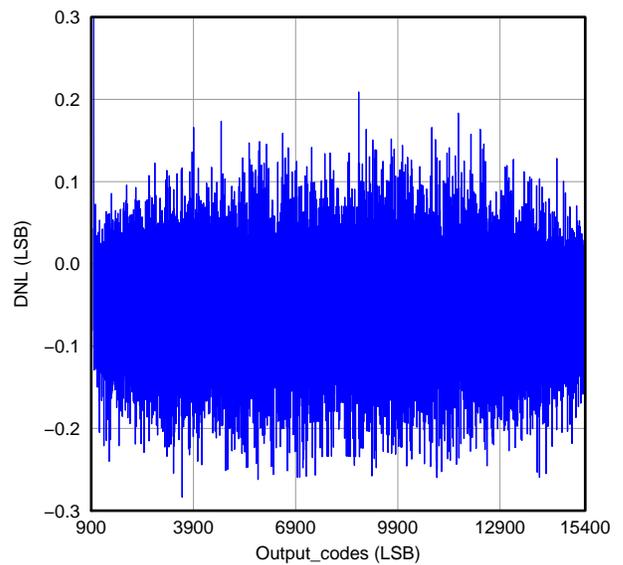


Figure 27. Differential Non-Linearity

**TYPICAL CHARACTERISTICS (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

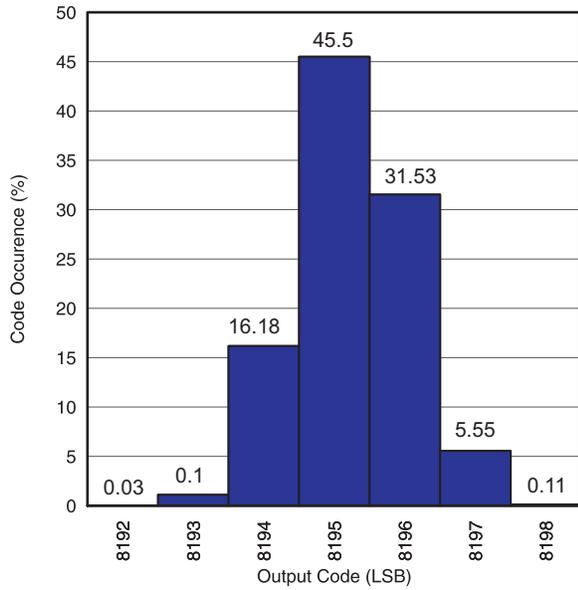


Figure 28. Histogram of Output Code with Analog Inputs Shorted

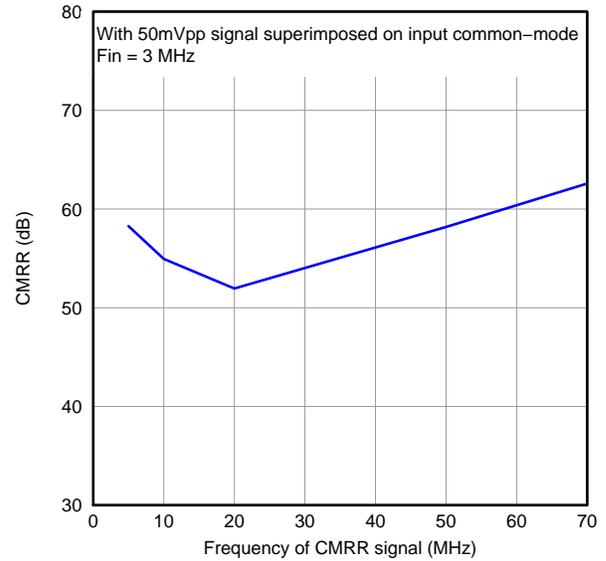


Figure 29. Common Mode Rejection Ratio vs. Frequency

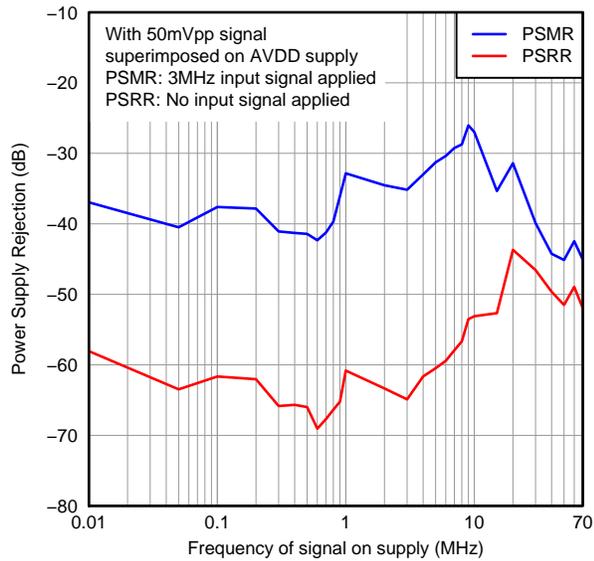


Figure 30. Power Supply Rejection Ratio vs. Frequency

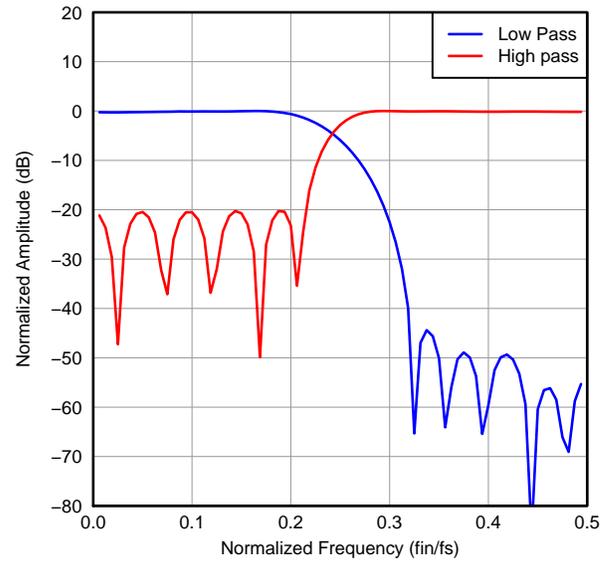


Figure 31. Filter Response, Decimate by 2

**TYPICAL CHARACTERISTICS (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

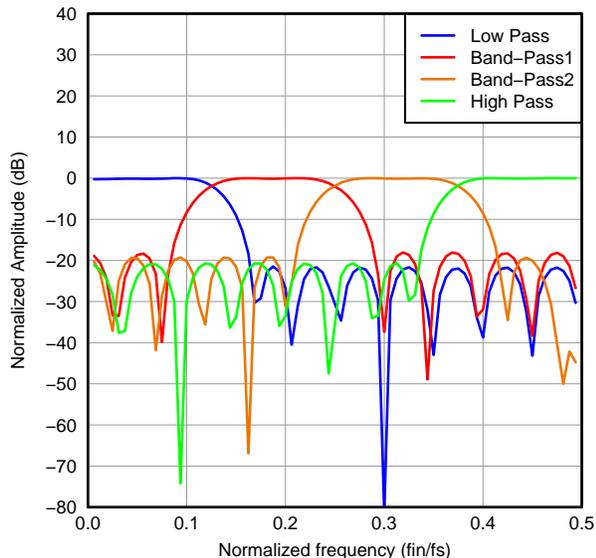


Figure 32. Filter Response, Decimate by 4

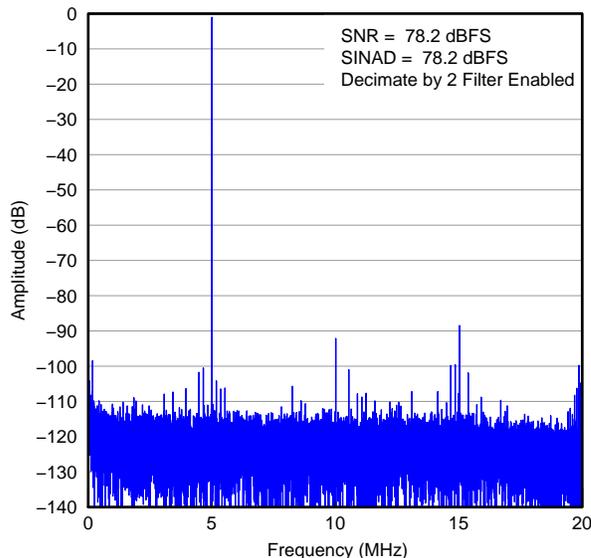


Figure 33. FFT for 5 MHz Input Signal, Sample Rate = 80 MSPS with Decimation Filter = 2

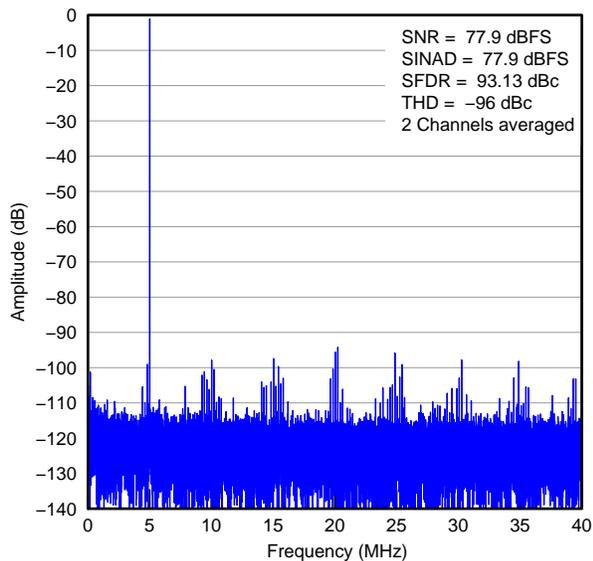


Figure 34. FFT for 5 MHz Input Signal, Sample Rate = 80 MSPS by Averaging 2 Channels

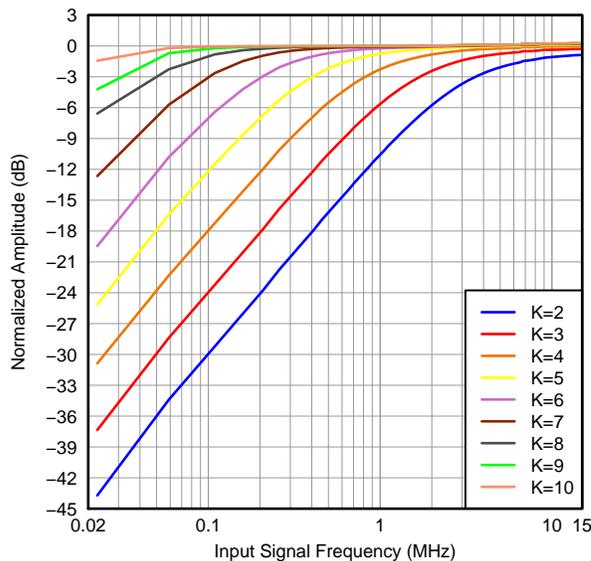


Figure 35. Digital High-Pass Filter Response

**TYPICAL CHARACTERISTICS (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

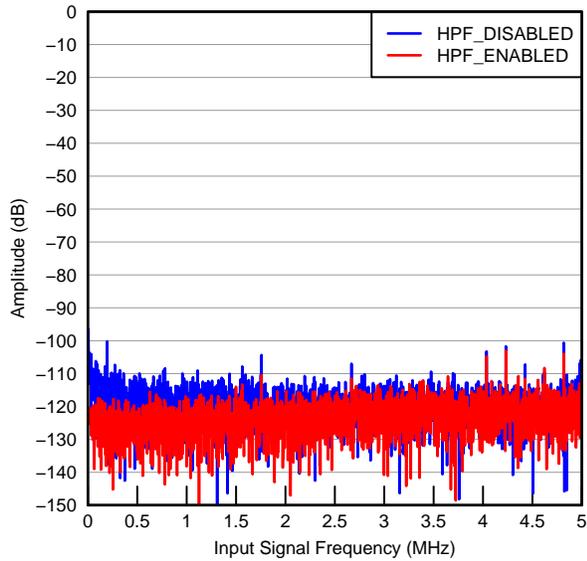


Figure 36. FFT with HPF Enabled and Disabled, No Signal

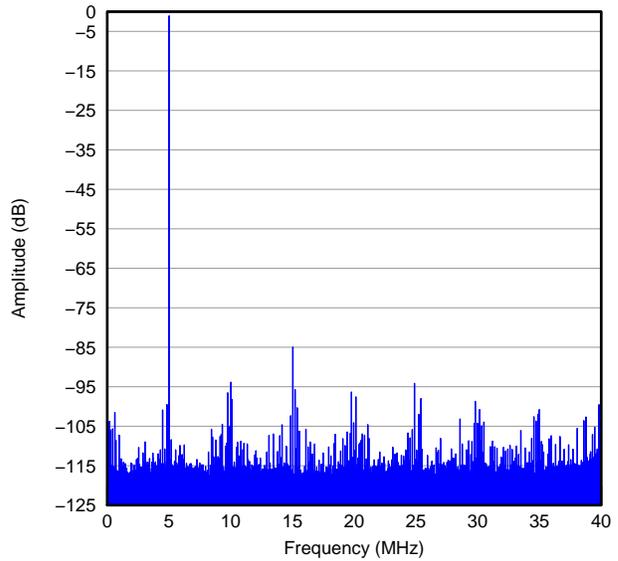


Figure 37. FFT (Full-Band) for 5 MHz Input Signal, Sample Rate = 80MSPS with Low Frequency Noise Suppression Enabled

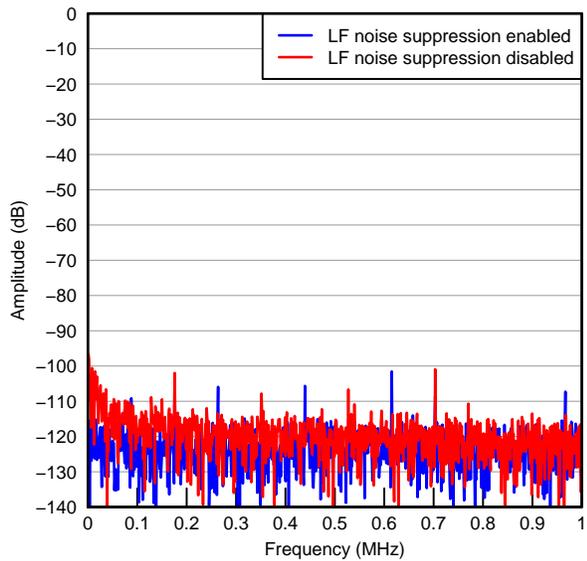


Figure 38. FFT (0 to 1 MHz) for 5 MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

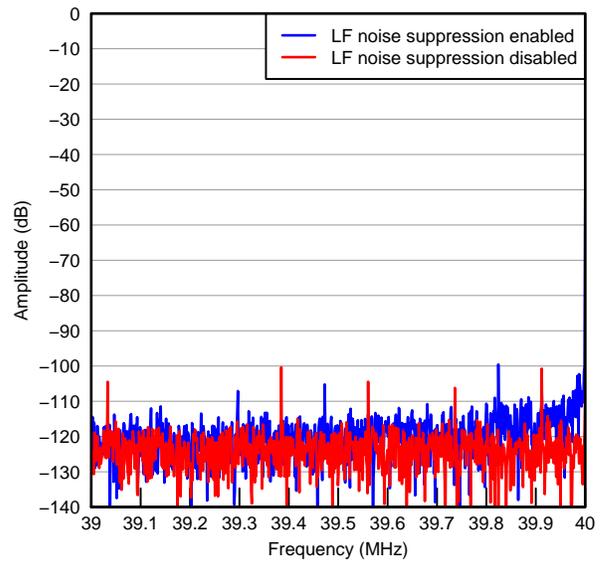


Figure 39. FFT (39 MHz to 40 MHz) for 5 MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

**TYPICAL CHARACTERISTICS (continued)**

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8V, 50% clock duty cycle, -1 dBFS differential analog input, 14 Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

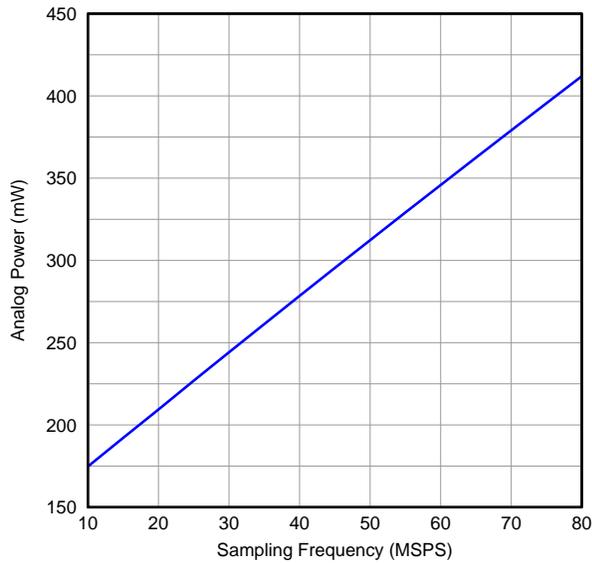


Figure 40. Power Consumption on Analog Supply

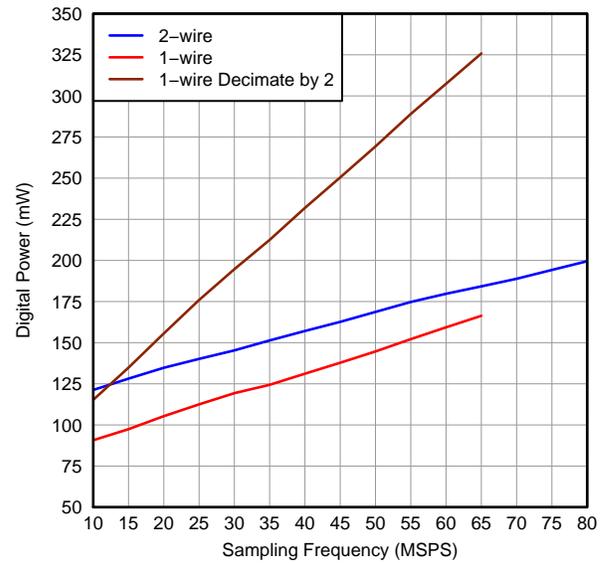


Figure 41. Power Consumption on Digital Supply

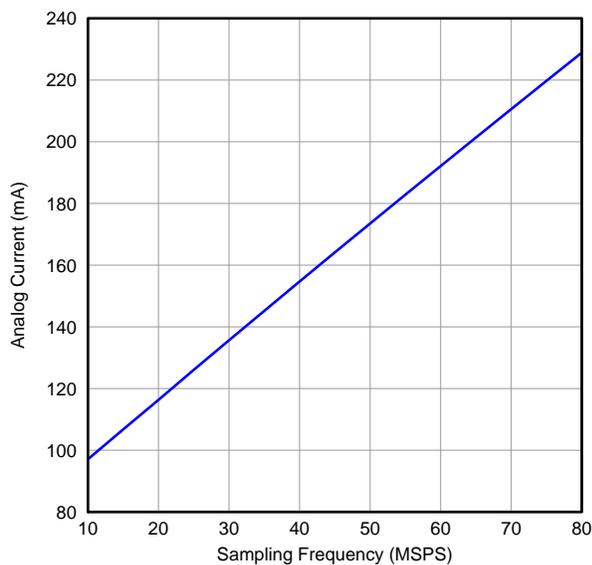


Figure 42. Supply Current on Analog Supply

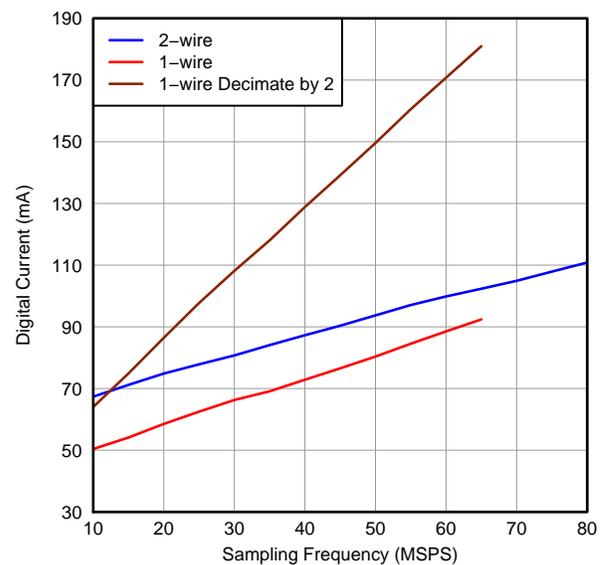


Figure 43. Supply Current on Digital Supply

## SERIAL INTERFACE

ADS5294 has a set of internal registers that can be accessed by the serial interface formed by pins CSZ (Serial interface Enable – Active Low), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

When CSZ is low,

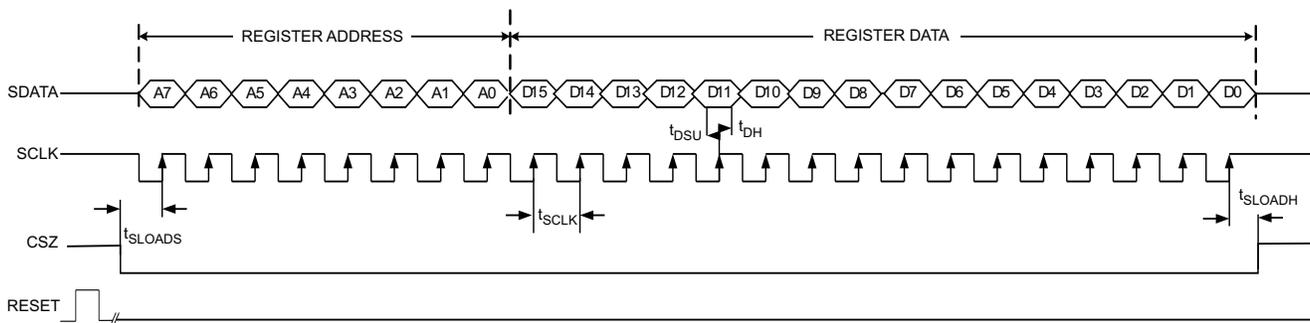
- Serial shift of bits into the device is enabled.
- Serial data (SDATA) is latched at every rising edge of SCLK.
- SDATA is loaded into the register at every 24<sup>th</sup> SCLK rising edge

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active CSZ pulse. The first eight bits form the register address and the remaining 16 bits the register data. The interface can work with SCLK frequencies from 15 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

### Register Initialization

After power-up, the internal registers must be initialized to the respective default values. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a high pulse on the RESET pin; or
2. Through a software reset; using the serial interface, set the RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the bit low. In this case, the RESET pin stays low (inactive).



**Figure 44. Serial Interface Timing**

### SERIAL INTERFACE TIMING CHARACTERISTICS

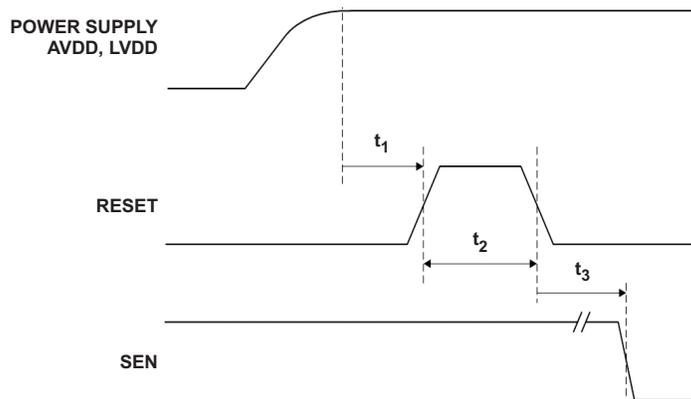
Typical values at 25°C, MIN and MAX values across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  $AVDD = 1.8\text{ V}$ ,  $LVDD = 1.8\text{ V}$ , unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
$f_{SCLK}$	SCLK frequency (= $1/t_{SCLK}$ )	> DC	15		MHz
$t_{SLOADS}$	$\overline{CS}$ to SCLK setup time	33			ns
$t_{SLOADH}$	SCLK to $\overline{CS}$ hold time	33			ns
$t_{DS}$	SDATA setup time	33			ns
$t_{DH}$	SDATA hold time	33			ns

**RESET TIMING**

Typical values at 25°C, MIN and MAX values across the full temperature range  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = 85^{\circ}C$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_1$	Power-on delay		1		ms
$t_2$	Reset pulse duration	50			ns
$t_3$	Register write delay		100		ns



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

**Figure 45. Reset Timing Diagram**

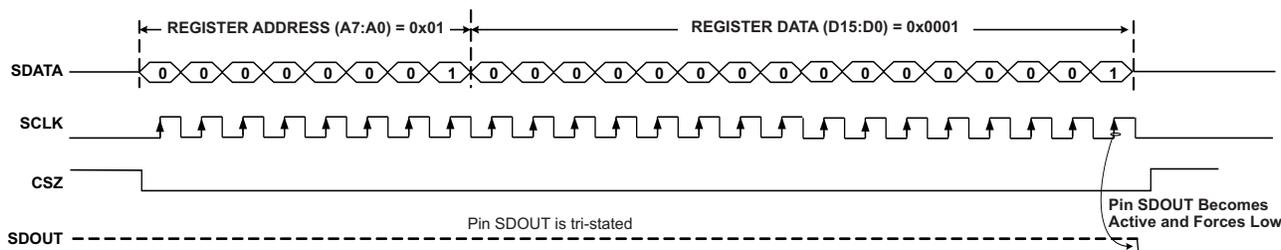
### Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back on SDOOUT pin. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

By default, after power up and device reset, the SDOOUT pin is in the high-impedance state. When the readout mode is enabled using the register bit <READOUT>, SDOOUT outputs the contents of the selected register serially, described as follows.

- Set register bit <READOUT> = 1 to put the device in serial readout mode. This disables any further writes into the internal registers, EXCEPT the register at address 1. Note that the <READOUT> bit itself is also located in register 1.  
The device can exit readout mode by writing <READOUT> to 0.  
Only the contents of register at address 1 cannot be read in the register readout mode.
- Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content is to be read.
- The device serially outputs the contents (D15–D0) of the selected register on the SDOOUT pin.
- The external controller can latch the contents at the rising edge of SCLK.
- To exit the serial readout mode, reset register bit <READOUT> = 0, which enables writes into all registers of the device. At this point, the SDOOUT pin enters the high-impedance state.

A) Enable Serial Readout (<READOUT> = 1)



B) Read Contents of Register 0x0F.  
This Register has been Initialized with 0x0200  
(The Device was earlier put in global power down)

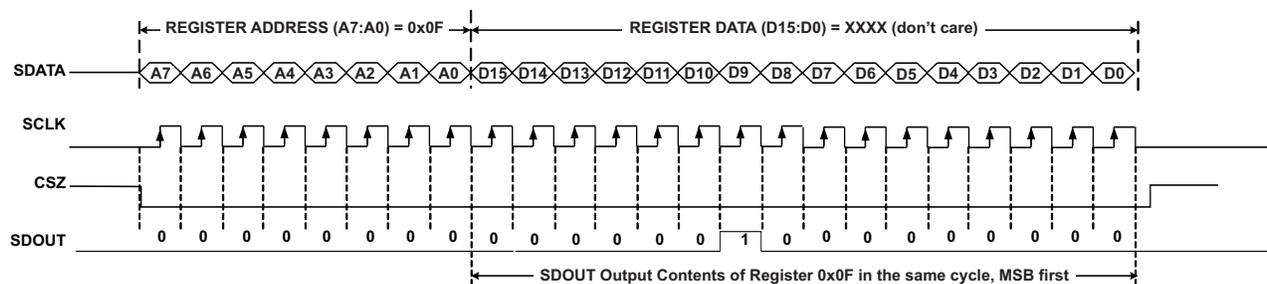


Figure 46. Serial Readout Timing

## DEFAULT STATES AFTER RESET

- Device is in normal operation mode with 14-bit ADC enabled for all channels.
- Output interface is 1-wire, 14× serialization with 7×bit clock and 1×frame clock frequency
- Serial readout is disabled
- PDN pin is configured as global power-down pin
- Digital gain is set to 0 dB.
- Digital modes such as LFNS, digital filters, and etc., are disabled.

## Register Map

**Table 3. Summary of Functions Supported by Serial Interface <sup>(1)(2)(3)(4)</sup>**

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
00																X	RST	1: Self-clearing software RESET; . After reset, this bit is set to 0 0: Normal operation.
01																X	EN_READOUT	1: READOUT of registers mode;0: Normal operation
02			X														EN_SYNC	1:Enable SYNC feature to synchronize multiple chips for lower rate output and to synchronize the test patterns; 0: Normal operation, SYNC feature is disabled. Note: this bit needs to be set as 1 when software or hardware SYNC feature is used. see Reg.0x25[8] and 0x25[15]
0A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RAMP_PAT_RESET_VAL	Ramp pattern reset value
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>	1:Channel-specific ADC power-down mode; 0: Normal operation
								X									PDN_PARTIAL	1:Partial power-down mode - fast recovery from power-down; 0: Normal operation
							X										PDN_COMPLETE	1:Register mode for complete power-down - slower recovery; 0: Normal operation
						X											PDN_PIN_CFG	1:Configures PD pin for partial power-down mode; 0:Configures PD pin for complete power-down mode
	X																EN_EXT_REF	1: Enable external reference mode, the voltage reference can be applied on either REFP/B pins or VCM pin. 0: Default: internal reference mode.
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>	1: Channel-specific low frequency noise suppression mode enable; 0: LFNS disabled
1C		X															EN_FRAME_PAT	1: Enables output frame clock to be programmed through a pattern; 0: Normal operation on frame clock
			X	X	X	X	X	X	X	X	X	X	X	X	X	X	ADCLKOUT<13:0>	14-bit pattern for frame clock on ADCLKP/ADCLKN pins
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>	PRBS pattern starting seed value lower 16 bits
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>	1: Swaps the polarity of the analog input pins electrically; 0: Normal configuration
	X	X	X	X	X	X	X										PRBS_SEED<22:16>	PRBS seed starting value upper 7 bits

- (1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.
- (2) X = Register bit referenced by the corresponding name and description
- (3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.
- (4) Multiple functions in a register can be programmed in a single write operation.

**Table 3. Summary of Functions Supported by Serial Interface <sup>(1)(2)(3)(4)</sup> (continued)**

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
25										X	0	0					EN_RAMP	1: Enables a repeating full scale ramp pattern on the outputs; 0: Normal operation
										0	X	0					DUALCUSTOM_PAT	1: Enables mode wherein output toggles between 2 defined codes; 0: Normal operation
										0	0	X					SINGLE_CUSTOM_PAT	1: Enables mode wherein output is a constant specified code; 0: Normal operation
															X	X	BITS_CUSTOM1<13:12>	2 MSBs for single custom pattern (and for the first code of the dual custom patterns)
														X	X		BITS_CUSTOM2<13:12>	2 MSBs for second code of the dual custom patterns
									X								TP_SOFT_SYNC	1: Software sync bit for Test patterns on all 8 CHs; 0: No sync
					X												PRBS_TP_EN	1: PRBS test pattern enable bit; 0: PRBS test pattern disabled
				X													PRBS_MODE_2	PRBS 9 bit LFSR (23bit LFSR is default)
		X															PRBS_SEED_FROM_REG	1: Enable PRBS seed to be chosen from register 0x23 and 0x24; 0: Disabled
	X															HARD_SYNC_TP	1: Enable the external SYNC feature for syncing test patterns. 0: Inactive	
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>	12 lower bits for single custom pattern (and for the first code of the dual custom pattern).
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>	12 lower bits for second code of the dual custom pattern
28	X																EN_BITORDER	Enables the bit order output. 0 = Byte wise, 1 = Word wise
	0																BIT_WISE	Selects between bitwise and bit wise 1: bit-wise, odd bits come out on one wire and even bits come out on other wire 0: byte-wise, upper bits on one wire and lower bits on other wire 1 = bit-wise, odd bits come out on one wire and even bits come out on other wire Note: D15 must be set to '0' for this mode
	1														X	X	EN_WORDWISE_BY_CH<7:0>	1: Output format is one sample on one LVDS wire and next sample on other LVDS wire. 0: Data comes out in two-wire mode with upper set of bits on one channel and lower set of bits on the other. Note: D15 must set '1' for this mode.
29															X		GLOBAL_EN_FILTER	1: Enables filter blocks - global control; 0: Inactive
																X	EN_CHANNEL_AVG	1: Enables channel averaging mode; 0: Inactive
2A													X	X	X	X	GAIN_CH1<3:0>	Programmable gain - Channel 1
									X	X	X	X					GAIN_CH2<3:0>	Programmable gain - Channel 2
					X	X	X	X									GAIN_CH3<3:0>	Programmable gain - Channel 3
	X	X	X	X													GAIN_CH4<3:0>	Programmable gain - Channel 4
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain - Channel 5
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain - Channel 6
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain - Channel 7
										X	X	X	X				GAIN_CH8<3:0>	Programmable gain - Channel 8

**Table 3. Summary of Functions Supported by Serial Interface <sup>(1)(2)(3)(4)</sup> (continued)**

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION				
2C						X	X										AVG_CTRL4<1:0>	1: Averaging control for what comes out on LVDS output OUT4				
									X	X							AVG_CTRL3<1:0>	Averaging control for what comes out on LVDS output OUT3				
												X	X				AVG_CTRL2<1:0>	Averaging control for what comes out on LVDS output OUT2				
															X	X	AVG_CTRL1<1:0>	Averaging control for what comes out on LVDS output OUT1				
2D						X	X										AVG_CTRL8<1:0>	Averaging control for what comes out on LVDS output OUT8				
									X	X							AVG_CTRL7<1:0>	Averaging control for what comes out on LVDS output OUT7				
											X	X					AVG_CTRL6<1:0>	Averaging control for what comes out on LVDS output OUT6				
														X	X		AVG_CTRL5<1:0>	Averaging control for what comes out on LVDS output OUT5				
2E							X	X	X								FILTER1_COEFF_SET<2:0>	Select stored coefficient set for filter 1				
										X	X	X					FILTER1_RATE<2:0>	Set decimation factor for filter 1				
														X			ODD_TAP1	Use odd tap filter 1				
				X	X	X	X											USE_FILTER1	1: Enables filter for channel 1; 0: Disables			
		X																HPF_CORNER_CH1	HPF corner in values k from 2 to 10			
2F							X	X	X									FILTER2_COEFF_SET<2:0>	Select stored coefficient set for filter 2			
										X	X	X						FILTER2_RATE<2:0>	Set decimation factor for filter 2			
														X				ODD_TAP2	Use odd tap filter 2			
				X	X	X	X												USE_FILTER2	1: Enables filter for channel 2; 0: Disables		
		X																	HPF_CORNER_CH2	HPF corner in values k from 2 to 10		
30							X	X	X										FILTER3_COEFF_SET<2:0>	Select stored coefficient set for filter 3		
										X	X	X							FILTER3_RATE<2:0>	Set decimation factor for filter 3		
														X					ODD_TAP3	Use odd tap filter 3		
				X	X	X	X													USE_FILTER3	1: Enables filter for channel 3; 0: Disables	
		X																		HPF_CORNER_CH3	HPF corner in values k from 2 to 10	
31							X	X	X											FILTER4_COEFF_SET<2:0>	Select stored coefficient set for filter 4	
										X	X	X								FILTER4_RATE<2:0>	Set decimation factor for filter 4	
														X						ODD_TAP4	Use odd tap filter 4	
				X	X	X	X									X					USE_FILTER4	1: Enables filter for channel 4; 0: Disables
		X																			HPF_CORNER_CH4	HPF corner in values k from 2 to 10
		X																			HPF_EN_CH4	1: HPF filter enabled for the channel; 0: Disabled

**Table 3. Summary of Functions Supported by Serial Interface <sup>(1)(2)(3)(4)</sup> (continued)**

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
32							X	X	X								FILTER5_COEFF_SET<2:0>	Select stored coefficient set for filter 5
										X	X	X					FILTER5_RATE<2:0>	Set decimation factor for filter 5
														X			ODD_TAP5	Use odd tap filter 5
				X	X	X	X									X	USE_FILTER5	1: Enables filter for channel 5; 0: Disables
	X																HPF_CORNER_CH5	HPF corner in values k from 2 to 10
33							X	X	X								FILTER_TYPE6<2:0>	Select stored coefficient set for filter 6
										X							DECBY8_6	Enables decimate by 8 filter 6
											X	X					FILTER_MODE6<1:0>	Set decimation factor for filter 6
														X			ODD_TAP6	Use odd tap filter 6
				X	X	X	X									X	USE_FILTER6	Enables filter for channel 6
34	X																HPF_CORNER_CH6	HPF corner in values k from 2 to 10
																	HPF_EN_CH6	Hpf filter enable for the channel
							X	X	X								FILTER_TYPE7<2:0>	Select stored coefficient set for filter 7
										X							DECBY8_7	Enables decimate by 8 filter 7
											X	X					FILTER_MODE7<1:0>	Set decimation factor for filter 7
35														X			ODD_TAP7	Use odd tap filter 7
															X		USE_FILTER7	Enables filter for channel 7
				X	X	X	X										HPF_CORNER_CH7	HPF corner in values k from 2 to 10
	X																HPF_EN_CH7	Hpf filter enable for the channel
							X	X	X								FILTER_TYPE8<2:0>	Select stored coefficient set for filter 8
38										X							DECBY8_8	Enables decimate by 8 filter 8
											X	X					FILTER_MODE8<1:0>	Set decimation factor for filter 8
														X			ODD_TAP8	Use odd tap filter 8
																X	USE_FILTER8	1: Enables filter for channel 8; 0: Disables
				X	X	X	X										HPF_CORNER_CH8	HPF corner in values k from 2 to 10
42	X														X	X	EXT_REF_VCM	Drive external reference mode through: D15=D3=1: the VCM pin; D15=D3=0: REFT/REFB pins. Note: 0xF[15] should be set as '1' to enable the external reference mode
										X	X						PHASE_DDR<1:0>	Controls phase of LCLK output relative to data
45															0	X	PAT_DESKEW	1: Enable deskew pattern mode; 0: Inactive
															X	0	PAT_SYNC	1: Enable sync pattern mode; 0: Inactive

**Table 3. Summary of Functions Supported by Serial Interface <sup>(1)(2)(3)(4)</sup> (continued)**

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
46	1															X	EN_2WIRE	1: 2 wire LVDS output; 0: 1 wire LVDS output
	1													X			BTC_MODE	1: 2's complement; (ADC data output format) 0: Binary Offset (ADC data output format)
	1												X				MSB_FIRST	1: MSB First; 0: LSB First
	1										X						EN_SDR	1:SDR Bit Clock; 0: DDR Bit Clock
	1					0	0	X									EN_12BIT	1: Enable 12 bit serialization mode; 0: Inactive
	1					0	X	0									EN_14BIT	1: Enable 14 bit serialization mode; 0: Inactive
	1					X	0	0									EN_16BIT	1: Enable 16 bit serialization mode; 0: Inactive
			X														FALL_SDR	1: Controls LCLK rising or falling edge comes in the middle of data window when operating in SDR output mode; 0: At the edge of data window.
50	1												X	X	X	X	MAP_Ch1234_to_OUT1A	OUT1A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT1B	OUT1B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT2A	OUT2A Pin pair to channel data mapping selection
51	1												X	X	X	X	MAP_Ch1234_to_OUT2B	OUT2B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT3A	OUT3A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT3B	OUT3B Pin pair to channel data mapping selection
52	1												X	X	X	X	MAP_Ch1234_to_OUT4A	OUT4A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT4B	OUT4B Pin pair to channel data mapping selection
53	1												X	X	X	X	MAP_Ch5678_to_OUT5B	OUT5B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT5A	OUT5A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT6B	OUT6B Pin pair to channel data mapping selection
54	1												X	X	X	X	MAP_Ch5678_to_OUT6A	OUT6A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT7B	OUT7B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT7A	OUT7A Pin pair to channel data mapping selection
55	1												X	X	X	X	MAP_Ch5678_to_OUT8B	OUT8B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT8A	OUT8A Pin pair to channel data mapping selection

## DESCRIPTION OF SERIAL REGISTERS

### POWER-DOWN MODES

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>
								X									PDN_PARTIAL
							X										PDN_COMPLETE
						X											PDN_PIN_CFG

Each of the 8 channels can be individually powered down. PDN\_CH<N> controls the power-down mode for ADC channel <N>. In addition to channel-specific power-down, the ADS5294 also has two global power-down modes:

1. The partial power-down mode. It partially powers down the chip; recovery time from the partial power-down mode is about 10  $\mu$ s provided that the clock has been running for at least 50  $\mu$ s before exiting this mode.
2. The complete power-down mode. It completely powers down the chip, and involves a much longer recovery time 100  $\mu$ s.

In addition to programming the chip in either of these two power-down modes (through either the PDN\_PARTIAL or PDN\_COMPLETE bits), the PD pin itself can be configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN\_PIN\_CFG=0 (default), when the PD pin is high, the device enters complete power-down mode. However, if PDN\_PIN\_CFG=1, when the PD pin is high, the device enters partial power-down mode.

### LOW FREQUENCY NOISE SUPPRESSION MODE

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>

The low frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the frequency band of 0 to 1 MHz (around DC). Setting this mode shifts the low-frequency noise of the ADS5294 to approximately  $F_s/2$ , thereby, moving the noise floor around DC to a much lower value. LFNS\_CH<8:1> enables this mode individually for each channel. See [Figure 38](#) and [Figure 39](#).

### ANALOG INPUT INVERT

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>

Normally,  $IN_P$  pin represents the positive analog input pin, and  $INN$  represents the complementary negative input. Setting the bits marked  $INVERT\_CH<8:1>$  (individual control for each channel) causes the inputs to be swapped.  $IN_N$  now represents the positive input, and  $IN_P$  the negative input.

## LVDS TEST PATTERNS

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>	
24	X	X	X	X	X	X	X										PRBS_SEED<22:16>	
										X	0	0					EN_RAMP	
										0	X	0					DUALCUSTOM_PAT	
										0	0	X					SINGLE_CUSTOM_PAT	
25															X	X	BITS_CUSTOM1<13:12>	
													X	X			BITS_CUSTOM2<13:12>	
								X									TP_SOFT_SYNC	
				X														PRBS_TP_EN
			X															PRBS_MODE_2
		X																PRBS_SEED_FROM_REG
	X																	HARD_SYNC_TP
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>	
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>	
45															0	X	PAT_DESKEW	
															X	0	PAT_SYNC	

The ADS5294 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. All these patterns can be synchronized across devices by the sync function either through the hardware SYNC pin or the software sync bit  $TP\_SOFT\_SYNC$  bit in register 0x25.  $HARD\_SYNC\_TP$  bit when set enables the Test patterns to be synchronized by the hardware SYNC Pin. When the software sync bit  $TP\_SOFT\_SYNC$  bit is set, special timing is needed.

- Setting  $EN\_RAMP$  to 1 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full scale code, it returns back to zero code and ramps again.
- The device can also be programmed to output a constant code by setting  $SINGLE\_CUSTOM\_PAT$  to 1, and programming the desired code in  $BITS\_CUSTOM1<13:0>$ . In this mode,  $BITS\_CUSTOM1<13:0>$  take the place of the 14-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes the same way as normal ADC data are.
- The device may also be made to toggle between two consecutive codes, by programming  $DUAL\_CUSTOM\_PAT$  to 1. The two codes are represented by the contents of  $BITS\_CUSTOM1<13:0>$  and  $BITS\_CUSTOM2<13:0>$ .
- In addition to custom patterns, the device may also be made to output two preset patterns:
  - Deskew patten** – Set using  $PAT\_DESKEW$ , this mode replaces the 14-bit ADC output  $D<13:0>$  with the 01010101010101 word.
  - Sync pattern** – Set using  $PAT\_SYNC$ , the normal ADC word is replaced by a fixed 11111110000000 word.
  - PRBS patterns:** The device can give 9 bit or 23 bit LFSR Pseudo random pattern on the channel outputs that are controlled by the register 0x25. To enable the PRBS pattern  $PRBS\_TP\_EN$  bit in the register 0x25 needs to be set. Default is the 23 bit LFSR but 9 bit LFSR can be chosen by setting  $PRBS\_MODE\_2$  bit. The seed value for the PRBS patterns can be chosen by enabling the  $PRBS\_SEED\_FROM\_REG$  bit to 1 and the value written to the  $PRBS\_SEED$  registers in 0x24 and 0x23.

**Note that only one of the above patterns should be active at any given instant.**

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## PROGRAMMABLE DIGITAL GAIN

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A													X	X	X	X	GAIN_CH1<3:0>
									X	X	X	X					GAIN_CH2<3:0>
					X	X	X	X									GAIN_CH3<3:0>
	X	X	X	X													GAIN_CH4<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

In applications where the full scale swing of the analog input signal is much less than the  $2 V_{PP}$  range supported by the ADS5294, a programmable gain can be set to achieve the full-scale output code even with a lower analog input swing. The programmable gain for each channel can be individually set using a set of four bits, indicated as GAIN\_CHN<3:0> for Channel N. The gain setting is coded in binary from 0-12 dB as shown in [Table 4](#).

**Table 4. Gain Setting for Channel N**

GAIN_CHN<3>	GAIN_CHN<2>	GAIN_CHN<1>	GAIN_CHN<0>	CHANNEL N GAIN SETTING
0	0	0	0	0 dB
0	0	0	1	1 dB
0	0	1	0	2 dB
0	0	1	1	3 dB
0	1	0	0	4 dB
0	1	0	1	5 dB
0	1	1	0	6 dB
0	1	1	1	7 dB
1	0	0	0	8 dB
1	0	0	1	9 dB
1	0	1	0	10 dB
1	0	1	1	11 dB
1	1	0	0	12 dB
1	1	0	1	Do not use
1	1	1	0	Do not use
1	1	1	1	Do not use

## CHANNEL AVERAGING

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29																X	EN_CHANNEL_AVG
2C						X	X										AVG_CTRL4<1:0>
									X	X							AVG_CTRL3<1:0>
											X	X					AVG_CTRL2<1:0>
														X	X		AVG_CTRL1<1:0>
2D						X	X										AVG_CTRL8<1:0>
									X	X							AVG_CTRL7<1:0>
											X	X					AVG_CTRL6<1:0>
														X	X		AVG_CTRL5<1:0>

In the default mode of operation, the LVDS outputs <8..1> contain the data of the ADC Channels <8..1>. By setting the EN\_CHANNEL\_AVG bit to '1', the outputs from multiple channels can be averaged. The resulting outputs from the Channel averaging block (which is bypassed in the default mode) are referred to as Bins. The contents of the Bins <8..1> come out on the LVDS outputs <8..1>. The contents of each of the 8 bins are determined by the register bits marked AVG\_CTRLn<1:0> where n stands for the Bin number. The different settings are shown below:

<b>AVG_CTRL1&lt;1&gt;</b>	<b>AVG_CTRL1&lt;0&gt;</b>	<b>Contents of Bin 1</b>
0	0	Zero
0	1	ADC Channel 1
1	0	Average of ADC Channel 1, 2
1	1	Average of ADC Channel 1, 2, 3, 4
<b>AVG_CTRL2&lt;1&gt;</b>	<b>AVG_CTRL2&lt;0&gt;</b>	<b>Contents of Bin 2</b>
0	0	Zero
0	1	ADC Channel 2
1	0	ADC Channel 3
1	1	Average of ADC Channel 3, 4
<b>AVG_CTRL3&lt;1&gt;</b>	<b>AVG_CTRL3&lt;0&gt;</b>	<b>Contents of Bin 3</b>
0	0	Zero
0	1	ADC Channel 3
1	0	ADC Channel 2
1	1	Average of ADC Channel 1, 2
<b>AVG_CTRL4&lt;1&gt;</b>	<b>AVG_CTRL4&lt;0&gt;</b>	<b>Contents of Bin 4</b>
0	0	Zero
0	1	ADC Channel 4
1	0	Average of ADC Channel 3, 4
1	1	Average of ADC Channel 1, 2, 3, 4
<b>AVG_CTRL5&lt;1&gt;</b>	<b>AVG_CTRL5&lt;0&gt;</b>	<b>Contents of Bin 5</b>
0	0	Zero
0	1	ADC Channel 5
1	0	Average of ADC Channel 5, 6
1	1	Average of ADC Channel 5, 6, 7, 8
<b>AVG_CTRL6&lt;1&gt;</b>	<b>AVG_CTRL6&lt;0&gt;</b>	<b>Contents of Bin 6</b>
0	0	Zero
0	1	ADC Channel 6
1	0	ADC Channel 7
1	1	Average of ADC Channel 7, 8
<b>AVG_CTRL7&lt;1&gt;</b>	<b>AVG_CTRL7&lt;0&gt;</b>	<b>Contents of Bin 7</b>
0	0	Zero
0	1	ADC Channel 7
1	0	ADC Channel 6
1	1	Average of ADC Channel 6, 5
<b>AVG_CTRL8&lt;1&gt;</b>	<b>AVG_CTRL8&lt;0&gt;</b>	<b>Contents of Bin 8</b>
0	0	Zero
0	1	ADC Channel 8
1	0	Average of ADC Channel 7, 8
1	1	Average of ADC Channel 5, 6, 7, 8

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When the contents of a particular bin is set to Zero, then the LVDS buffer corresponding to that bin gets automatically powered down.

## DECIMATION FILTER

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29															X		GLOBAL_EN_FILTER
2E							X	X	X								FILTER1_COEFF_SET<2:0>
										X	X	X					FILTER1_RATE<2:0>
														X			ODD_TAP1
2F																X	USE_FILTER1
							X	X	X								FILTER2_COEFF_SET<2:0>
										X	X	X					FILTER2_RATE<2:0>
30														X			ODD_TAP2
							X	X	X							X	USE_FILTER2
							X	X	X								FILTER3_COEFF_SET<2:0>
31										X	X	X					FILTER3_RATE<2:0>
							X	X	X								ODD_TAP3
										X	X	X					FILTER4_COEFF_SET<2:0>
32														X			FILTER4_RATE<2:0>
							X	X	X								ODD_TAP4
							X	X	X							X	USE_FILTER4
33																	FILTER5_COEFF_SET<2:0>
							X	X	X								FILTER5_RATE<2:0>
										X	X	X					ODD_TAP5
34																X	USE_FILTER5
							X	X	X								FILTER6_COEFF_SET<2:0>
										X	X	X					FILTER6_RATE<2:0>
35														X			ODD_TAP6
							X	X	X								USE_FILTER6
							X	X	X								FILTER7_COEFF_SET<2:0>
36										X	X	X					FILTER7_RATE<2:0>
														X			ODD_TAP7
							X	X	X								USE_FILTER7
37																	FILTER8_COEFF_SET<2:0>
							X	X	X								FILTER8_RATE<2:0>
														X			ODD_TAP8
															X		USE_FILTER8

The decimation filter is implemented as 24-tap FIR with symmetrical coefficients (each coefficient is 12-bit signed). The filter equation is:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times [(h_0 \times x(n) + h_1 \times x(n-1) + h_2 \times x(n-2) + \dots + h_{11} \times x(n-11) + h_{11} \times x(n-12) + \dots + h_1 \times x(n-22) + h_0 \times x(n-23)] \quad (1)$$

By setting the register bit <ODD\_TAPn> = 1, a 23-tap FIR is implemented:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times [(h_0 \times x(n) + h_1 \times x(n-1) + h_2 \times x(n-2) + \dots + h_{10} \times x(n-10) + h_{11} \times x(n-11) + h_{10} \times x(n-12) + \dots + h_1 \times x(n-21) + h_0 \times x(n-22)] \quad (2)$$

In Equation 1 and Equation 2,  $h_0, h_1 \dots h_{11}$  are 12 bit signed representation of the coefficients,  $x(n)$  is the input data sequence to the filter and  $y(n)$  is the filter output sequence.

A decimation filter can be introduced at the output of each channel. To enable this feature, the

GLOBAL\_EN\_FILTER should be set to '1'. Setting this bit to '1' increases the overall latency of each channel to 20 clock cycles irrespective of whether the filter for that particular channel has been chosen or not (using the USE\_FILTER bit). The bits marked FILTER $n$ \_COEFF\_SET<2:0>, FILTER $n$ \_RATE<2:0>, ODD\_TAP $n$  and USE\_FILTER $n$  represent the controls for the filter for Channel  $n$ . Note that these bits are functional only when the GLOBAL\_EN\_FILTER gets set to '1'. For illustration, the controls for channel 1 are listed in [Table 5](#):

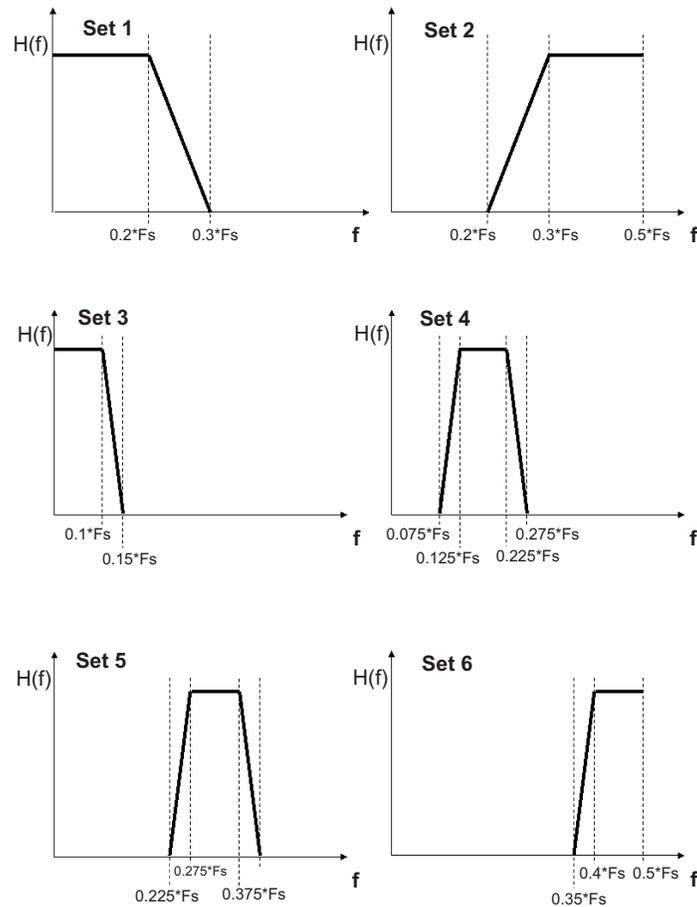
The USE\_FILTER1 bit determines whether the filter for Channel 1 is used or not. When this bit is set to '1', the filter for channel 1 is enabled. When this bit is set to '0', the filter for channel 1 is disabled but the channel data passes through a dummy delay so that the overall latency of channel 1 is 20 clock cycles. With the USE\_FILTER1 bit set to '1', the characteristics of the filter can be set by using the other sets of bits.

The ADS5294 has 6 sets of filter coefficients stored in memory. Each of these sets define a unique pass band in the frequency domain and contain 12 coefficients (each coefficient is 12-bit long). These 12 coefficients are used to implement either a symmetric 24-tap (even-tap) filter, or a symmetric 23-tap (odd-tap) filter. Setting the register bit ODD\_TAP1 to '1' enables the odd-tap configuration (the default is even tap with this bit set to '0') for Channel 1. The bits FILTER1\_COEFF\_SET<2:0> can be used to choose the required set of coefficients for Channel 1.

**Table 5.**

FILTER1_COEFF_SET<2>	FILTER1_COEFF_SET<1>	FILTER1_COEFF_SET<0>	CHOICE OF FILTER COEFFICIENT SET
0	0	0	Set 1
0	0	1	Set 2
0	1	0	Set 3
0	1	1	Set 4
1	0	0	Set 5
1	0	1	Set 6

The passbands corresponding to of each of these filter coefficient sets is shown in [Figure 47](#)



**Figure 47. Filter Types**

Coefficient Sets 1 and 2 are the most appropriate when Decimation by a factor of 2 is required, whereas Coefficient Sets 3,4,5,6 are appropriate when Decimation by a factor of 4 is desired. The computation rate of the filter output can be independently set using the bits FILTERn\_RATE<2:0>. The settings are shown in [Table 6](#).

**Table 6.**

FILTER_MODE1<2>	FILTER_MODE1<1>	FILTER_MODE1<0>	CHOICE OF FILTER COEFFICIENT SET
0	0	0	Decimation by 2
0	0	1	Decimation by 4
0	1	0	Do not use
0	1	1	Do not use
1	0	0	Decimation by 8
1	0	1	Do not use
1	1	0	Do not use
1	1	1	Do not use

The choice of the odd/even tap setting, filter coefficient set and the filter rate uniquely determines the filter to be used. In addition to the preset filter coefficients, the coefficients for each of the eight filter channels can be programmed by the user. Each of the eight channels has 12 programmable coefficients, each 12-bit long. The 96 registers with addresses from 5A (Hex) to B9 (Hex) are used to program these 8 sets of 12 programmable coefficients. Registers 5A to 65 are used to program the 1<sup>st</sup> filter, with the 1<sup>st</sup> coefficient occupying the bits D11..D0 of register 5A, the 2<sup>nd</sup> coefficient occupying the bits D11..D0 of register 5B, and so on. Similarly registers 66(Hex) to 71(Hex) are used to program the 2<sup>nd</sup> filter, and so on.

When programming the filter coefficients, the D15 bit of each of the 12 registers corresponding to that filter should be set to '1'. If the D15 bit of these 12 registers is set to '0', then the preset coefficient (as programmed by FILTER<sub>n</sub>\_COEFF\_SET<2:0>) is used even if the bits D11..D0 get programmed. By setting or not setting the D15 bits of individual filter channels to '1', some filters can be made to operate with preset coefficient sets, and some others can be made to simultaneously operate with programmed coefficient sets.

## HIGH PASS FILTER

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2E			X	X	X	X											HPF_corner_CH1
2E		X															HPF_EN_CH1
2F			X	X	X	X											HPF_corner_CH2
2F		X															HPF_EN_CH2
30			X	X	X	X											HPF_corner_CH3
30		X															HPF_EN_CH3
31			X	X	X	X											HPF_corner_CH4
31		X															HPF_EN_CH4
32			X	X	X	X											HPF_corner_CH5
32		X															HPF_EN_CH5
33			X	X	X	X											HPF_corner_CH6
33		X															HPF_EN_CH6
34			X	X	X	X											HPF_corner_CH7
34		X															HPF_EN_CH7
35			X	X	X	X											HPF_corner_CH8
35		X															HPF_EN_CH8

This group of registers controls the characteristics of a digital high pass transfer function applied to the output data, using [Equation 3](#):

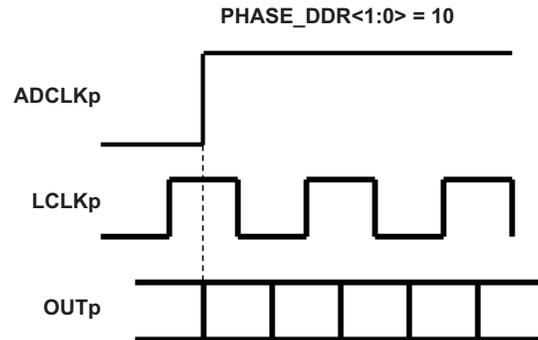
$$y(n) = \frac{2^k}{2^k+1} [x(n) - x(n-1) + y(n-1)] \quad (3)$$

Where k is set as described by the HPF\_corner registers (one for each channel). Also the HPF\_EN bit in each register needs to be set to enable the HPF feature for each channel.

## BIT CLOCK PROGRAMMABILITY

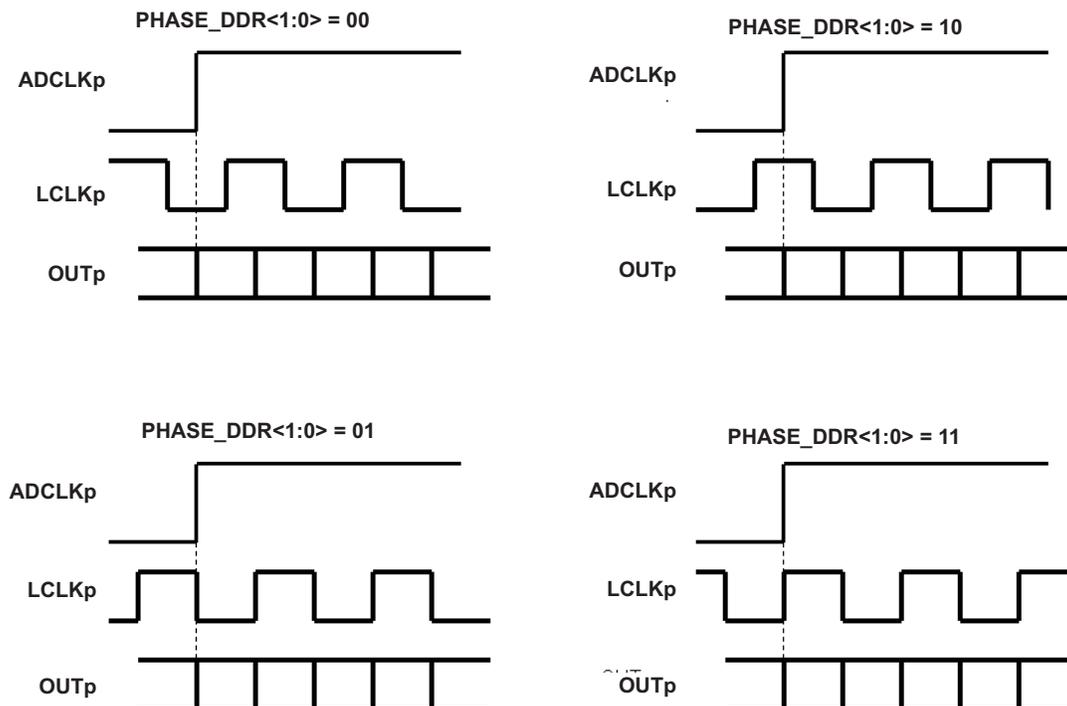
ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42										X	X						PHASE_DDR<1:0>
46	1											X					EN_SDR
46	1		X														FALL_SDR

The output interface of the ADS5294 is normally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. This default phase is shown in [Figure 48](#).



**Figure 48. Default Phase of LCLK**

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE\_DDR<1:0>. The LCLK phase modes are shown in [Figure 49](#).



**Figure 49. Phase Programmability Modes for LCLK**

In addition to programming the phase of the LCLK in the DDR mode, the device can also be made to operate in SDR mode by setting bit EN\_SDR to 1. In the mode, the bit clock (LCLK) is output at 14X times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL\_SDR, the LCLK may be output in either of the two manners shown in [Figure 50](#). As can be seen in [Figure 50](#), only the LCLK rising (or falling edge) is used to capture the output data in SDR mode. The SDR mode does not work well beyond 40 MSPS because the LCLK frequency will become very high.

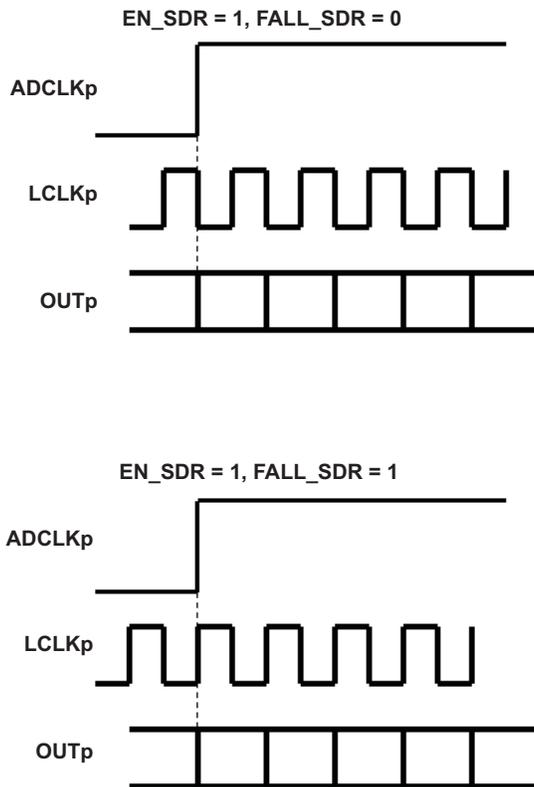


Figure 50. SDR Interface Modes

### OUTPUT DATA RATE CONTROL

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38															DATA_RATE<1>	DATA_RATE<0>

In the default mode of operation, the data rate at the output of the ADS5294 is at the sampling rate of the ADC. This is true even when the custom pattern generator is enabled. In addition, both output data rate and sampling rate can also be configured to a sub-multiple of the input clock rate.

With the DATA\_RATE<1:0> control, the output data rate can be programmed to be a sub-multiple of the ADC sampling rate. This feature can be used to lower the output data rate, for example when the decimation filter is used. Without enabling the decimation filter, the sub-multiple ADC sampling rate feature still can be used.

The different settings are listed below:

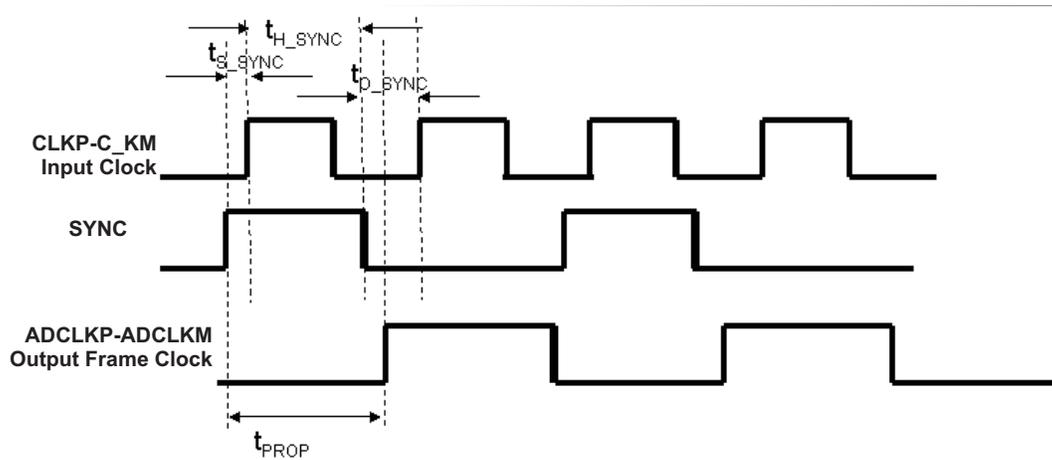
DATA_RATE<1>	DATA_RATE<0>	Output data rate
0	0	Same as ADC sampling rate
0	1	1/2 of ADC sampling rate
1	0	1/4 of ADC sampling rate
1	1	1/8 of ADC sampling rate

### SYNCHRONIZATION PULSE

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
25	HARD_SYNC_TP															
02			EN_SYNC													

While setting the data rate to a fraction of the ADC sampling rate, a synchronization pulse can be used to position the location of the output frame clock (and thereby output data). This is especially useful when there are multiple ADS5294 chips on the board, and a common output frame reference is desired for reducing the pin count in FPGA deserialization. The synchronization pulse is to be applied on the SYNC pin at the same rate as the desired (reduced) output data rate. To enable the use of the SYNC pulse, the EN\_SYNC (0x02[13]) and HARD\_SYNC\_TP(0x25[15]) should be programmed. The sync pulse can be used to synchronize the test patterns across multiple chips.

The timing diagram and characteristics for the synchronization pulse are shown below.



Timing Diagram for the Synchronization Pulse

**Figure 51. Synchronization Pulse**

## DATA OUTPUT FORMAT MODES

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
46	1													X			BTC_MODE
46	1												X				MSB_FIRST

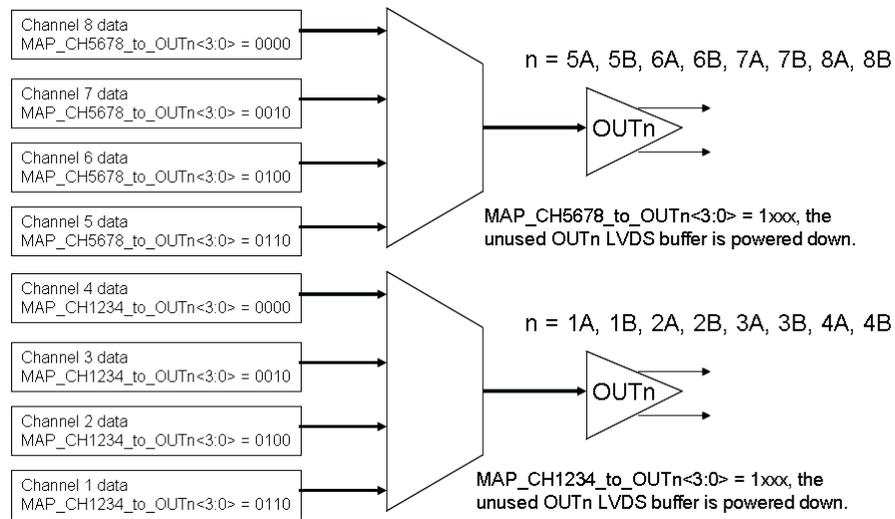
The ADC output, by default, is in Straight offset binary mode. Programming the BTC\_MODE bit to '1' inverts the MSB, and the output becomes Binary 2's complement mode. Also, by default, the first bit of the frame (following the rising edge of CLKP) is the LSB of the ADC output. Programming the MSB\_FIRST mode inverts the bit order in the word, and the MSB is output as the first bit following CLKP rising edge.

### PROGRAMMABLE MAPPING BETWEEN INPUT CHANNELS AND OUTPUT PINS

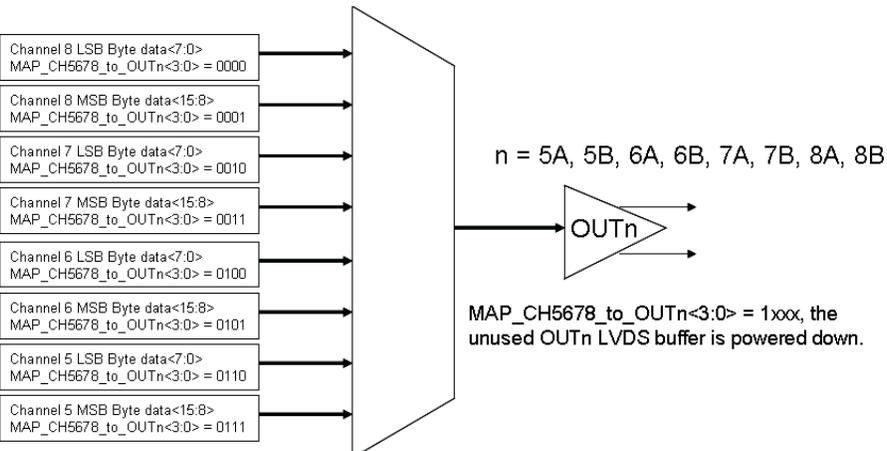
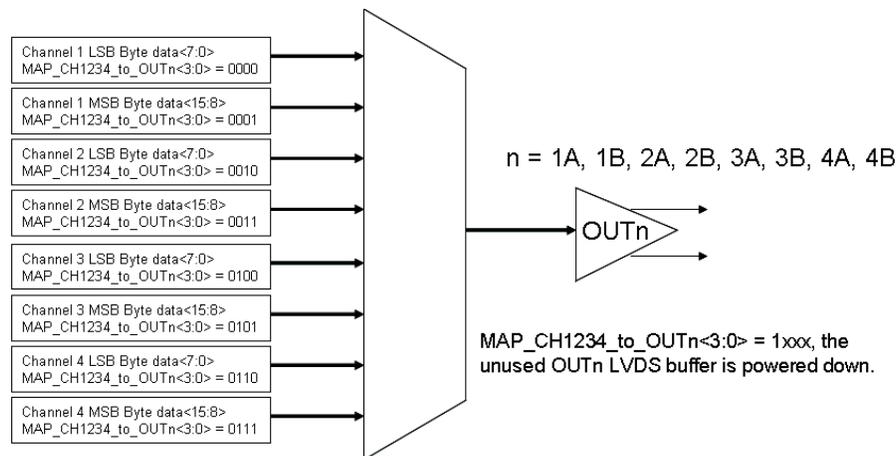
ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
50	1												X	X	X	X	MAP_CH1234_TO_OUT1A
	1								X	X	X	X					MAP_CH1234_TO_OUT1B
	1				X	X	X	X									MAP_CH1234_TO_OUT2A
51	1												X	X	X	X	MAP_CH1234_TO_OUT2B
	1								X	X	X	X					MAP_CH1234_TO_OUT3A
	1				X	X	X	X									MAP_CH1234_TO_OUT3B
52	1												X	X	X	X	MAP_CH1234_TO_OUT4A
	1								X	X	X	X					MAP_CH1234_TO_OUT4B
53	1												X	X	X	X	MAP_CH5678_TO_OUT5B
	1								X	X	X	X					MAP_CH5678_TO_OUT5A
	1				X	X	X	X									MAP_CH5678_TO_OUT6B
54	1												X	X	X	X	MAP_CH5678_TO_OUT6A
	1								X	X	X	X					MAP_CH5678_TO_OUT7B
	1				X	X	X	X									MAP_CH5678_TO_OUT7A
55	1												X	X	X	X	MAP_CH5678_TO_OUT8B
	1								X	X	X	X					MAP_CH5678_TO_OUT8A

The ADS5294 has 16 pairs of LVDS channel outputs. The mapping of ADC channels to LVDS output channels is programmable to allow for flexibility in board layout. The 16 LVDS channel outputs are split in to 2 groups of 8 LVDS pairs. Within each group 4 ADC input channels can be multiplexed in to the 8 LVDS pairs depending on the modes of operation whether it is 1 wire mode or 2 wire mode.

Input channels 1 to 4 can be mapped to any of the LVDS outputs OUT1A/B to OUT4A/B (using the MAP\_CH1234\_TO\_OUTnA/B). Similarly, input channels 5 to 8 can be mapped to any of the LVDS outputs OUT5A/B to OUT8A/B (using the MAP\_CH5678\_TO\_OUTnA/B). The block diagram of the mapping is listed in [Figure 52](#).



(a) 1-wire mode



(b) 2-wire mode

Figure 52. Input and Output Channel Mapping

Registers 0x50 to 0x55 control the multiplexing options as below:

MAP_CH1234_to_OUTn<3:0>	Mapping	Used in 1-wire mode?	Used in 2-wire mode?
0000	ADC input channel IN1 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN1 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN2 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN2 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN3 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN3 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN4 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN4 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

MAP_CH5678_to_OUTn<3:0>	Mapping	Used in 1-wire mode?	Used in 2-wire mode?
0000	ADC input channel IN8 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN8 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN7 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN7 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN6 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN6 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN5 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN5 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

The default mapping for 1-wire and 2-wire modes is:

**Table 7. Mapping for 1-wire Mode**

Analog Input channel	LVDS Output
Channel IN1	OUT1A
Channel IN2	OUT2A
Channel IN3	OUT3A
Channel IN4	OUT4A
Channel IN5	OUT5A
Channel IN6	OUT6A
Channel IN7	OUT7A
Channel IN8	OUT8A

Note: In the single wire mode with default register settings, ADC data is available only on OUTnA.

**Table 8. Mapping for 2-wire Mode**

Analog Input channel	LVDS Output
Channel IN1	OUT1A, OUT1B
Channel IN2	OUT2A, OUT2B
Channel IN3	OUT3A, OUT3B
Channel IN4	OUT4A, OUT4B
Channel IN5	OUT5A, OUT5B
Channel IN6	OUT6A, OUT6B
Channel IN7	OUT7A, OUT7B
Channel IN8	OUT8A, OUT8B

Note: In the 2-wire mode, the ADC data is available on both OUTnA (LSB bytes) and OUTnB (MSB bytes).

## APPLICATION INFORMATION

### THEORY OF OPERATION

The ADS5294 is an octal channel, 14-bit high-speed ADC with sample rate up to 80 MSPS that runs off a single 1.8 V supply. All eight channels of the ADS5294 simultaneously sample their analog inputs at the rising edge of the input clock. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock, edge the sample propagates through the pipeline resulting in a data latency of 11 clock cycles.

The 14 data bits of each channel are serialized and sent out in either 1-wire (one pair of LVDS pins are used) or 2-wire (two pairs of LVDS pins are used) mode, depending on the LVDS output rate. When the data is output in the 2-wire mode, it can reduce the serial data rate of the outputs, especially at higher sampling rates. Hence, low cost FPGAs can be used to capture 80 MSPS/14bit data. Alternately, at lower sample rates, the 14-bit data can be output as a single data stream over one pair of LVDS pins (1-wire mode). The device outputs a bit clock at 7x and frame clock at 1x times the sample frequency in the 14-bit mode.

This 14-bit ADC achieves approximately 76 dBFS SNR at 80 MSPS. Its output resolution can be configured as 12-bit and 10-bit if necessary. 70 dBFS and 61 dBFS SNRs are achieved when the ADS5294's output resolution is 12-bit and 10-bit respectively.

### ANALOG INPUT

The analog inputs consist of a switched-capacitor based, differential sample and hold architecture. This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins are internally biased around a common-mode voltage of  $V_{cm}$  (0.95 V). For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between  $V_{cm} + 0.5V$  and  $V_{cm} - 0.5V$ , resulting in a  $2 V_{pp}$  differential input swing. Figure 53 illustrates the equivalent circuit of the input sampling circuit.

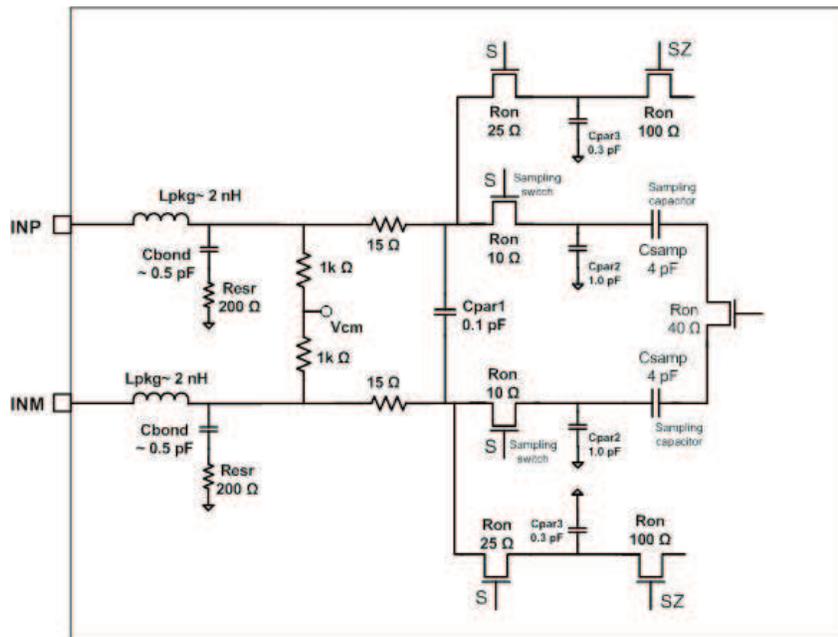
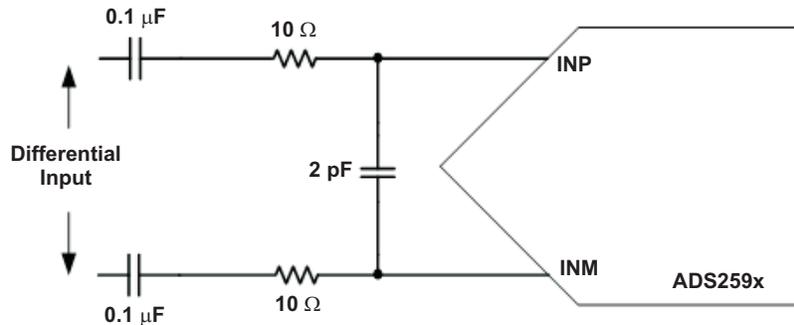


Figure 53. Analog Input Circuit Model

### DRIVE CIRCUIT

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A 5 Ω to 15 Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitic.

The drive circuit shows an R-C filter across the analog input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors.



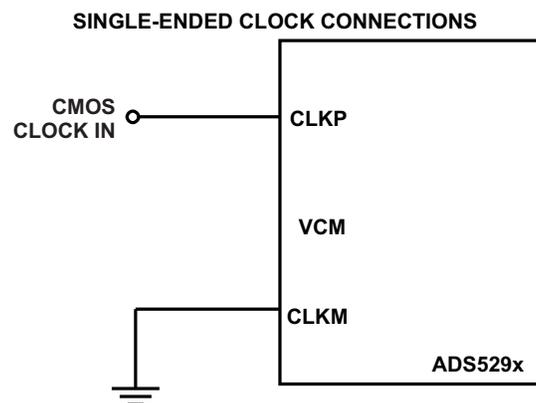
**Figure 54. Analog Input Drive Circuit**

### Large and Small Signal Input Bandwidth

The small signal bandwidth of the analog input circuit is high, around 550 MHz. When using an amplifier to drive the ADS5294, the total noise of the amplifier up to the small signal bandwidth must be considered. The large signal bandwidth of the device depends on the amplitude of the input signal. The ADS5294 supports  $2 V_{PP}$  amplitude for input signal frequency up to 80 MHz. For higher frequencies (80 MHz), the amplitude of the input signal must be decreased proportionally. For example, at 160 MHz, the device supports a maximum of  $1 V_{PP}$  signal.

### INPUT CLOCK

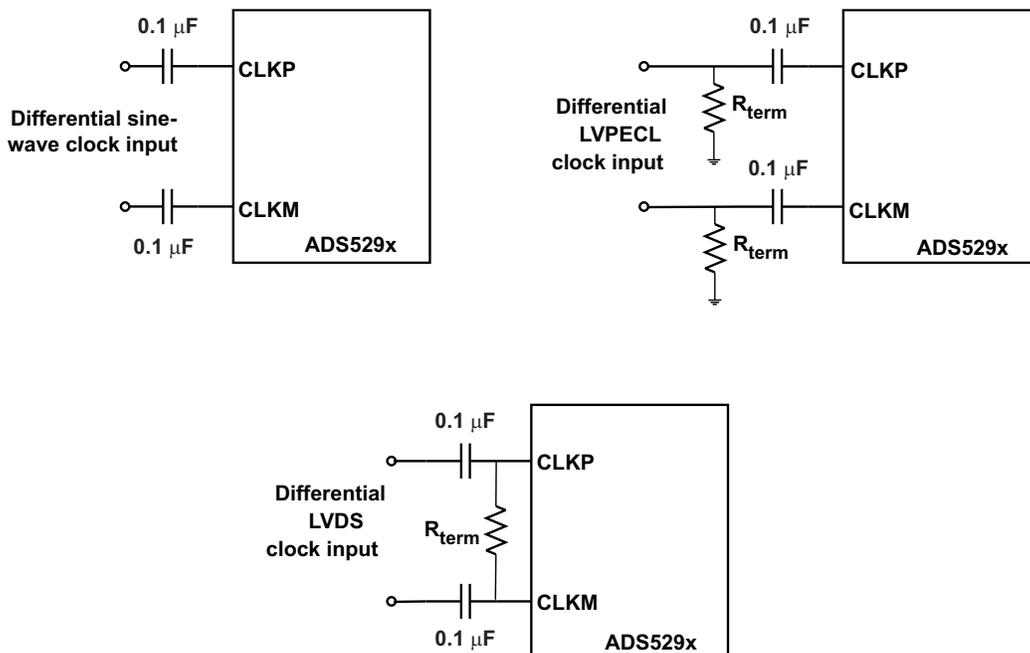
The ADS5294 is configured by default to operate with a single-ended input clock – CLKP is driven by a CMOS clock and CLKM is tied to GND. The device can automatically detect a single-ended or differential clock. If CLKM is grounded, the device treats clock as a single-ended clock. Operating with a low-jitter differential clock usually gives better SNR performance, especially at input frequencies greater than 30 MHz. Typical clock termination structures are listed in [Figure 55](#).



**Figure 55. Single-Ended Clock Drive Circuit**

## DIFFERENTIAL CLOCK CONNECTIONS

### DIFFERENTIAL CLOCK CONNECTIONS



## DIGITAL HIGH PASS IIR FILTER

DC offset is often observed at ADC input signals. For example, in ultrasound applications, the DC offset from VGA (variable Gain amplifier) varies at different gains. Such a variable offset can introduce artifacts in ultrasound images especially in Doppler modes. Analog filter between ADC and VGA can be used with added noise and power. Digital filter achieves the same performance as analog filters and has more flexibility in fine tuning multiple characteristics.

ADS5294 includes optional 1<sup>st</sup> order digital high-pass IIR filter. Its block diagram is shown in [Figure 56](#) as well as its transfer function

$$y(n) = \frac{2^k}{2^k+1} [x(n) - x(n-1) + y(n-1)] \quad (4)$$

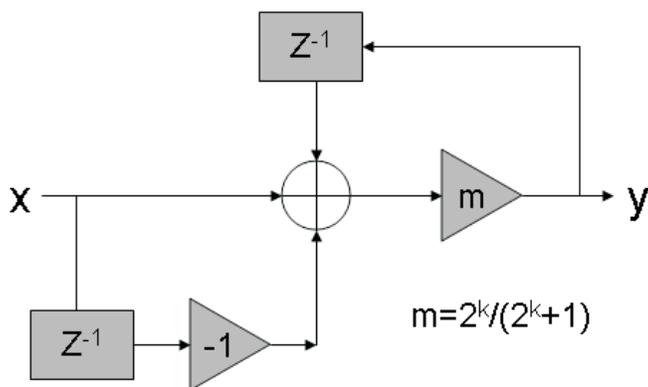


Figure 56. HP Filter Block Diagram

[Figure 57](#) shows its characteristics at k=2 to 10.

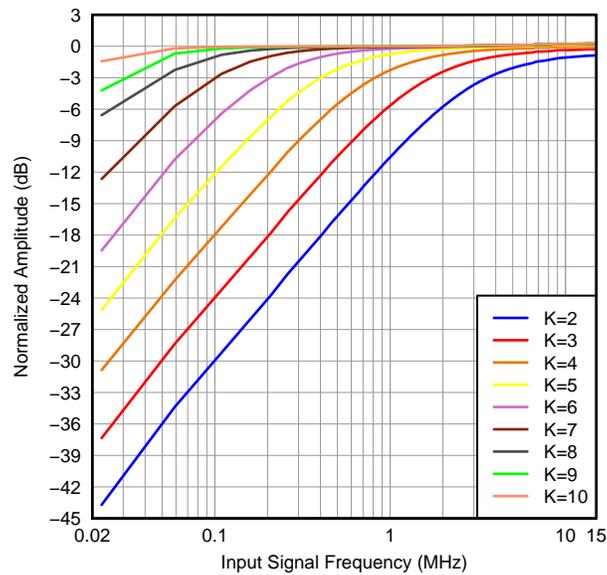


Figure 57. HP Filter Amplitude Response at K = 2 to 10

**DECIMATION FILTER**

ADS5294 includes an option to decimate the ADC output data using filters. Once the decimation is enabled, the decimation rate, frequency band of the filter can be programmed. In addition, the user can select either the pre-defined or custom coefficients.

**Table 9. Decimation Filter Modes**

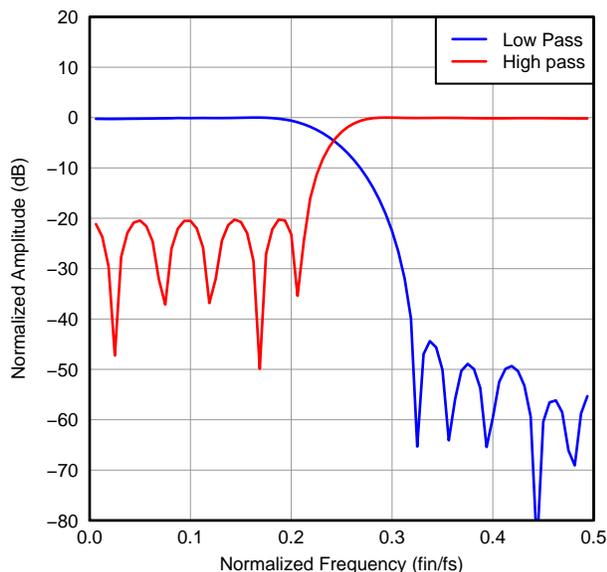
COMBINATION OF DECIMATION RATES and FILTER TYPES		SERIAL INTERFACE SETTINGS						
DECIMATION	TYPE OF FILTER	<DECIMATION RATE>			<DECIMATION FILTER FREQ BAND>		<FILTER COEFF SELECT>	<DECIMATION ENABLE>
Decimate by 2	Build-in low pass filter (pass band = 0 to Fs/4)	0	0	0	0	0	0	1
	Build-in high pass filter (pass band = Fs/4 to Fs/2)	0	0	0	0	1	0	1
Decimate by 4	Build-in low pass filter (pass band = 0 to Fs/8)	0	0	1	0	0	0	1
	Build-in 2nd band pass filter (pass band = Fs/8 to Fs/4)	0	0	1	0	1	0	1
	Build-in 3rd band pass filter (pass band = Fs/4 to 3Fs/8)	0	0	1	1	0	0	1
Decimate by 4	Build-in last band pass filter (pass band = 3Fs/8 to Fs/2)	0	0	1	1	1	0	1
Decimate by 2	Custom filter (user programmable coefficients)	0	0	0	X	X	1	1
Decimate by 4	Custom filter (user programmable coefficients)	0	0	1	X	X	1	1
Decimate by 8	Custom filter (user programmable coefficients)	1	0	0	X	X	1	1
No decimation	Custom filter (user programmable coefficients)	0	1	1	X	X	1	0

## DECIMATION FILTER EQUATION

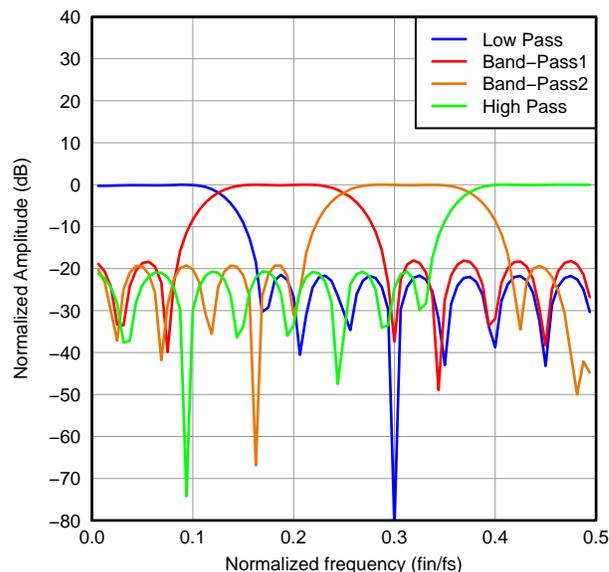
In the default setting, the decimation filter is implemented as a 24-tap FIR filter with symmetrical coefficients (each coefficient is 12-bit signed). By setting the register bit **<ODD TAPn>** = 1, a 23-tap FIR is implemented

### Pre-defined Coefficients

The build-in filters (low pass, high pass and band pass) use pre-defined coefficients. The frequency responses of the build-in decimation filters with different decimation factors are shown in [Figure 58](#).



**Figure 58. Decimation Filter Responses (Decimate by 2)**



**Figure 59. Decimation Filter Responses (Decimate by 4)**

### Custom Filter Coefficients

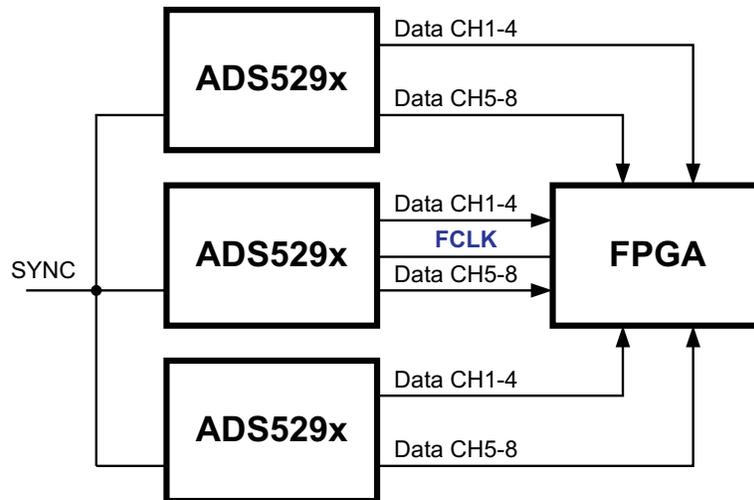
The filter coefficients can also be programmed by the user (customized). For custom coefficients, set the register bit **<FILTER COEFF SELECT>** and load the coefficients ( $h_0$  to  $h_{11}$ ) in registers 0x5A to 0xB9, using the serial interface as:

Register content = real coefficient value x 211, i.e., 12 bit signed representation of real coefficient.

### Synchronization Pulse

While using decimation filters, it may be required to synchronize the filters across multiple ADS5294s on the board. The ADS5294 has a SYNC pulse input pin that can be used to position the location of the output frame clock (and thereby output data) unambiguously for each chip.

The synchronization pulse has to be applied on the SYNC pin of every ADS5294 chip. The SYNC pulse should be at the same rate as the desired (reduced) output data rate. This ensures that the output data from all chips will be aligned. More information can be found in the register description section. A typical configuration is shown in [Figure 60](#).



**Figure 60. SYNC Pin Configuration**

## Board Design Considerations

### Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See *ADS5294VM Evaluation Module (SLAU355)* for placement of components, routing and grounding.

### Supply Decoupling

Because the ADS5294 already includes internal decoupling, minimal external decoupling can be used without loss in performance. For example, the ADS5294EVM uses a single 0.1  $\mu\text{F}$  decoupling capacitor for each supply, placed close to the device supply pins.

### Packaging

#### Exposed Pad

The exposed pad at the bottom of the package is the main path for heat dissipation. Therefore, the pad must be soldered to a ground plane on the PCB for best thermal performance. The pad must be connected to the ground plane through the optimum number of vias.

Also, visit TI's thermal website at [www.ti.com/thermal](http://www.ti.com/thermal).

## DEFINITION OF SPECIFICATIONS

**Analog Bandwidth** – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

**Aperture Delay** – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

**Aperture Uncertainty (Jitter)** – The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle** – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Maximum Conversion Rate** – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

**Minimum Conversion Rate** – The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL)** – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL)** – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error** – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as  $E_{GREF}$  and  $E_{GCHAN}$ .

To a first-order approximation, the total gain error is  $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$ .

For example, if  $E_{TOTAL} = \pm 0.5\%$ , the full-scale input varies from  $(1 - 0.5/100) \times FS_{ideal}$  to  $(1 + 0.5/100) \times FS_{ideal}$ .

**Offset Error** – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

**Temperature Drift** – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from  $T_{MIN}$  to  $T_{MAX}$ . It is calculated by dividing the maximum deviation of the parameter across the  $T_{MIN}$  to  $T_{MAX}$  range by the difference  $T_{MAX} - T_{MIN}$ .

**Signal-to-Noise Ratio** – SNR is the ratio of the power of the fundamental ( $P_S$ ) to the noise floor power ( $P_N$ ), excluding the power at dc and the first nine harmonics.

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (5)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**Signal-to-Noise and Distortion (SINAD)** – SINAD is the ratio of the power of the fundamental ( $P_S$ ) to the power of all the other spectral components including noise ( $P_N$ ) and distortion ( $P_D$ ), but excluding dc.

$$SINAD = 10 \log_{10} \frac{P_S}{P_N + P_D} \quad (6)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**Effective Number of Bits (ENOB)** – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (7)$$

**Total Harmonic Distortion (THD)** – THD is the ratio of the power of the fundamental ( $P_S$ ) to the power of the first nine harmonics ( $P_D$ ).

$$\text{THD} = 10\text{Log}^{10} \frac{P_S}{P_N} \quad (8)$$

THD is typically given in units of dBc (dB to carrier).

**Spurious-Free Dynamic Range (SFDR)** – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion** – IMD3 is the ratio of the power of the fundamental (at frequencies  $f_1$  and  $f_2$ ) to the power of the worst spectral component at either frequency  $2f_1 - f_2$  or  $2f_2 - f_1$ . IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**DC Power-Supply Rejection Ratio (DC PSRR)** – DC PSRR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

**AC Power-Supply Rejection Ratio (AC PSRR)** – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If  $\Delta V_{\text{SUP}}$  is the change in supply voltage and  $\Delta V_{\text{OUT}}$  is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{SUP}}} \quad (\text{Expressed in dBc}) \quad (9)$$

**Voltage Overload Recovery** – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

**Common-Mode Rejection Ratio (CMRR)** – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If  $\Delta V_{\text{CM\_IN}}$  is the change in the common-mode voltage of the input pins and  $\Delta V_{\text{OUT}}$  is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{CM}}} \quad (\text{Expressed in dBc}) \quad (10)$$

**Crosstalk (only for multi-channel ADCs)** – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

## REVISION HISTORY

Changes from Original (November 2011) to Revision A	Page
• Changed From: Product Preview To: Production .....	1

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
ADS5294IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS5294IPFPR	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS5294IPFPT	ACTIVE	HTQFP	PFP	80	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

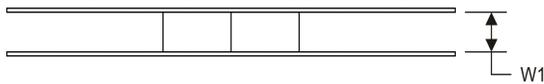
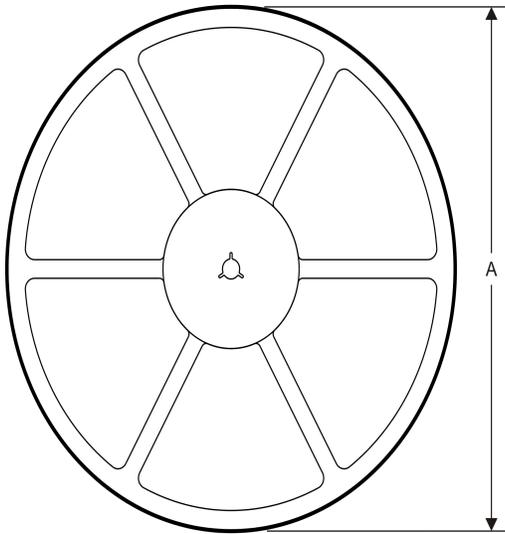
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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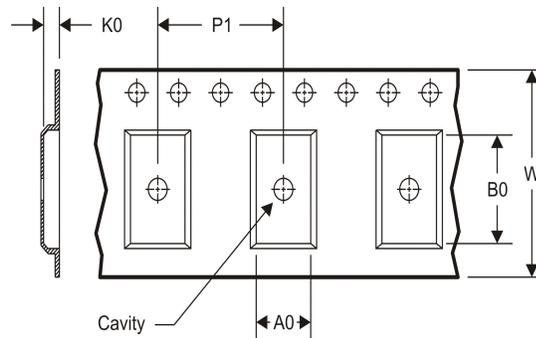
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**

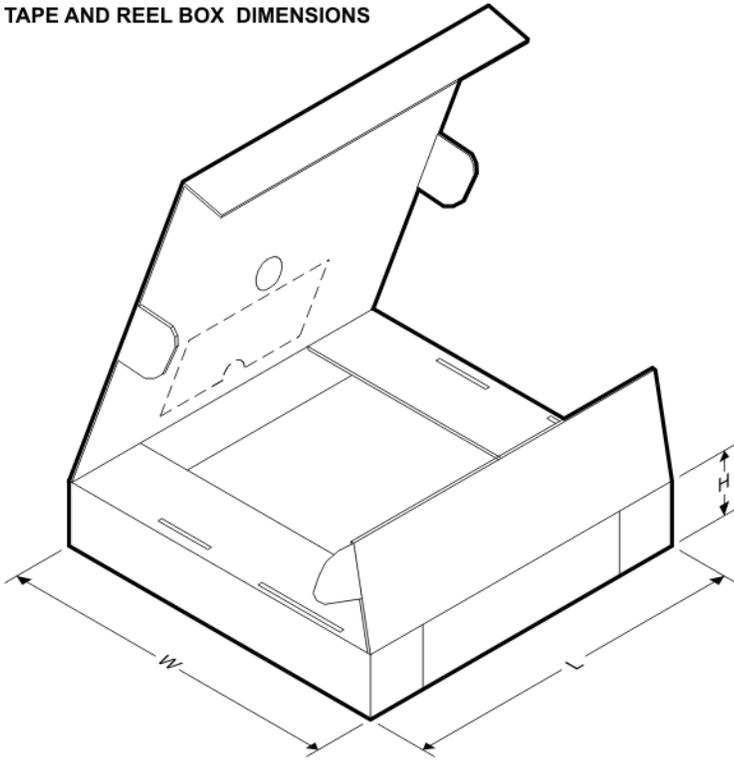


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5294IPFPR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
ADS5294IPFPT	HTQFP	PFP	80	250	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


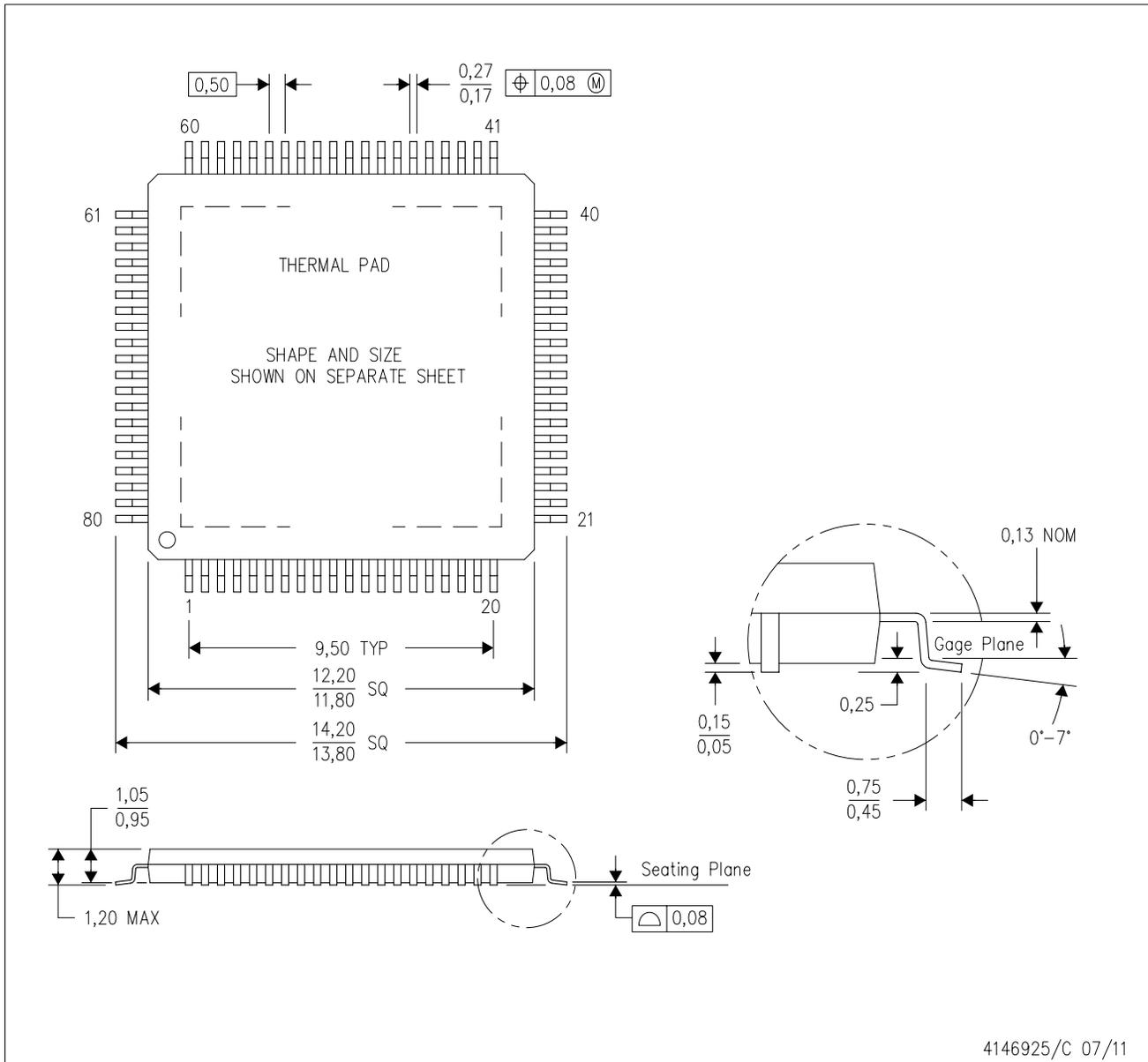
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5294IPFPR	HTQFP	PFP	80	1000	346.0	346.0	41.0
ADS5294IPFPT	HTQFP	PFP	80	250	346.0	346.0	41.0

# MECHANICAL DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

PFP (S-PQFP-G80)

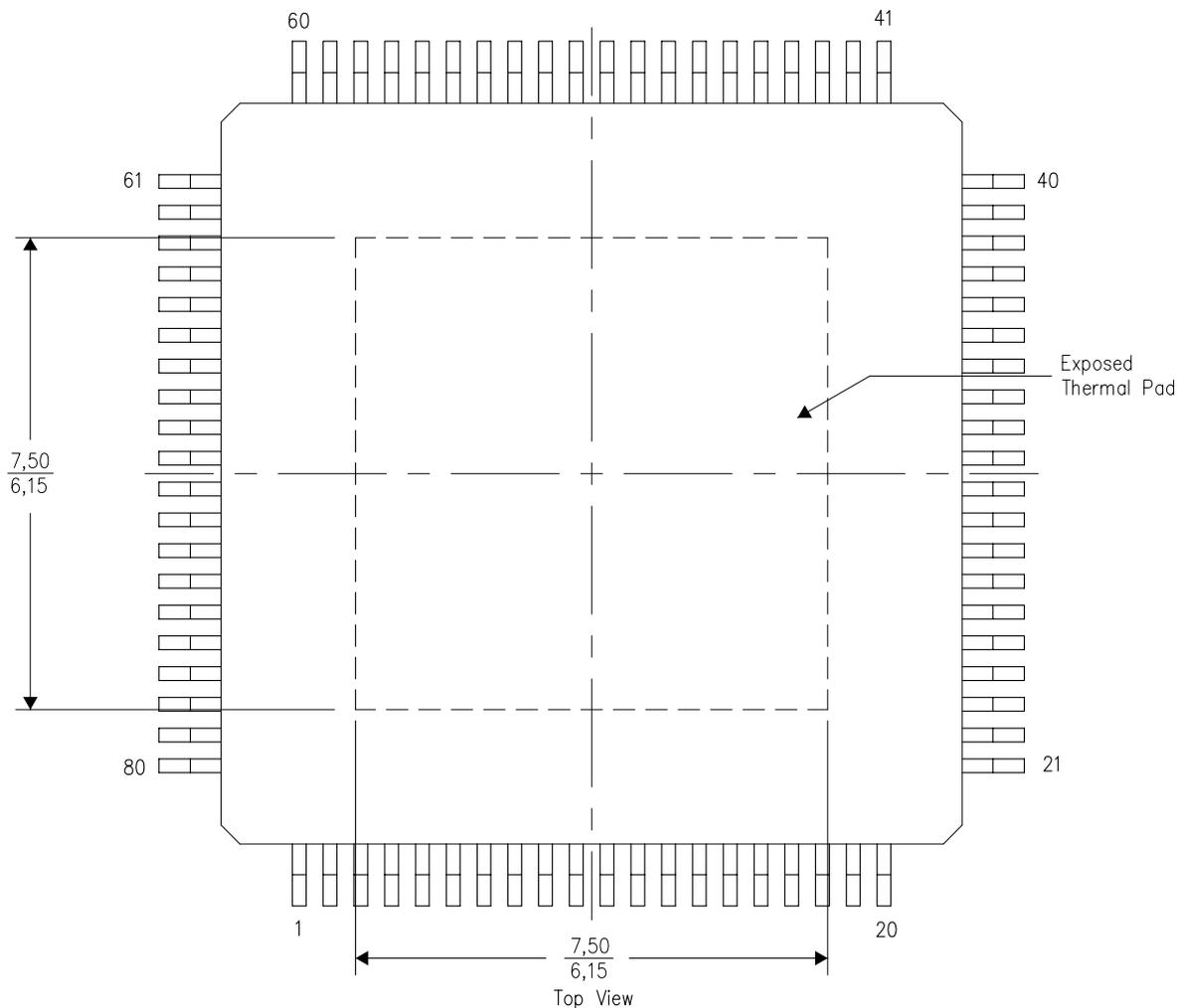
PowerPAD™ PLASTIC QUAD FLATPACK

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



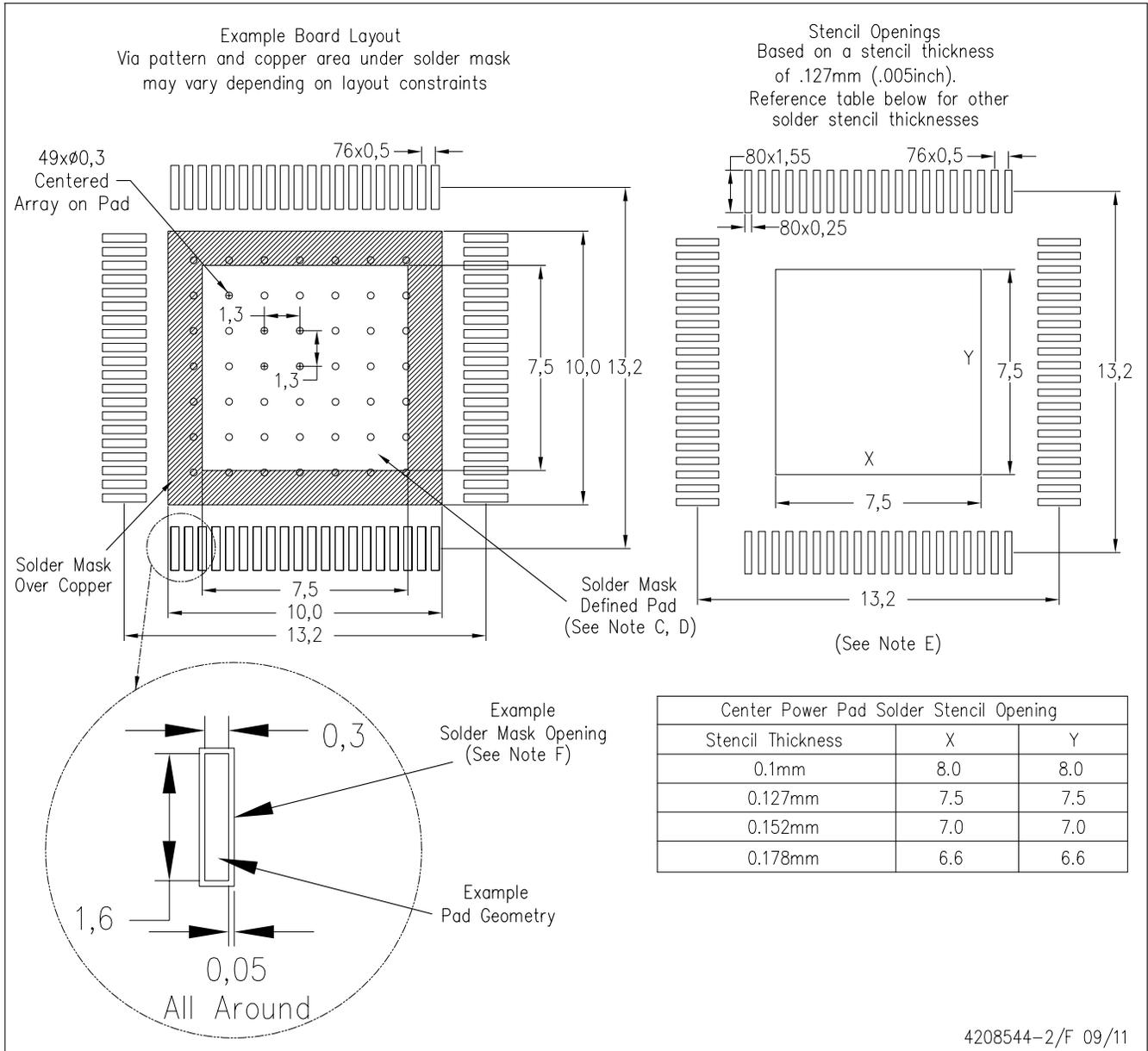
NOTE: A. All linear dimensions are in millimeters

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# LAND PATTERN DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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