

# ADC12010

## 12-Bit, 10 MSPS, 160 mW A/D Converter with Internal Sample-and-Hold

### General Description

The ADC12010 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 10 Megasamples per second (MSPS), minimum. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. Operating on a single 5V power supply, this device consumes just 160 mW at 10 MSPS, including the reference current. The Power Down feature reduces power consumption to 25 mW.

The differential inputs provide a full scale input swing equal to  $2V_{REF}$  with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. For ease of use, the buffered, high impedance, single-ended reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format is 12-bit offset binary.

This device is available in the 32-lead LQFP package and will operate over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### Features

- Internal sample-and-hold
- Outputs 2.4V to 5V compatible
- TTL/CMOS compatible input/outputs
- Power down mode
- On-chip reference buffer

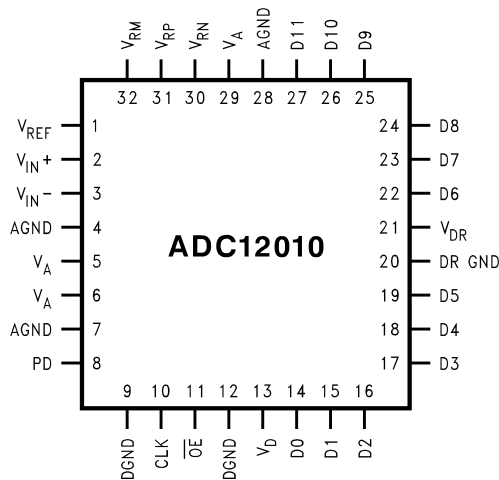
### Key Specifications

■ Resolution	12 Bits
■ Conversion Rate	10 MSPS (min)
■ DNL	$\pm 0.3$ LSB (typ)
■ INL	$\pm 0.5$ LSB (typ)
■ SNR ( $f_{IN} = 10.1$ MHz)	70 dB (typ)
■ ENOB ( $f_{IN} = 10.1$ MHz)	11.3 bits (typ)
■ Data Latency	6 Clock Cycles
■ Supply Voltage	+5V $\pm 5\%$
■ Power Consumption, 10 MHz	160 mW (typ)

### Applications

- Image Processing Front End
- Instrumentation
- PC-Based Data Acquisition
- Fax Machines
- Wireless Local Loops/Cable Modems
- Waveform Digitizers
- DSP Front Ends

### Connection Diagram



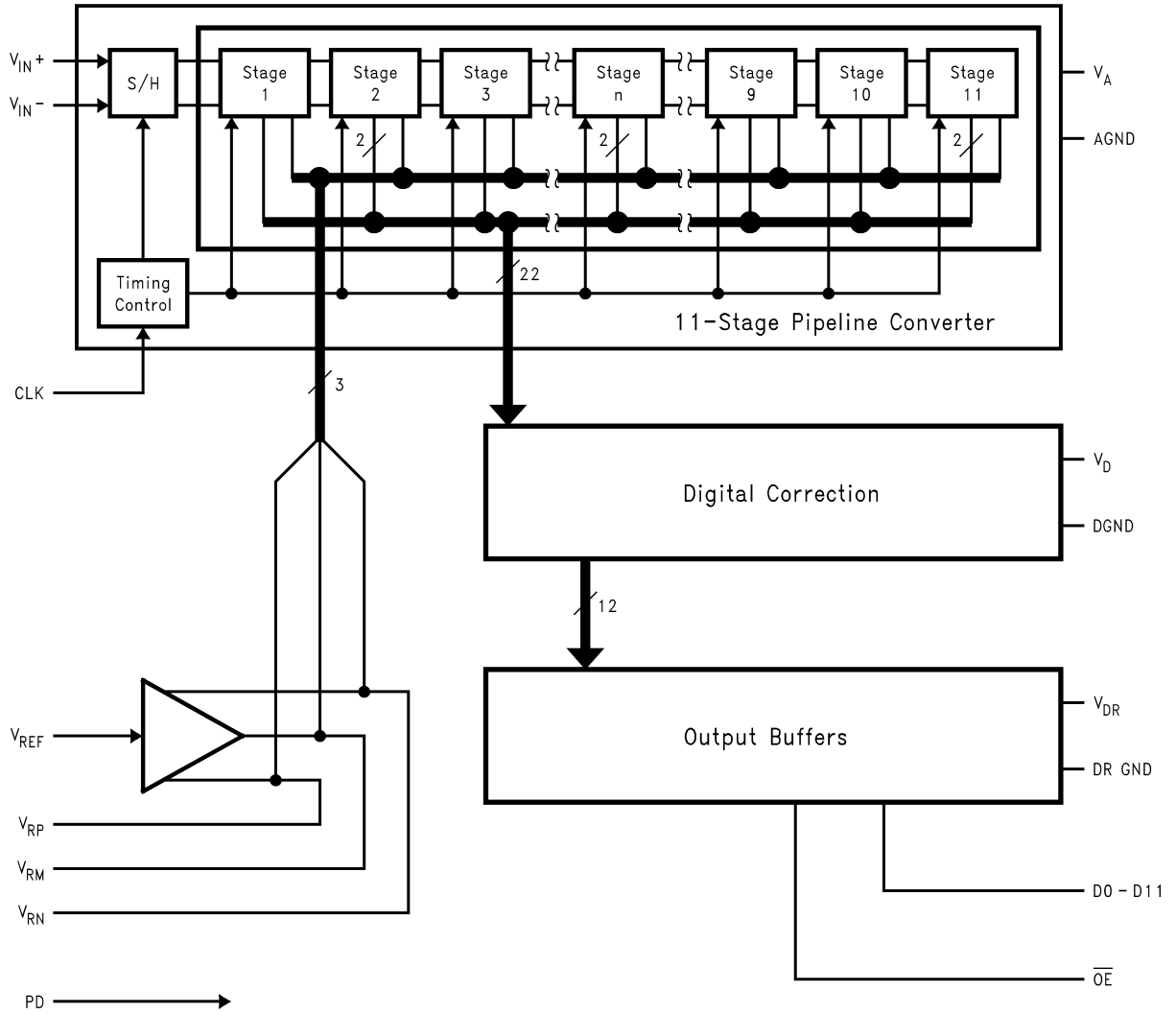
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## Ordering Information

Industrial ( $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ )	Package
ADC12010CIVY	32 Pin LQFP
ADC12010CIVYX	32 Pin LQFP Tape and Reel
ADC12010EVAL	Evaluation Board

## Block Diagram

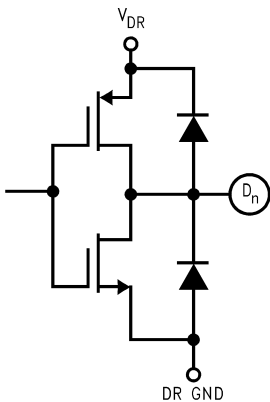


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## Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
<b>ANALOG I/O</b>			
2	$V_{IN+}$		Non-Inverting analog signal Input. With a 2.0V reference voltage, the ground-referenced input signal level is 2.0 $V_{P-P}$ centered on $V_{CM}$ .
3	$V_{IN-}$		Inverting analog signal Input. With a 2.0V reference voltage the ground-referenced input signal level is 2.0 $V_{P-P}$ centered on $V_{CM}$ . This pin may be connected to $V_{CM}$ for single-ended operation, but a differential input signal is required for best performance.
1	$V_{REF}$		Reference input. This pin should be bypassed to AGND with a 0.1 $\mu F$ monolithic capacitor. $V_{REF}$ is 2.0V nominal and should be between 1.0V to 2.4V.
31	$V_{RP}$		<p>These pins are high impedance reference bypass pins. Connect a 0.1 <math>\mu F</math> capacitor from each of these pins to AGND. DO NOT LOAD these pins.</p>
32	$V_{RM}$		
30	$V_{RN}$		
<b>DIGITAL I/O</b>			
10	CLK		Digital clock input. The range of frequencies for this input is 100 kHz to 15 MHz (typical) with guaranteed performance at 10 MHz. The input is sampled on the rising edge of this input.
11	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE® data output pins. When this pin is high, the outputs are in a high impedance state.
8	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.

## Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
14–19, 22–27	D0–D11		Digital data output pins that make up the 12-bit conversion results. D0 is the LSB, while D11 is the MSB of the offset binary output word. Output levels are TTL/CMOS compatible.
<b>ANALOG POWER</b>			
5, 6, 29	$V_A$		Positive analog supply pins. These pins should be connected to a quiet +5V voltage source and be bypassed to AGND with 0.1 $\mu\text{F}$ monolithic capacitors located within 1 cm of these power pins, and with a 10 $\mu\text{F}$ capacitor.
4, 7, 28	AGND		The ground return for the analog supply.
<b>DIGITAL POWER</b>			
13	$V_D$		Positive digital supply pin. This pin should be connected to the same quiet +5V source as is $V_A$ and bypassed to DGND with a 0.1 $\mu\text{F}$ monolithic capacitor in parallel with a 10 $\mu\text{F}$ capacitor, both located within 1 cm of the power pin.
9, 12	DGND		The ground return for the digital supply.
21	$V_{DR}$		Positive digital supply pin for the ADC12010's output drivers. This pin should be connected to a voltage source of +2.35V to +5V and be bypassed to DR GND with a 0.1 $\mu\text{F}$ monolithic capacitor. If the supply for this pin is different from the supply used for $V_A$ and $V_D$ , it should also be bypassed with a 10 $\mu\text{F}$ tantalum capacitor. $V_{DR}$ should never exceed the voltage on $V_D$ . All bypass capacitors should be located within 1 cm of the supply pin.
20	DR GND		The ground return for the digital supply for the ADC12010's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC12010's DGND or AGND pins. See Section 5 (Layout and Grounding) for more details.

**Absolute Maximum Ratings** (Notes 1,

2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_A, V_D$	6.5V
$V_{DR}$	$\leq V_D + 0.3V$
$ V_A - V_D $	$\leq 100$ mV
Voltage on Any Input or Output Pin	-0.3V to ( $V_A$ or $V_D$ + 0.3V)
Input Current at Any Pin (Note 3)	$\pm 25$ mA
Package Input Current (Note 3)	$\pm 50$ mA
Package Dissipation at $T_A = 25^\circ\text{C}$	See (Note 4)
ESD Susceptibility	
Human Body Model (Note 5)	2500V
Machine Model (Note 5)	250V
Soldering Temperature,	
Infrared, 10 sec. (Note 6)	235°C
Storage Temperature	-65°C to +150°C

**Operating Ratings** (Notes 1, 2)

Operating Temperature	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Supply Voltage ( $V_A, V_D$ )	+4.75V to +5.25V
Output Driver Supply ( $V_{DR}$ )	+2.35V to $V_D$
$V_{REF}$ Input	1.0V to 2.4V
CLK, PD, $\overline{OE}$	-0.05V to ( $V_D + 0.05V$ )
$V_{IN}$ Input	-0V to ( $V_A - 0.5V$ )
$V_{CM}$	1.0V to 4.0V
IAGND-DGNDI	$\leq 100\text{mV}$

**Converter Electrical Characteristics**

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V,  $V_A = V_D = +5V$ ,  $V_{DR} = +3.0V$ , PD = 0V,  $V_{REF} = +2.0V$ ,  $f_{CLK} = 10$  MHz,  $t_r = t_f = 3$  ns,  $C_L = 25$  pF/pin. **Boldface limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ\text{C}$  (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
<b>STATIC CONVERTER CHARACTERISTICS</b>					
	Resolution with No Missing Codes			<b>12</b>	Bits (min)
INL	Integral Non Linearity (Note 11)		$\pm 0.5$	<b><math>\pm 1.5</math></b>	LSB (max)
DNL	Differential Non Linearity		$\pm 0.3$	<b><math>\pm 0.9</math></b>	LSB (max)
GE	Gain Error		$\pm 0.2$	<b>2.9</b>	%FS (max)
	Offset Error ( $V_{IN} = V_{IN-}$ )		-0.1	<b>1.75</b>	%FS (max)
	Under Range Output Code		0	<b>0</b>	
	Over Range Output Code		4095	<b>4095</b>	
<b>DYNAMIC CONVERTER CHARACTERISTICS</b>					
FPBW	Full Power Bandwidth	0 dBFS Input, Output at -3 dB	100		MHz
SNR	Signal-to-Noise Ratio	$f_{IN} = 1$ MHz, $V_{IN} = -0.5$ dBFS	70		dB
		$f_{IN} = 4.4$ MHz, $V_{IN} = -0.5$ dBFS	70		dB
		$f_{IN} = 10.1$ MHz, $V_{IN} = -0.5$ dBFS	70	<b>66</b>	dB (min)
SINAD	Signal-to-Noise and Distortion	$f_{IN} = 1$ MHz, $V_{IN} = -0.5$ dBFS	70		dB
		$f_{IN} = 4.4$ MHz, $V_{IN} = -0.5$ dBFS	70		dB
		$f_{IN} = 10.1$ MHz, $V_{IN} = -0.5$ dBFS	69	<b>66</b>	dB (min)
ENOB	Effective Number of Bits	$f_{IN} = 1$ MHz, $V_{IN} = -0.5$ dBFS	11.4		dB
		$f_{IN} = 4.4$ MHz, $V_{IN} = -0.5$ dBFS	11.4		dB
		$f_{IN} = 10.1$ MHz, $V_{IN} = -0.5$ dBFS	11.3	<b>10.7</b>	dB (min)
THD	Total Harmonic Distortion	$f_{IN} = 1$ MHz, $V_{IN} = -0.5$ dBFS	-88		dB
		$f_{IN} = 4.4$ MHz, $V_{IN} = -0.5$ dBFS	-86		dB
		$f_{IN} = 10.1$ MHz, $V_{IN} = -0.5$ dBFS	-79	<b>-74</b>	dB (min)
SFDR	Spurious Free Dynamic Range	$f_{IN} = 1$ MHz, $V_{IN} = -0.5$ dBFS	92		dB
		$f_{IN} = 4.4$ MHz, $V_{IN} = -0.5$ dBFS	89		dB
		$f_{IN} = 10.1$ MHz, $V_{IN} = -0.5$ dBFS	83	<b>69</b>	dB (min)

## Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V,  $V_A = V_D = +5V$ ,  $V_{DR} = +3.0V$ , PD = 0V,  $V_{REF} = +2.0V$ ,  $f_{CLK} = 10$  MHz,  $t_r = t_f = 3$  ns,  $C_L = 25$  pF/pin. **Boldface limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ C$  (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
IMD	Intermodulation Distortion	$f_{IN} = 4.7$ MHz and 4.9 MHz, each = -7 dBFS	-75		dBFS
<b>REFERENCE AND ANALOG INPUT CHARACTERISTICS</b>					
$V_{CM}$	Common Mode Input Voltage		$V_A / 2$		V
$C_{IN}$	$V_{IN}$ Input Capacitance (each pin to GND)	$V_{IN} = 2.5$ Vdc + 0.7 $V_{rms}$	(CLK LOW) 8		pF
			(CLK HIGH) 7		pF
$V_{REF}$	Reference Voltage (Note 13)		2.00	<b>1.0</b> <b>2.4</b>	V (min) V (max)
	Reference Input Resistance		100		MΩ(min)

## DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V,  $V_A = V_D = +5V$ ,  $V_{DR} = +3.0V$ , PD = 0V,  $V_{REF} = +2.0V$ ,  $f_{CLK} = 10$  MHz,  $t_r = t_f = 3$  ns,  $C_L = 25$  pF/pin. **Boldface limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ C$  (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
<b>CLK, PD, OE DIGITAL INPUT CHARACTERISTICS</b>					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_D = 5.25V$		<b>2.0</b>	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_D = 4.75V$		<b>1.0</b>	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5.0V$	10		μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	-10		μA
$C_{IN}$	Digital Input Capacitance		5		pF
<b>D0-D11 DIGITAL OUTPUT CHARACTERISTICS</b>					
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_{OUT} = -0.5$ mA	$V_{DR} = 2.5V$	<b>2.3</b>	V (min)
			$V_{DR} = 3V$	<b>2.7</b>	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{DR} = 3V$		<b>0.4</b>	V (max)
$I_{OZ}$	TRI-STATE Output Current	$V_{OUT} = 2.5V$ or $5V$	100		nA
		$V_{OUT} = 0V$	-100		nA
+ $I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	-20		mA (min)
- $I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_{DR}$	20		mA (min)
<b>POWER SUPPLY CHARACTERISTICS</b>					
$I_A$	Analog Supply Current	PD Pin = DGND, $V_{REF} = 2.0V$	30	<b>39</b>	mA (max)
		PD Pin = $V_{DR}$	2.8		mA
$I_D$	Digital Supply Current	PD Pin = DGND	2	<b>2.5</b>	mA (max)
		PD Pin = $V_{DR}$ , $f_{CLK} = 0$	2.2		mA
$I_{DR}$	Digital Output Supply Current	PD Pin = DGND, $C_L = 0$ pF (Note 14)	0		mA
		PD Pin = $V_{DR}$ , $f_{CLK} = 0$	0		mA
	Total Power Consumption	PD Pin = DGND, $C_L = 0$ pF (Note 15)	160	<b>207</b>	mW
		PD Pin = $V_{DR}$ , $f_{CLK} = 0$	25		mW
PSRR1+	Power Supply Rejection Ratio	Rejection of Positive Full-Scale Error with $V_A = 4.75V$ vs. 5.25V	69		dBFS
PSRR1-	Power Supply Rejection Ratio	Rejection of Negative Full-Scale Error with $V_A = 4.75V$ vs. 5.25V	51		dBFS
PSRR2	Power Supply Rejection Ratio	Rejection of Power Supply Noise with 10 MHz, 250 mV <sub>P-P</sub> riding on $V_A$	48		dBFS

## AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V,  $V_A = V_D = +5V$ ,  $V_{DR} = +3.0V$ , PD = 0V,  $V_{REF} = +2.0V$ ,  $f_{CLK} = 10\text{ MHz}$ ,  $t_r = t_f = 3\text{ ns}$ ,  $C_L = 25\text{ pF/pin}$ . **Boldface limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^\circ\text{C}$  (Notes 7, 8, 9, 12)**

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
$f_{CLK}^1$	Maximum Clock Frequency		10	<b>15</b>	MHz (min)
$f_{CLK}^2$	Minimum Clock Frequency		100		kHz
$t_{CH}$	Clock High Time			<b>30</b>	ns (min)
$t_{CL}$	Clock Low Time			<b>30</b>	ns(min)
$t_{CONV}$	Conversion Latency			<b>6</b>	Clock Cycles
$t_{OD}$	Data Output Delay after Rising CLK Edge	$V_{DR} = 2.5V$	11	<b>16.8</b>	ns (max)
		$V_{DR} = 3.0V$	11	<b>16.8</b>	ns (max)
$t_{AD}$	Aperture Delay		1.2		ns
$t_{AJ}$	Aperture Jitter		2		ps rms
$t_{DIS}$	Data outputs into TRI-STATE Mode		4		ns
$t_{EN}$	Data Outputs Active after TRI-STATE		4		ns
$t_{PD}$	Power Down Mode Exit Cycle	0.1 $\mu\text{F}$ cap on pins 30, 31,32	500		ns

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

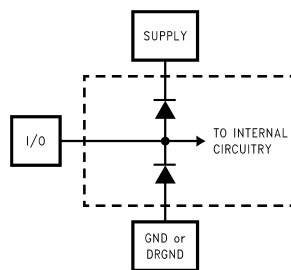
**Note 3:** When the input voltage at any pin exceeds the power supplies (that is,  $V_{IN} < AGND$ , or  $V_{IN} > V_A$ ), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

**Note 4:** The absolute maximum junction temperature ( $T_{Jmax}$ ) for this device is  $150^\circ\text{C}$ . The maximum allowable power dissipation is dictated by  $T_{Jmax}$ , the junction-to-ambient thermal resistance ( $\theta_{JA}$ ), and the ambient temperature, ( $T_A$ ), and can be calculated using the formula  $P_{DMAX} = (T_{Jmax} - T_A) / \theta_{JA}$ . In the 32-pin LQFP,  $\theta_{JA}$  is  $79^\circ\text{C/W}$ , so  $P_{DMAX} = 1,582\text{ mW}$  at  $25^\circ\text{C}$  and  $823\text{ mW}$  at the maximum operating ambient temperature of  $85^\circ\text{C}$ . Note that the power consumption of this device under normal operation will typically be about 180 mW (160 typical power consumption + 20 mW TTL output loading). The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

**Note 5:** Human body model is 100 pF capacitor discharged through a 1.5 k $\Omega$  resistor. Machine model is 220 pF discharged through 0 $\Omega$ .

**Note 6:** The  $235^\circ\text{C}$  reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above  $183^\circ\text{C}$  for a minimum 60 seconds. The temperature measured on the package body must not exceed  $220^\circ\text{C}$ . Only one excursion above  $183^\circ\text{C}$  is allowed per reflow cycle.

**Note 7:** The inputs are protected as shown below. Input voltage magnitudes above  $V_A$  or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above  $V_A$  or below GND by more than 100 mV. As an example, if  $V_A$  is 4.75V, the full-scale input voltage must be  $\leq 4.85V$  to ensure accurate conversions.



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**Note 8:** To guarantee accuracy, it is required that  $|V_A - V_D| \leq 100\text{ mV}$  and separate bypass capacitors are used at each power supply pin.

**Note 9:** With the test condition for  $V_{REF} = +2.0V$  (4V<sub>P-P</sub> differential input), the 12-bit LSB is 977  $\mu\text{V}$ .

**Note 10:** Typical figures are at  $T_A = T_J = 25^\circ\text{C}$ , and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 11:** Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

**Note 12:** Timing specifications are tested at TTL logic levels,  $V_{IL} = 0.4V$  for a falling edge and  $V_{IH} = 2.4V$  for a rising edge.

**Note 13:** Optimum performance will be obtained by keeping the reference input in the 1.8V to 2.2V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for this application.

## AC Electrical Characteristics (Continued)

**Note 14:**  $I_{DR}$  is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage,  $V_{DR}$ , and the rate at which the outputs are switching (which is signal dependent).  $I_{DR} = V_{DR}(C_0 \times f_0 + C_1 \times f_1 + \dots + C_{11} \times f_{11})$  where  $V_{DR}$  is the output driver power supply voltage,  $C_n$  is total capacitance on the output pin, and  $f_n$  is the average frequency at which that pin is toggling.

**Note 15:** Excludes  $I_{DR}$ . See note 14.

### Specification Definitions

**APERTURE DELAY** is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

**APERTURE JITTER (APERTURE UNCERTAINTY)** is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

**CLOCK DUTY CYCLE** is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

**COMMON MODE VOLTAGE ( $V_{CM}$ )** is the d.c. potential present at both signal inputs to the ADC.

**CONVERSION LATENCY** is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as  $(\text{SINAD} - 1.76) / 6.02$  and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**FULL POWER BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

**GAIN ERROR** is the deviation from the ideal slope of the transfer function. It can be calculated as:

$$\text{Gain Error} = \text{Positive Full Scale Error} - \text{Offset Error}$$

**INTEGRAL NON LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from negative full scale ( $1/2$  LSB below the first code transition) through positive full scale ( $1/2$  LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

**INTERMODULATION DISTORTION (IMD)** is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

**MISSING CODES** are those output codes that will never appear at the ADC outputs. The ADC12010 is guaranteed not to have any missing codes.

**NEGATIVE FULL SCALE ERROR** is the difference between the actual first code transition and its ideal value of  $1/2$  LSB above negative full scale.

**OFFSET ERROR** is the difference between the two input voltages ( $V_{IN+} - V_{IN-}$ ) required to cause a transition from code 2047 to 2048.

**OUTPUT DELAY** is the time delay after the rising edge of the clock before the data update is presented at the output pins.

**PIPELINE DELAY (LATENCY)** See CONVERSION LATENCY

**POSITIVE FULL SCALE ERROR** is the difference between the actual last code transition and its ideal value of  $1/2$  LSB below positive full scale.

**POWER SUPPLY REJECTION RATIO (PSRR)** is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12010, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the dc power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

**SIGNAL TO NOISE RATIO (SNR)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

**SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD)** Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

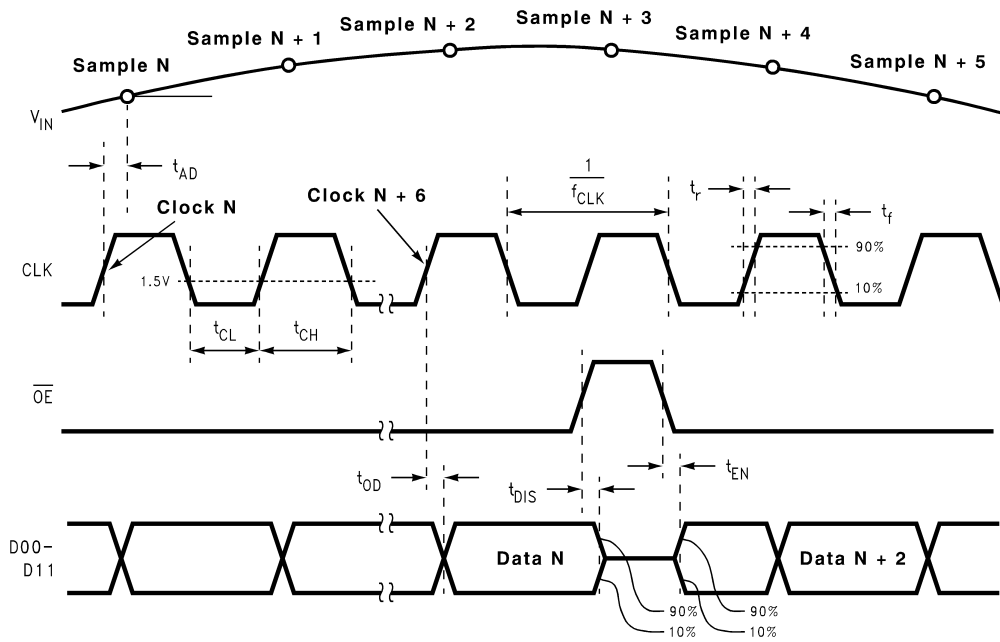
**TOTAL HARMONIC DISTORTION (THD)** is the ratio, expressed in dBc, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \times \log \sqrt{\frac{f_2^2 + \dots + f_{10}^2}{f_1^2}}$$

where  $f_1$  is the RMS power of the fundamental (output) frequency and  $f_2$  through  $f_{10}$  are the RMS power in the first 9 harmonic frequencies.



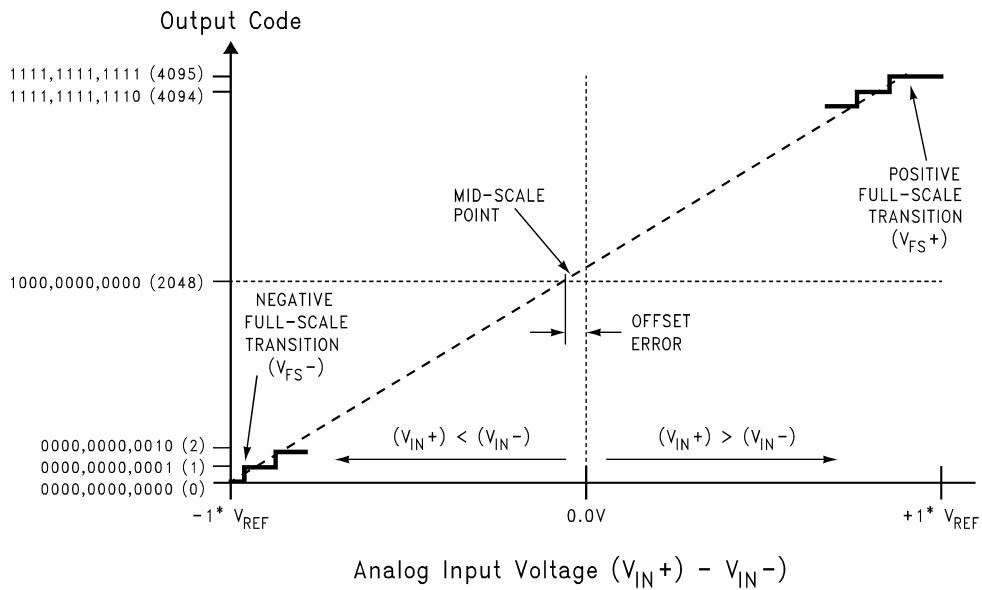
### Timing Diagram



Output Timing

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### Transfer Characteristic



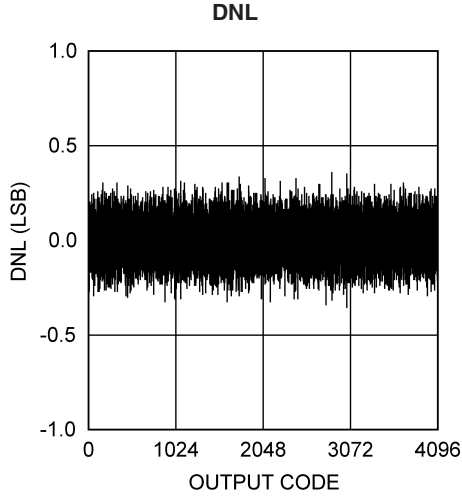
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FIGURE 1. Transfer Characteristic

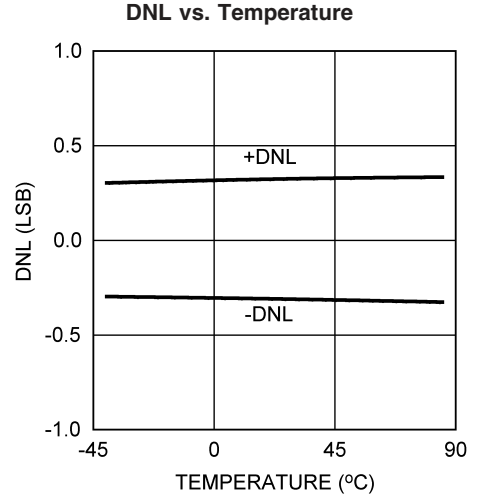
# ADC12010 Typical Performance Characteristics

$f_{CLK} = 10 \text{ MHz}$ ,  $f_{IN} = 10.1 \text{ MHz}$ ,  $V_{REF} = 2.0\text{V}$  unless otherwise stated

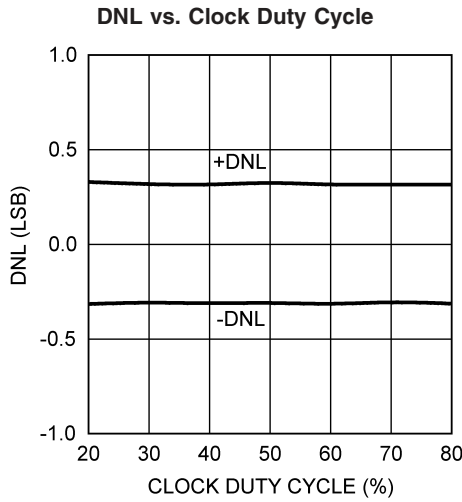
$V_A = V_D = 5.0\text{V}$ ,  $V_{DR} = 3.0\text{V}$ ,



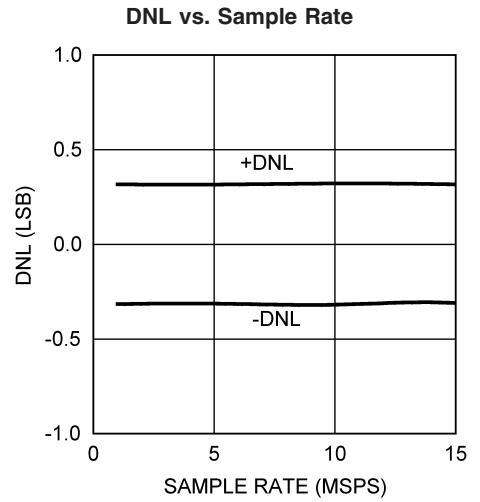
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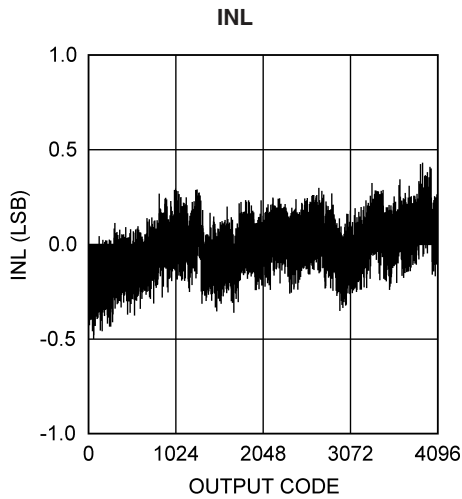
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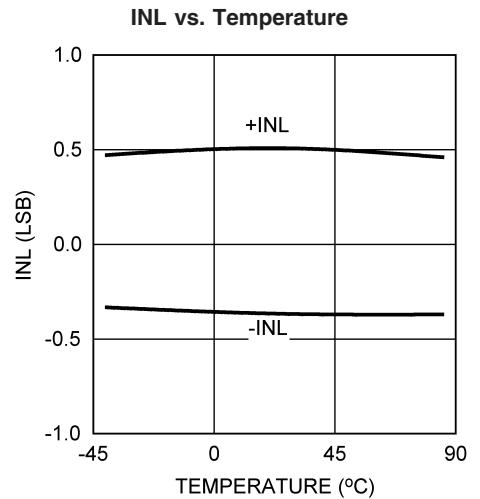
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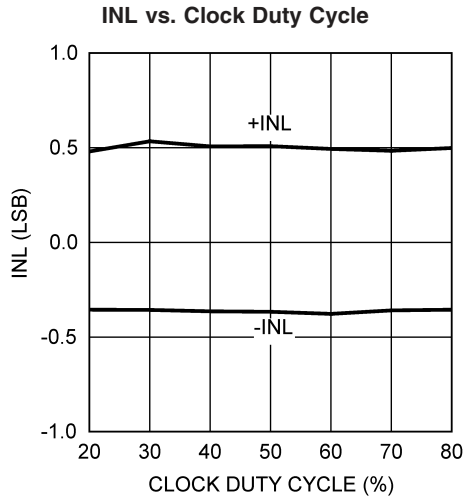


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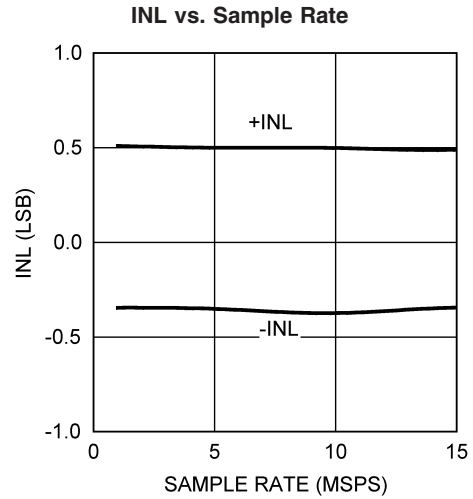


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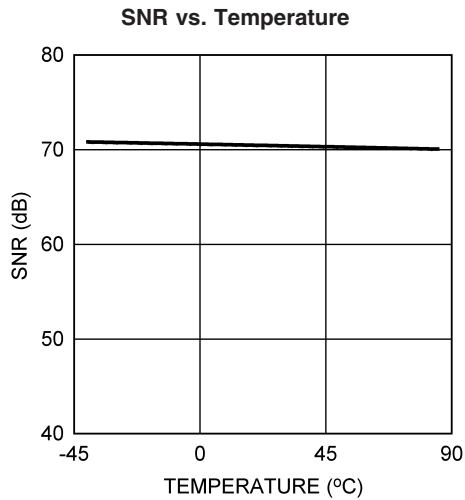
**ADC12010 Typical Performance Characteristics**  $V_A = V_D = 5.0V$ ,  $V_{DR} = 3.0V$ ,  $f_{CLK} = 10\text{ MHz}$ ,  $f_{IN} = 10.1\text{ MHz}$ ,  $V_{REF} = 2.0V$  unless otherwise stated (Continued)



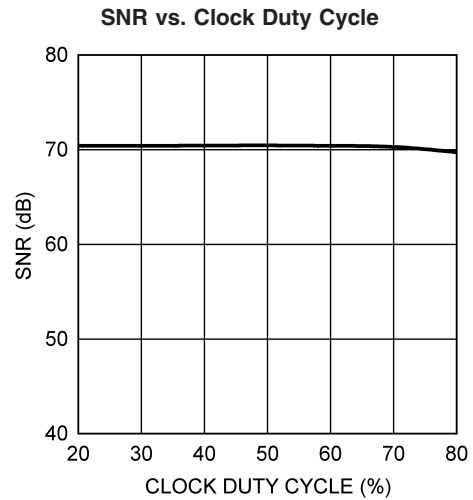
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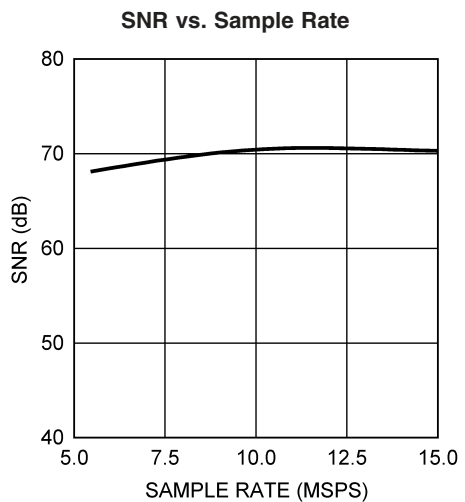
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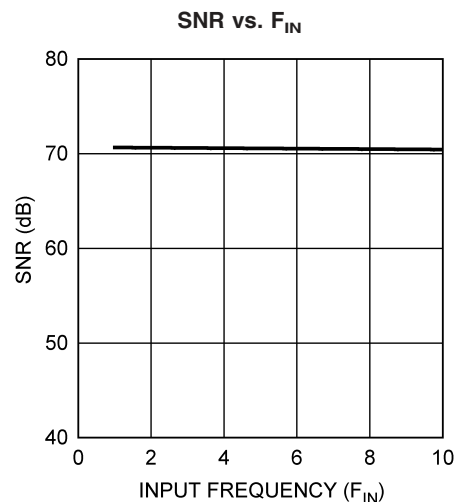
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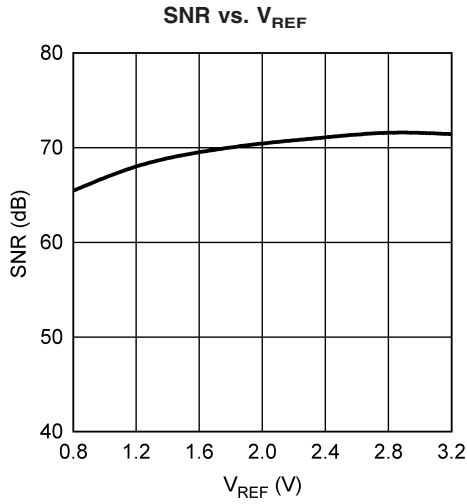


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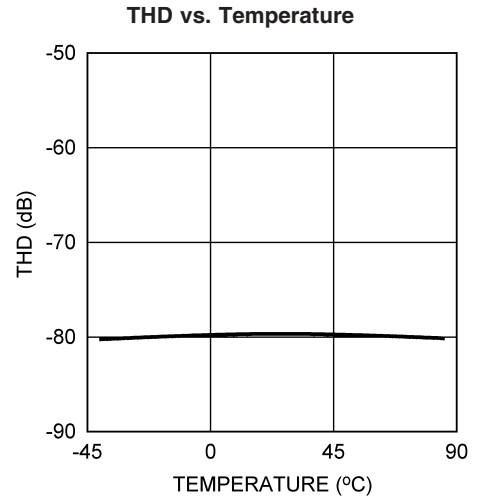


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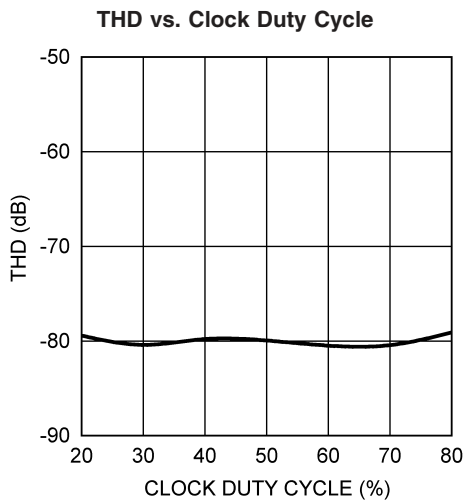
**ADC12010 Typical Performance Characteristics**  $V_A = V_D = 5.0V$ ,  $V_{DR} = 3.0V$ ,  $f_{CLK} = 10\text{ MHz}$ ,  $f_{IN} = 10.1\text{ MHz}$ ,  $V_{REF} = 2.0V$  unless otherwise stated (Continued)



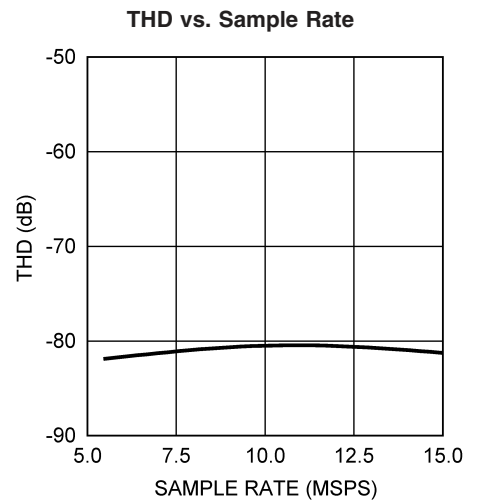
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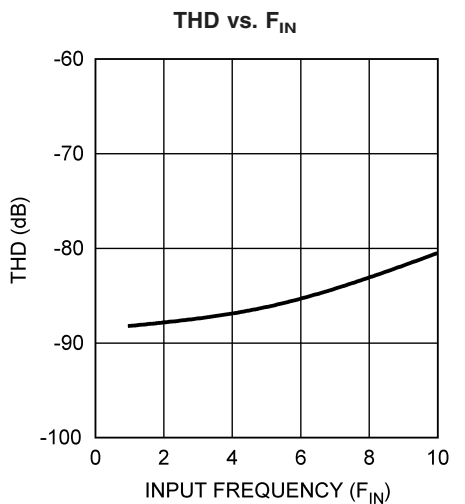
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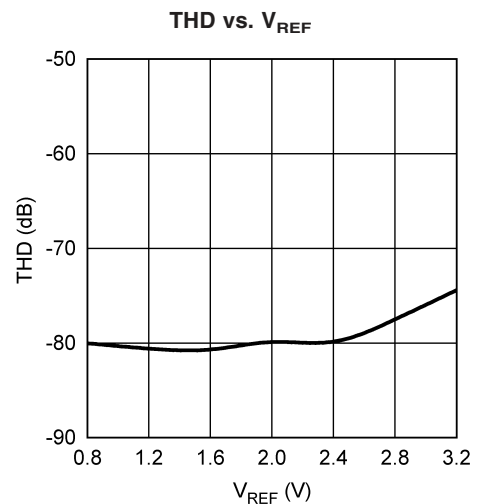
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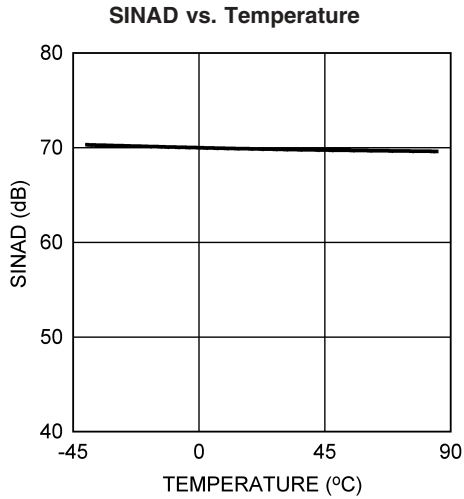


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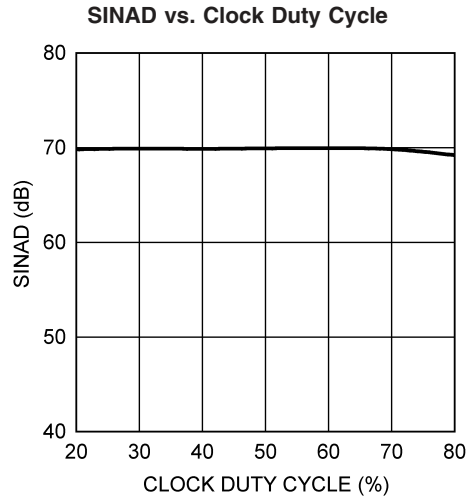


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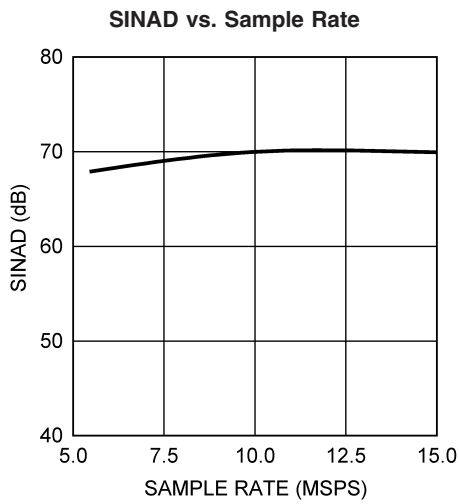
**ADC12010 Typical Performance Characteristics**  $V_A = V_D = 5.0V$ ,  $V_{DR} = 3.0V$ ,  $f_{CLK} = 10\text{ MHz}$ ,  $f_{IN} = 10.1\text{ MHz}$ ,  $V_{REF} = 2.0V$  unless otherwise stated (Continued)



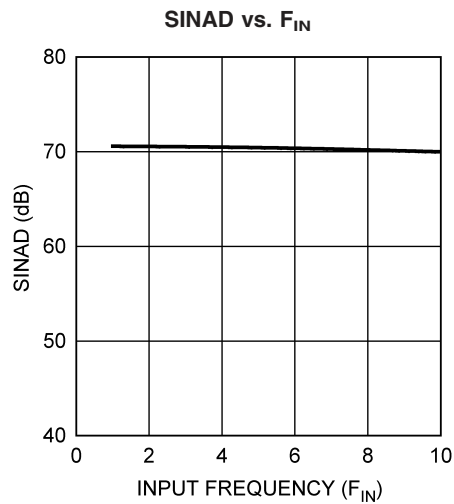
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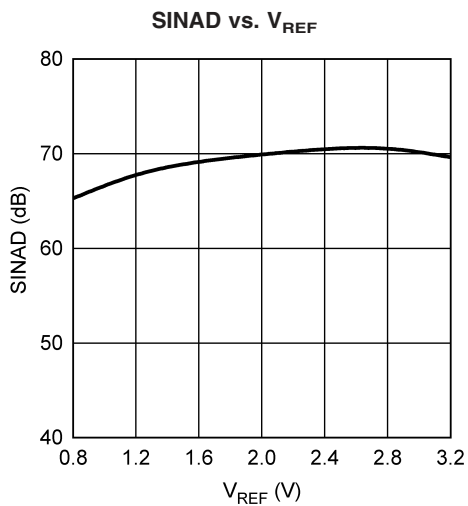
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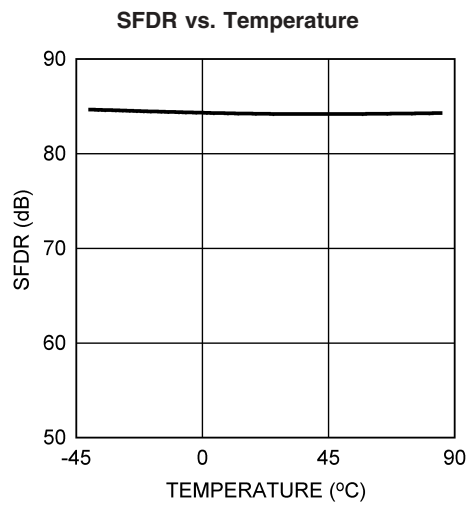
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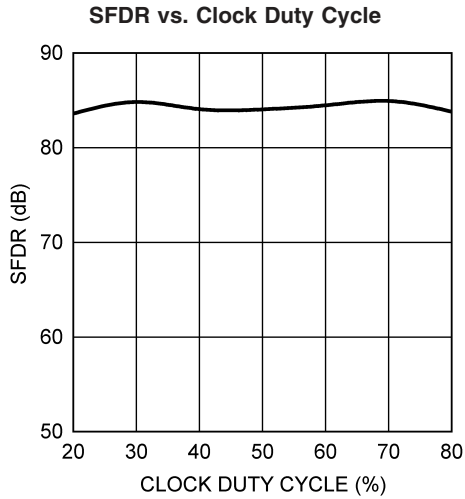


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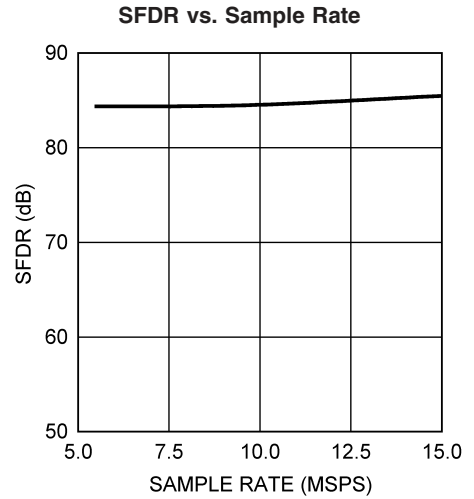


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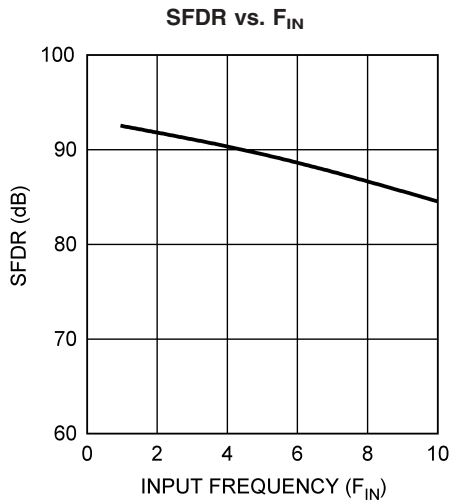
**ADC12010 Typical Performance Characteristics**  $V_A = V_D = 5.0V$ ,  $V_{DR} = 3.0V$ ,  $f_{CLK} = 10\text{ MHz}$ ,  $f_{IN} = 10.1\text{ MHz}$ ,  $V_{REF} = 2.0V$  unless otherwise stated (Continued)



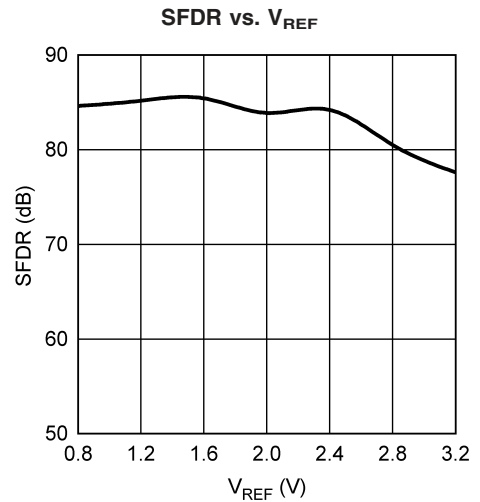
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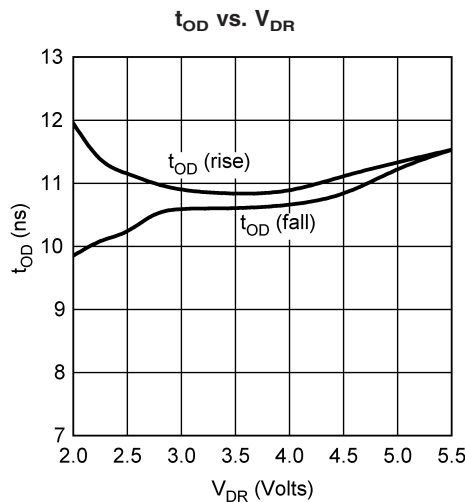
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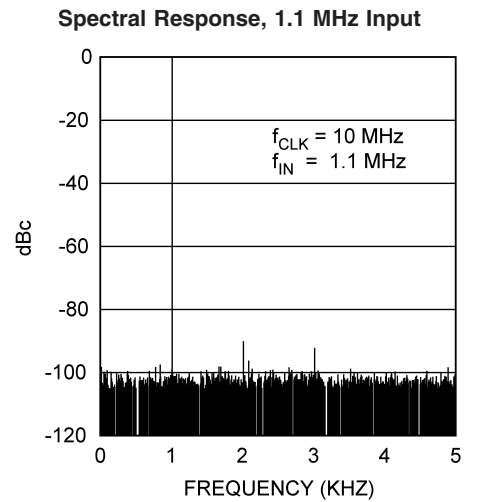
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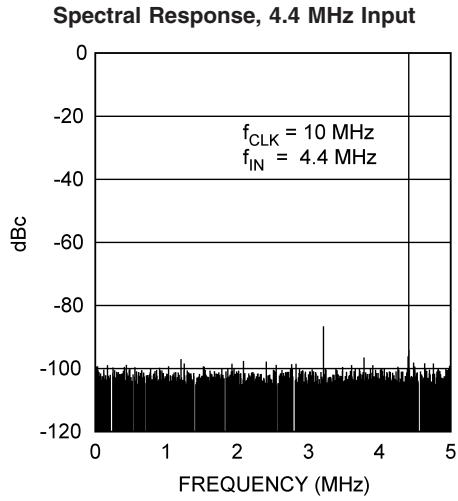


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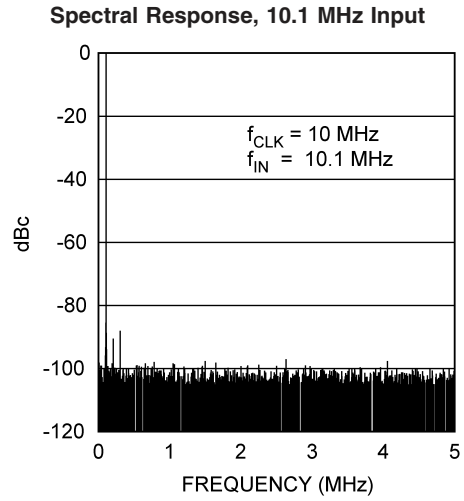


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**ADC12010 Typical Performance Characteristics**  $V_A = V_D = 5.0V$ ,  $V_{DR} = 3.0V$ ,  $f_{CLK} = 10\text{ MHz}$ ,  
 $f_{IN} = 10.1\text{ MHz}$ ,  $V_{REF} = 2.0V$  unless otherwise stated (Continued)



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## Functional Description

Operating on a single +5V supply, the ADC12010 uses a pipeline architecture with error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits.

The reference input is buffered to ease the task of driving that pin.

The output word rate is the same as the clock frequency, which can be between 100 kSPS and 15 MSPS (typical). The analog input voltage is acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 6 clock cycles.

A logic high on the power down (PD) pin reduces the converter power consumption to 40 mW.

## Applications Information

### 1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12010:

- $4.75V \leq V_A \leq 5.25V$
- $V_D = V_A$
- $2.35V \leq V_{DR} \leq V_D$
- $100 \text{ kHz} \leq f_{CLK} \leq 15 \text{ MHz}$
- $1.0V \leq V_{REF} \leq 2.4V$

### 1.1 Analog Inputs

The ADC12010 has two analog signal inputs,  $V_{IN+}$  and  $V_{IN-}$ . These two pins form a differential input pair. There is one reference input pin,  $V_{REF}$ .

### 1.2 Reference Pins

The ADC12010 is designed to operate with a 2.0V reference, but performs well with reference voltages in the range of 1.0V to 2.4V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12010. Increasing the reference voltage (and the input signal swing) beyond 2.4V will degrade THD for a full-scale input. It is very important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single point to minimize the effects of noise currents in the ground path.

The three Reference Bypass Pins ( $V_{RP}$ ,  $V_{RM}$  and  $V_{RN}$ ) are made available for bypass purposes. These pins should each be bypassed to ground with a 0.1  $\mu$ F capacitor. Smaller capacitor values will allow faster recovery from the power down mode, but may result in degraded noise performance. DO NOT LOAD these pins.

### 1.3 Signal Inputs

The signal inputs are  $V_{IN+}$  and  $V_{IN-}$ . The input signal,  $V_{IN}$ , is defined as

$$V_{IN} = (V_{IN+}) - (V_{IN-})$$

Figure 2 shows the expected input signal range.

Note that the common mode input voltage range is 1V to 3V with a nominal value of  $V_A/2$ . The input signals should remain between ground and 4V.

The Peaks of the individual input signals ( $V_{IN+}$  and  $V_{IN-}$ ) should each never exceed the voltage described as

$$V_{IN+}, V_{IN-} = V_{REF} + V_{CM}$$

to maintain THD and SINAD performance.

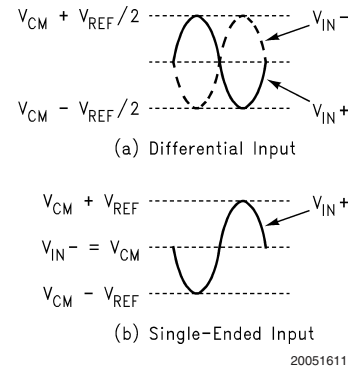


FIGURE 2. Expected Input Signal Range

The ADC12010 performs best with a differential input with each input centered around  $V_{CM}$ . The peak-to-peak voltage swing at both  $V_{IN+}$  and  $V_{IN-}$  each should not exceed the value of the reference voltage or the output data will be clipped. The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For a complex waveform, however, angular errors will result in distortion.

For angular deviations of up to 10 degrees from these two signals being 180 out of phase, the full scale error in LSB can be described as approximately

$$E_{FS} = dev^{1.79}$$

Where dev is the angular difference, in degrees, between the two signals having a 180° relative phase relationship to each other (see Figure 3). Drive the analog inputs with a source impedance less than 100 $\Omega$ .

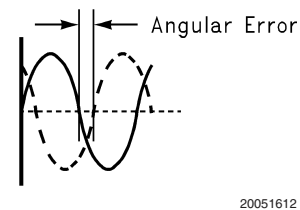


FIGURE 3. Angular Errors Between the Two Input Signals Will Reduce the Output Level

For differential operation, each analog input signal should have a peak-to-peak voltage equal to the input reference voltage,  $V_{REF}$ , and be centered around a common mode voltage,  $V_{CM}$ .

TABLE 1. Input to Output Relationship—Differential Input

$V_{IN+}$	$V_{IN-}$	Output
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	0100 0000 0000
$V_{CM}$	$V_{CM}$	1000 0000 0000
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111



## Applications Information (Continued)

**TABLE 2. Input to Output Relationship—  
Single-Ended Input**

V <sub>IN+</sub>	V <sub>IN-</sub>	Output
V <sub>CM</sub> - V <sub>REF</sub>	V <sub>CM</sub>	0000 0000 0000
V <sub>CM</sub> - V <sub>REF</sub> /2	V <sub>CM</sub>	0100 0000 0000
V <sub>CM</sub>	V <sub>CM</sub>	1000 0000 0000
V <sub>CM</sub> + V <sub>REF</sub> /2	V <sub>CM</sub>	1100 0000 0000
V <sub>CM</sub> + V <sub>REF</sub>	V <sub>CM</sub>	1111 1111 1111

### 1.3.1 Single-Ended Operation

Single-ended performance is lower than with differential input signals. For this reason, single-ended operation is not recommended. However, if single ended-operation is required, one of the analog inputs should be connected to the d.c. common mode voltage of the driven input. The peak-to-peak differential input signal should be twice the reference voltage to maximize SNR and SINAD performance (Figure 2b).

For example, set V<sub>REF</sub> to 1.0V, bias V<sub>IN-</sub> to 1.0V and drive V<sub>IN+</sub> with a signal range of 0V to 2.0V. Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. Table 1 and Table 2 indicate the input to output relationship of the ADC12010.

### 1.3.2 Driving the Analog Input

The V<sub>IN+</sub> and the V<sub>IN-</sub> inputs of the ADC12010 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 8 pF when the clock is low, and 7 pF when the clock is high. Although this difference is small, a dynamic capacitance is more difficult to drive than is a fixed capacitance, so choose the driving amplifier carefully. The LMH6702 and the LMH6628 are good amplifiers for driving the ADC12010.

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To prevent this, use 100Ω series resistors at each of the signal inputs with a 150 pF at each of the inputs, as can be seen in Figure 5 and Figure 6. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. Table 3 gives component values for Figure 5 to convert individual input signals to a range of 2.5V ±2.0V at each of the input pins of the ADC12010.

**TABLE 3. Resistor Values for Circuit of Figure 5**

SIGNAL RANGE	R1	R2	R3	R4	R5, R6
0 - 0.5V	392Ω	1540Ω	102Ω	115Ω	1000Ω
0 - 1.0V	634Ω	1470Ω	2490Ω	1050Ω	499Ω
±0.25V	499Ω	499Ω	499Ω	499Ω	1000Ω
±0.5V	100Ω	200Ω	100Ω	200Ω	499Ω

### 1.3.3 Input Common Mode Voltage

The input common mode voltage, V<sub>CM</sub>, should be in the range of 0.5V to 4.0V and be of a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 0.5 Volts below the V<sub>A</sub> supply voltage. The nominal V<sub>CM</sub> should generally be equal to V<sub>REF</sub>/2, but V<sub>RM</sub> can be used as a V<sub>CM</sub> source as long as V<sub>CM</sub> need not supply more than 10 μA of current.

## 2.0 DIGITAL INPUTS

The digital TTL/CMOS compatible inputs consist of CLK,  $\overline{OE}$  and PD.

### 2.1 CLK

The CLK signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 100 kHz to 15 MHz with rise and fall times of less than 3ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

If the CLK is interrupted, or its frequency too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate to 100 kSPS.

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12010 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 20% to 80%.

The clock line should be series terminated at the source end in the characteristic impedance of that line if the clock line is longer than

$$\frac{t_r}{6 \times t_{PR}}$$

where t<sub>r</sub> is the rise time of the clock signal and t<sub>PR</sub> is the propagation rate along the line. For a Board of FR-4 material, t<sub>PR</sub> is typically about 150 ps/inch, or 60 ps/cm. This resistor should be as close to the source as possible.

It might also be necessary to AC terminate the ADC end of the clock line with a series RC to ground such that the resistor value equals the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PR} \times L}{Z_0}$$

where t<sub>PR</sub> is again the propagation rate down the clock line, L is the length of the line in inches and Z<sub>0</sub> is the characteristic impedance of the clock line. A.C. termination should be near the ADC clock pin but beyond that pin as seen from the clock source.

Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 or AN-1113 for information on setting and determining characteristic impedance.

## Applications Information (Continued)

### 2.2 $\overline{OE}$

The  $\overline{OE}$  pin, when high, puts the output pins into a high impedance state. When this pin is low the outputs are in the active state. The ADC12010 will continue to convert whether this pin is high or low, but the output can not be read while the  $\overline{OE}$  pin is high.

The  $\overline{OE}$  pin should NOT be used to multiplex devices together to drive a common bus as this will result in excessive capacitance on the data output pins, reducing SNR and SINAD performance of the converter. See Section 3.0.

### 2.3 PD

The PD pin, when high, holds the ADC12010 in a power-down mode to conserve power when the converter is not being used. The power consumption is 25 mW and the output data pins are undefined in this mode. The data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the capacitors on pins 30, 31 and 32. These capacitors lose their charge in the Power Down mode and must be charged by on-chip circuitry before conversions can be accurate.

### 3.0 OUTPUTS

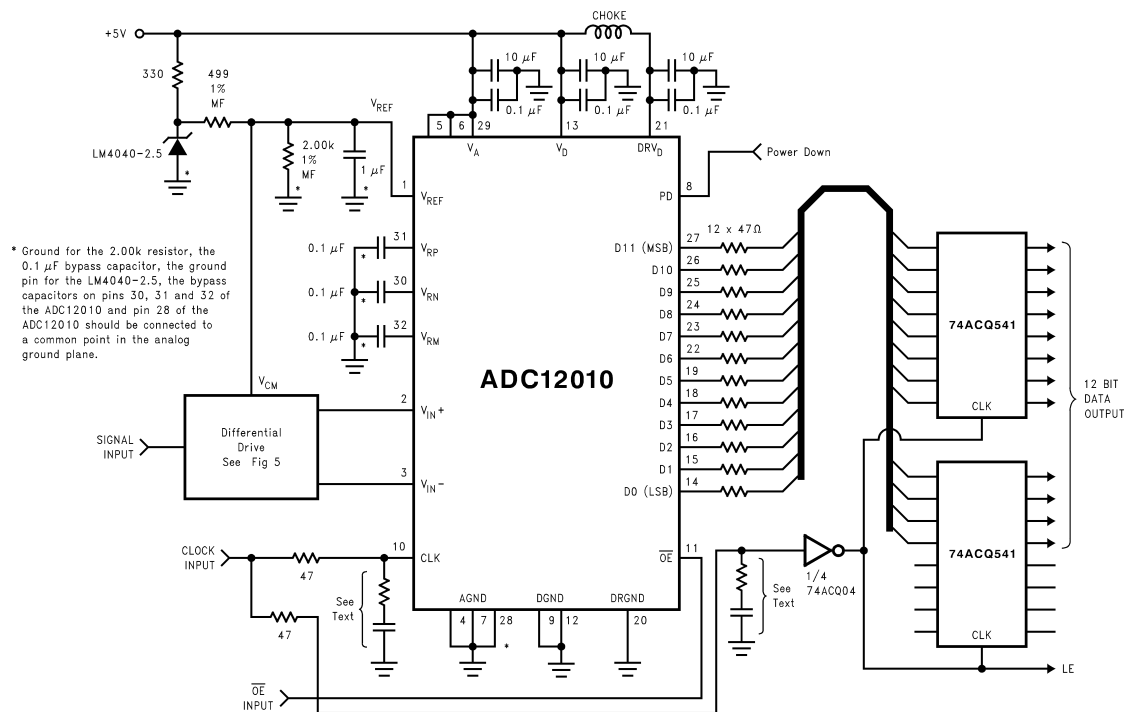
The ADC12010 has 12 TTL/CMOS compatible Data Output pins. Valid offset binary data is present at these outputs while

the  $\overline{OE}$  and PD pins are low. While the  $t_{OD}$  time provides information about output timing, a simple way to capture a valid output is to latch the data on the falling edge of the conversion clock (pin 10).

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through  $V_{DR}$  and DR GND. These large charging current spikes can cause on-chip noise that can couple into the analog circuitry, degrading dynamic performance. Adequate power supply bypassing and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 25 pF/pin will cause  $t_{OD}$  to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers (74ACQ541, for example) between the ADC outputs and any other circuitry. Only one driven input should be connected to each output pin. Additionally, inserting series resistors of 47 $\Omega$  to 100 $\Omega$  at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See Figure 4.

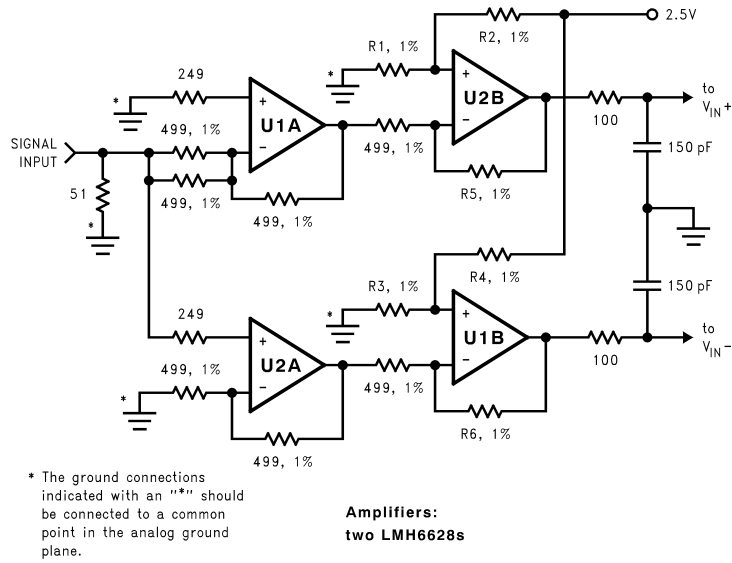
While the ADC12010 will operate with  $V_{DR}$  voltages down to 1.8V,  $t_{OD}$  increases with reduced  $V_{DR}$ . Be careful of external timing when using reduced  $V_{DR}$ .



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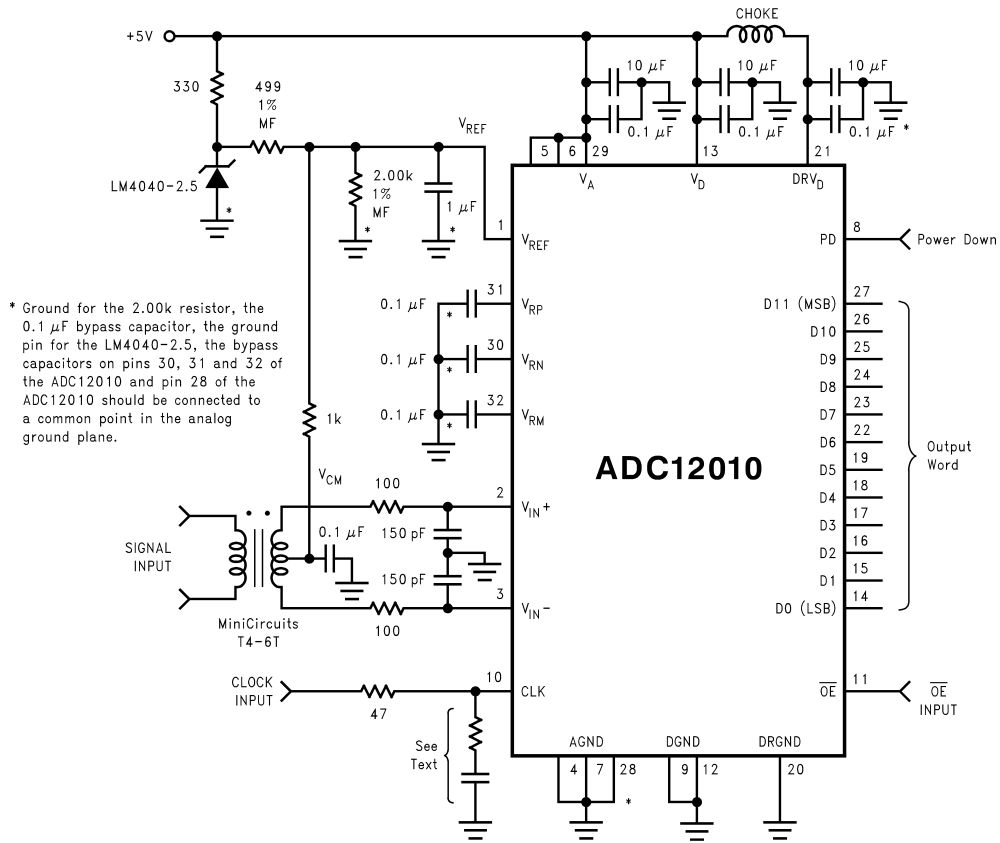
FIGURE 4. Simple Application Circuit with Single-Ended to Differential Buffer

Applications Information (Continued)



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FIGURE 5. Differential Drive Circuit of Figure 4



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FIGURE 6. Driving the Signal Inputs with a Transformer

## Applications Information (Continued)

### 4.0 POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10  $\mu$ F capacitor and with a 0.1  $\mu$ F ceramic chip capacitor within a centimeter of each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12010 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV<sub>P-P</sub>.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during turn on and turn off of power.

The V<sub>DR</sub> pin provides power for the output drivers and may be operated from a supply in the range of 2.35V to V<sub>D</sub> (nominal 5V). This can simplify interfacing to 3V devices and systems. **DO NOT operate the V<sub>DR</sub> pin at a voltage higher than V<sub>D</sub>.**

### 5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12010 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12010's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

The effects of the noise generated from the ADC output switching can be minimized through the use of 47 $\Omega$  to 100 $\Omega$  resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

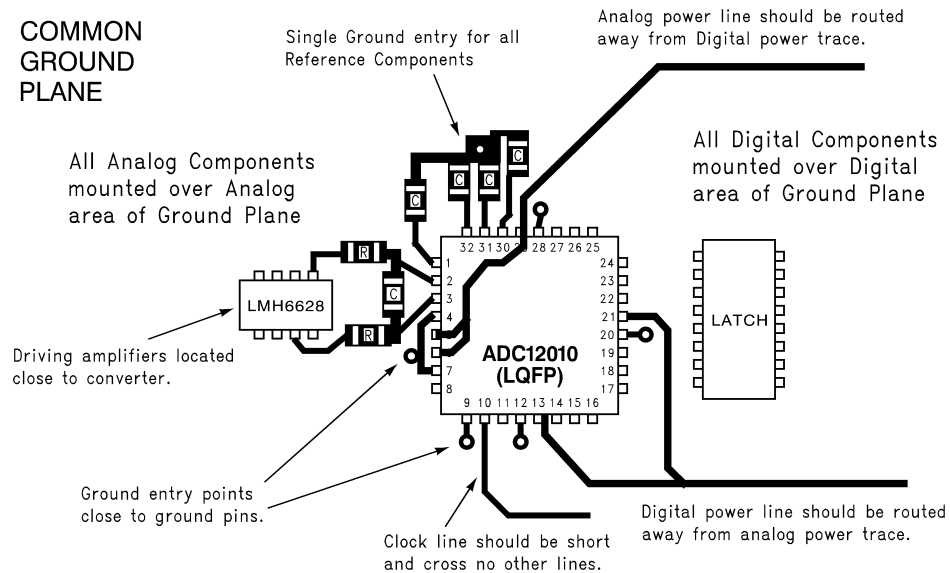


FIGURE 7. Example of a Suitable Layout

## Applications Information (Continued)

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the analog ground plane.

Figure 7 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog ground plane. All digital circuitry and I/O lines should be placed in the digital area of the board. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single point. All ground connections should have a low inductance path to ground.

We do not recommend a split ground plane. Rather, using wide power traces with analog and digital power traces well-separated from each other, and keeping analog and digital signal lines well-separated from each other will minimize noise while keeping EMI to tolerable levels.

### 6.0 DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 8.

As mentioned in Section 5.0, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

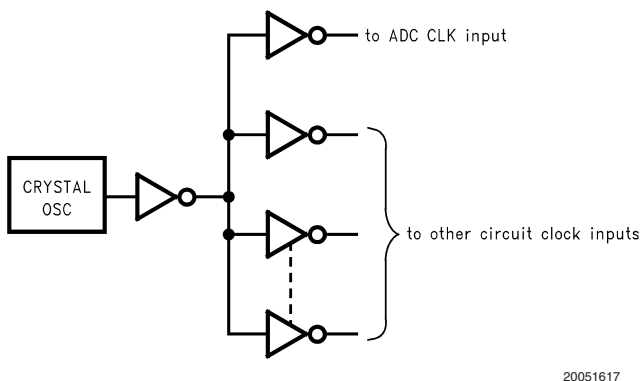


FIGURE 8. Isolating the ADC Clock from other Circuitry with a Clock Tree

### 7.0 COMMON APPLICATION PITFALLS

**Driving the inputs (analog or digital) beyond the power supply rails.** For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply

pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 50Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12010 with a device that is powered from supplies outside the range of the ADC12010 supply. Such practice may lead to conversion inaccuracies and even to device damage.

#### Attempting to drive a high capacitance digital data bus.

The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through  $V_{DR}$  and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the pc board will reduce this problem.

Additionally, bus capacitance beyond the specified 25 pF/pin will cause  $t_{OD}$  to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12010, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 47Ω to 100Ω.

#### Using an inadequate amplifier to drive the analog input.

As explained in Section 1.3, the capacitance seen at the input alternates between 8 pF and 7 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor and shunt capacitor at each amplifier output (as shown in Figure 5) will improve performance. The LMH6702 and the LMH6628 have been successfully used to drive the analog inputs of the ADC12010.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180° out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

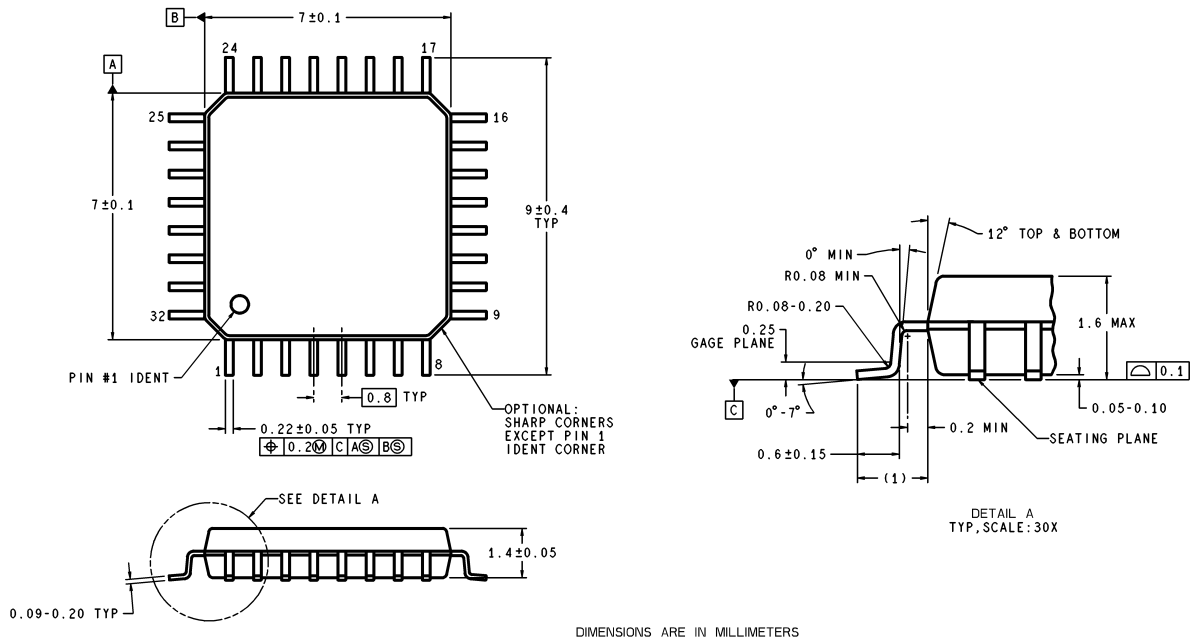
**Operating with the reference pins outside of the specified range.** As mentioned in Section 1.2,  $V_{REF}$  should be in the range of

$$1.0V \leq V_{REF} \leq 2.4V$$

Operating outside of these limits could lead to performance degradation.

**Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace.** This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

## Physical Dimensions inches (millimeters) unless otherwise noted



VBE32A (Rev E)

**32-Lead LQFP Package**  
**Ordering Number ADC12010CIVY**  
**NS Package Number VBE32A**

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