SCDS050D - MARCH 1998 - REVISED OCTOBER 2000

- Member of Texas Instruments' Widebus™ **Family**
- 5- Ω Switch Connection Between Two Ports
- **TTL-Compatible Input and Output Levels**

description

The SN74CBTS16211 provides 24 bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can operate as a dual 12-bit bus switch or as a single 24-bit bus switch. When 10E is low, 1A is connected to 1B. When 2OE is low, 2A is connected to 2B.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

		Т		1
NC	1	O	56	10E
1A1	2		55	20E
1A2	[]3		54] 1B1
1A3	4		53	1B2
1A4	5		52	1B3
1A5	6		51] 1B4
1A6	Q 7		50] 1B5
GND	8		49	GND
1A7	9		48	1B6
1A8	10		47	1B7
1A9	11		46	1B8
1A10	12		45	1B9
1A11	13		44	1B10
1A12	14		43] 1B11
2A1	15		42	1B12
2A2	16		41	2B1
V_{CC}			40	2B2
2A3	18		39	2B3
GND	19		38	GND
2A4	20		37	2B4
2A5	21		36	2B5
2A6	22		35	2B6
2A7	23		34	2B7
2A8	24		33	2B8
2A9	25		32	2B9
2A10	26		31	2B10
2A11	27		30	2B11
2A12	28		29	2B12

NC - No internal connection

ORDERING INFORMATION

TA	PACK	AGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74CBTS16211DL	CBTS16211
-40°C to 85°C	330F - DL	Tape and reel	SN74CBTS16211DLR	CB1310211
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74CBTS16211DGGR	CBTS16211
	TVSOP - DGV	Tape and reel	SN74CBTS16211DGVR	CYS211

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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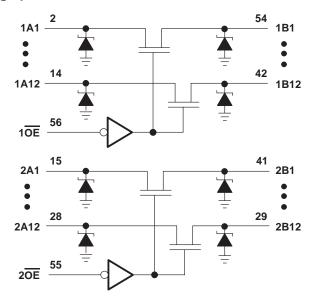
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FUNCTION TABLE (each 12-bit bus switch)

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T _{stq}		. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		MIN	TYP†	MAX	UNIT		
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA				-1.2	V
1.	կլ	$V_{CC} = 5.5 \text{ V},$	V _I = GND				-1	μА
1 ₁	lн	$V_{CC} = 5.5 \text{ V},$	V _I = 5.5 V				150	μΑ
Icc		$V_{CC} = 5.5 \text{ V},$	I _O = 0,	$V_I = V_{CC}$ or GND			3	μΑ
Δl _{CC} ‡	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				3		pF
C _{io(OFF)}		$V_{O} = 3 \text{ V or } 0,$	OE = V _{CC}			5.5		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _I = 15 mA		14	20	
ron§			V _I = 0	I _I = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	V = 0	I _I = 30 mA		5	7	
	V _I = 2.4 V,		I _I = 15 mA		8	12		

 $[\]dagger$ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	= 4 V	VCC =	UNIT	
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.35		0.25	ns
t _{en}	ŌĒ	A or B		9.3	3.3	8.6	ns
t _{dis}	ŌĒ	A or B		7.1	2.8	7.9	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

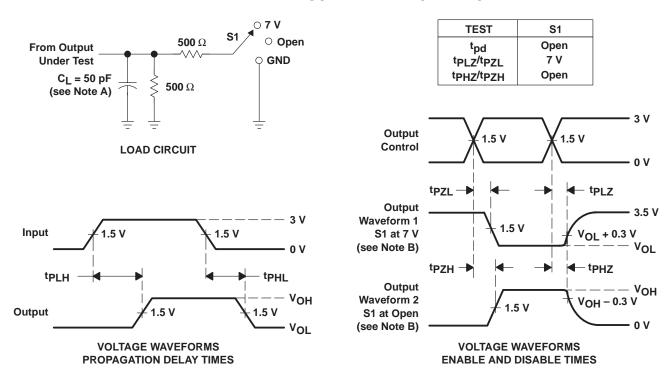


[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CBTS16211DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTS16211DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTS16211DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTS16211DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTS16211DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS16211DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS16211DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS16211DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS16211DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS16211DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

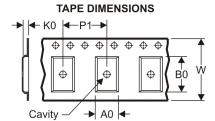
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TAPE AND REEL INFORMATION





Α	١0	Dimension designed to accommodate the component width
В	30	Dimension designed to accommodate the component length
K	(0	Dimension designed to accommodate the component thickness
٧	Ν	Overall width of the carrier tape
F	21	Pitch between successive cavity centers

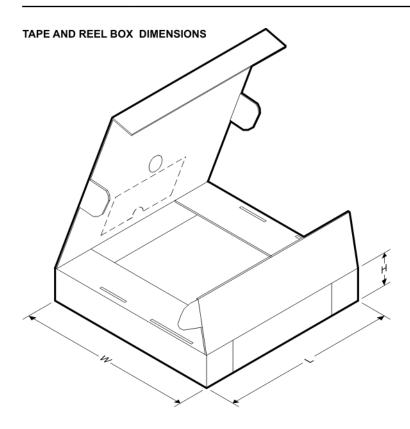
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTS16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBTS16211DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CBTS16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

7 III GITTIOTIOTOTIC GITC TIGITIITIGI							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTS16211DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74CBTS16211DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0
SN74CBTS16211DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



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