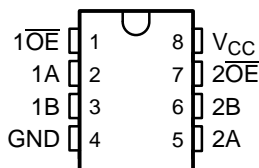


## FEATURES

- Output Voltage Translation Tracks  $V_{CC}$
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
  - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V  $V_{CC}$
  - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V  $V_{CC}$
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 5\ \Omega$  Typ)
- Low Input/Output Capacitance Minimizes Loading ( $C_{io(OFF)} = 4.5\text{ pF}$  Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 20\ \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, USB Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment

DCT OR DCU PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN74CB3T3306 is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks  $V_{CC}$ . The SN74CB3T3306 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see [Figure 1](#)).

The SN74CB3T3306 is organized as two 1-bit bus switches with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	SSOP – DCT	Tape and reel	SN74CB3T3306DCTR	WA6_ _ _
	VSSOP – DCU	Tape and reel	SN74CB3T3306DCUR	WA6_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.  
DCU: The actual top-side marking has one additional character that designates the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

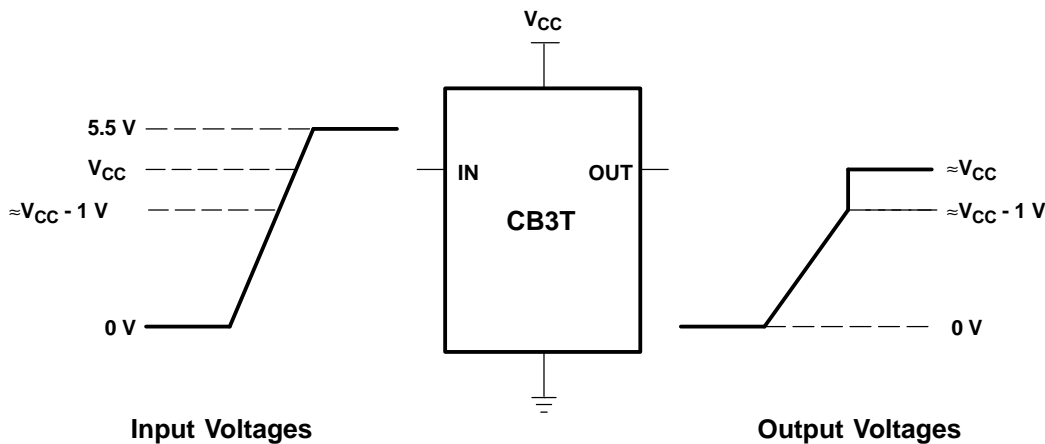
**SN74CB3T3306**  
**DUAL FET BUS SWITCH 2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH**  
**WITH 5-V TOLERANT LEVEL SHIFTER**

SCDS119A—JANUARY 2003—REVISED JUNE 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



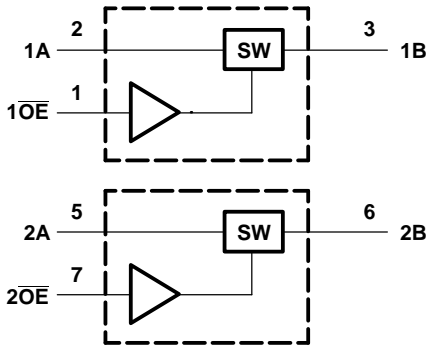
NOTE A: If the input high voltage ( $V_{IH}$ ) level is greater than or equal to  $V_{CC} - 1$  V, and less than or equal to 5.5 V, then the output high voltage ( $V_{OH}$ ) level will be equal to approximately the  $V_{CC}$  voltage level.

**Figure 1. Typical DC Voltage-Translation Characteristics**

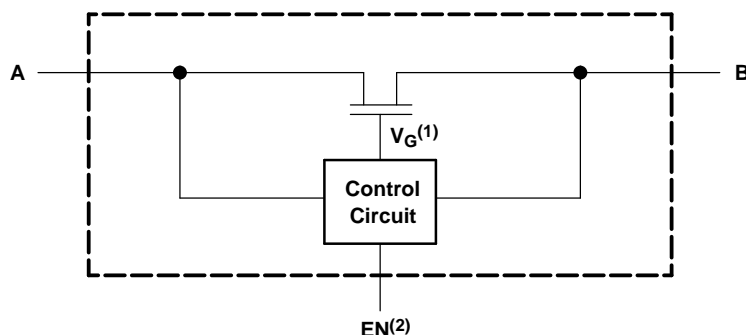
**FUNCTION TABLE**  
**(EACH BUS SWITCH)**

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)**



- (1) Gate voltage ( $V_G$ ) is approximately equal to  $V_{CC} + V_T$  when the switch is ON and  $V_I > V_{CC} + V_T$ .  
(2) EN is the internal enable applied to the switch.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(2)</sup>	−0.5	7	V
$V_{IN}$	Control input voltage range <sup>(2)(3)</sup>	−0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)(4)</sup>	−0.5	7	V
$I_{IK}$	Control input clamp current	$V_{IN} < 0$		−50 mA
$I_{I/O}$	I/O port clamp current	$V_{I/O} < 0$		−50 mA
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		±128	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(6)</sup>	DCT package		220
		DCU package		227
$T_{stg}$	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.  
(2) All voltages are with respect to ground, unless otherwise specified.  
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
(4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .  
(5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .  
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	5.5
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	0.8
$V_{I/O}$	Data input/output voltage	0	5.5	V
$T_A$	Operating free-air temperature	−40	85	°C

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics<sup>(1)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 3\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$		See <a href="#">Figure 3</a> and <a href="#">Figure 4</a>				
$I_{IN}$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_{IN} = 3.6\text{ V}$ to $5.5\text{ V}$ or GND			$\pm 10$	$\mu\text{A}$
$I_I$		$V_{CC} = 3.6\text{ V}$ , Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7\text{ V}$ to $5.5\text{ V}$		$\pm 20$	$\mu\text{A}$
			$V_I = 0.7\text{ V}$ to $V_{CC} - 0.7\text{ V}$		-40	
			$V_I = 0$ to $0.7\text{ V}$		$\pm 5$	
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 3.6\text{ V}$ , $V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND			$\pm 10$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ , $V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$			10	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $I_{I/O} = 0$ , Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND		20	$\mu\text{A}$
			$V_I = 5.5\text{ V}$		20	
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC} = 3\text{ V}$ to $3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND			300	$\mu\text{A}$
$C_{in}$	Control inputs	$V_{CC} = 3.3\text{ V}$ , $V_{IN} = V_{CC}$ or GND			3	pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$ , $V_{I/O} = 5.5\text{ V}$ , $3.3\text{ V}$ , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND			4.5	pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$ , Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5\text{ V}$ or $3.3\text{ V}$		4	pF
			$V_{I/O} = \text{GND}$		15	
$r_{on}$ <sup>(5)</sup>		$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$ , $V_I = 0$	$I_O = 24\text{ mA}$		5	$\Omega$
			$I_O = 16\text{ mA}$		5	
		$V_{CC} = 3\text{ V}$ , $V_I = 0$	$I_O = 64\text{ mA}$		5	
			$I_O = 32\text{ mA}$		5	

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

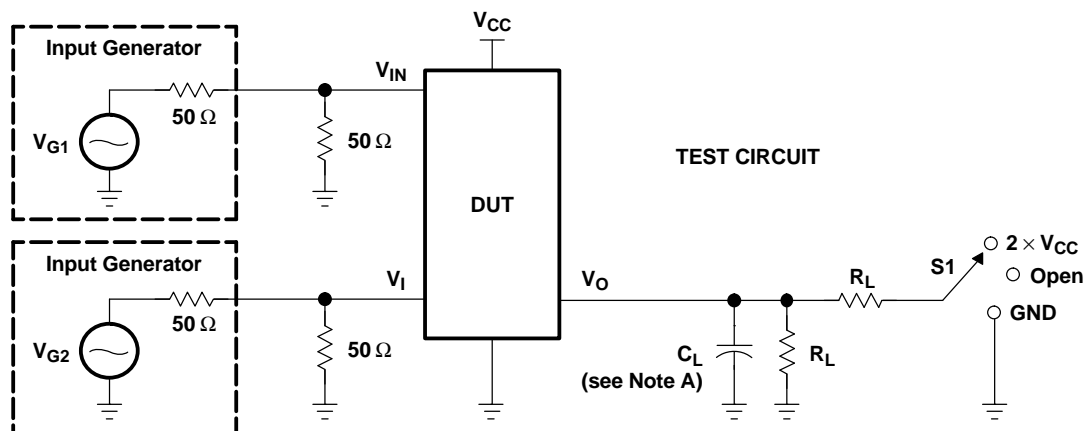
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**Switching Characteristics**over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

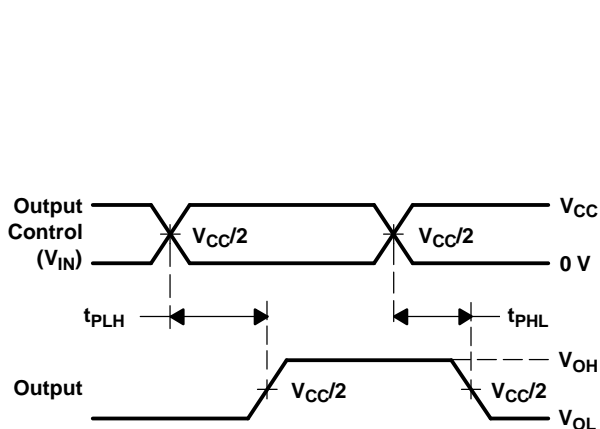
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$ <sup>(1)</sup>	A or B	B or A		0.15		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	1	8.5	1	6.5	ns
$t_{dis}$	$\overline{OE}$	A or B	1	9	1	9	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

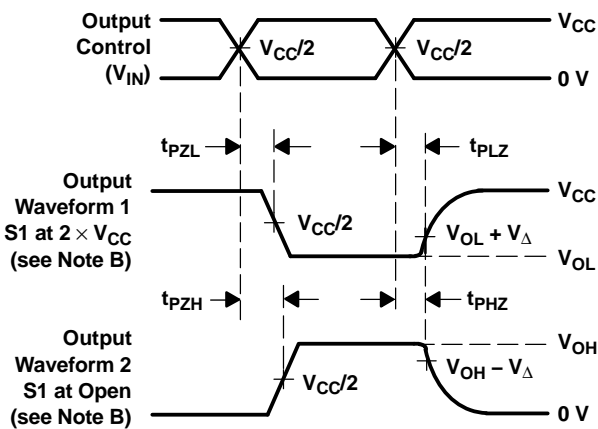
## PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (t<sub>pd(s)</sub>)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PZH</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

## TYPICAL CHARACTERISTICS

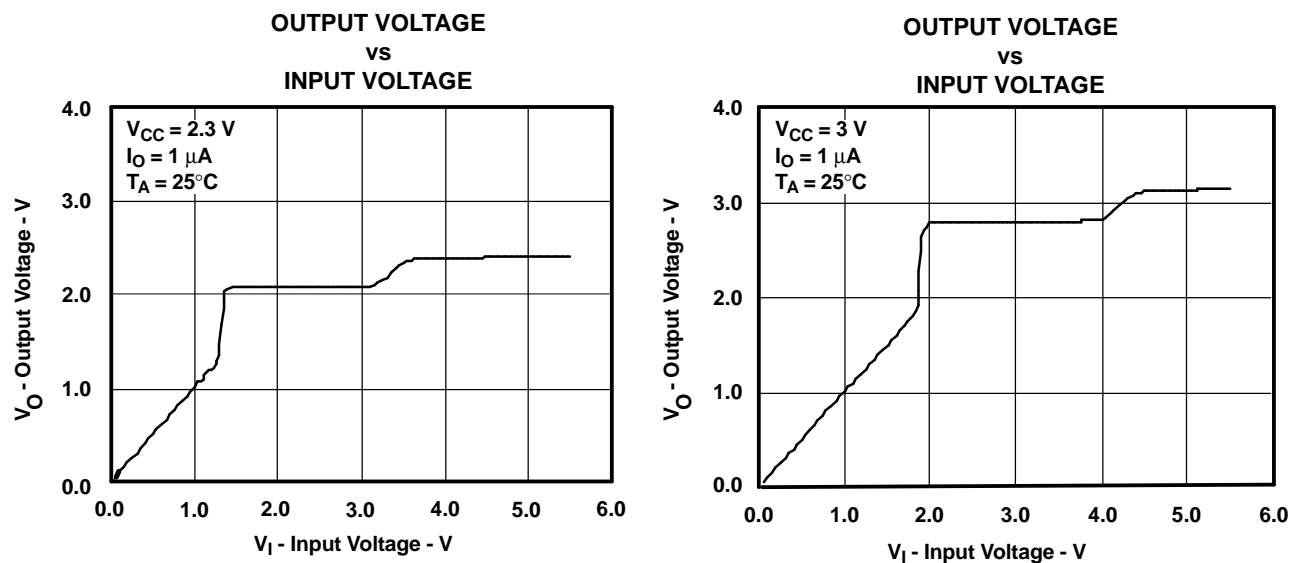


Figure 3. Data Output Voltage vs Data Input Voltage

## TYPICAL CHARACTERISTICS

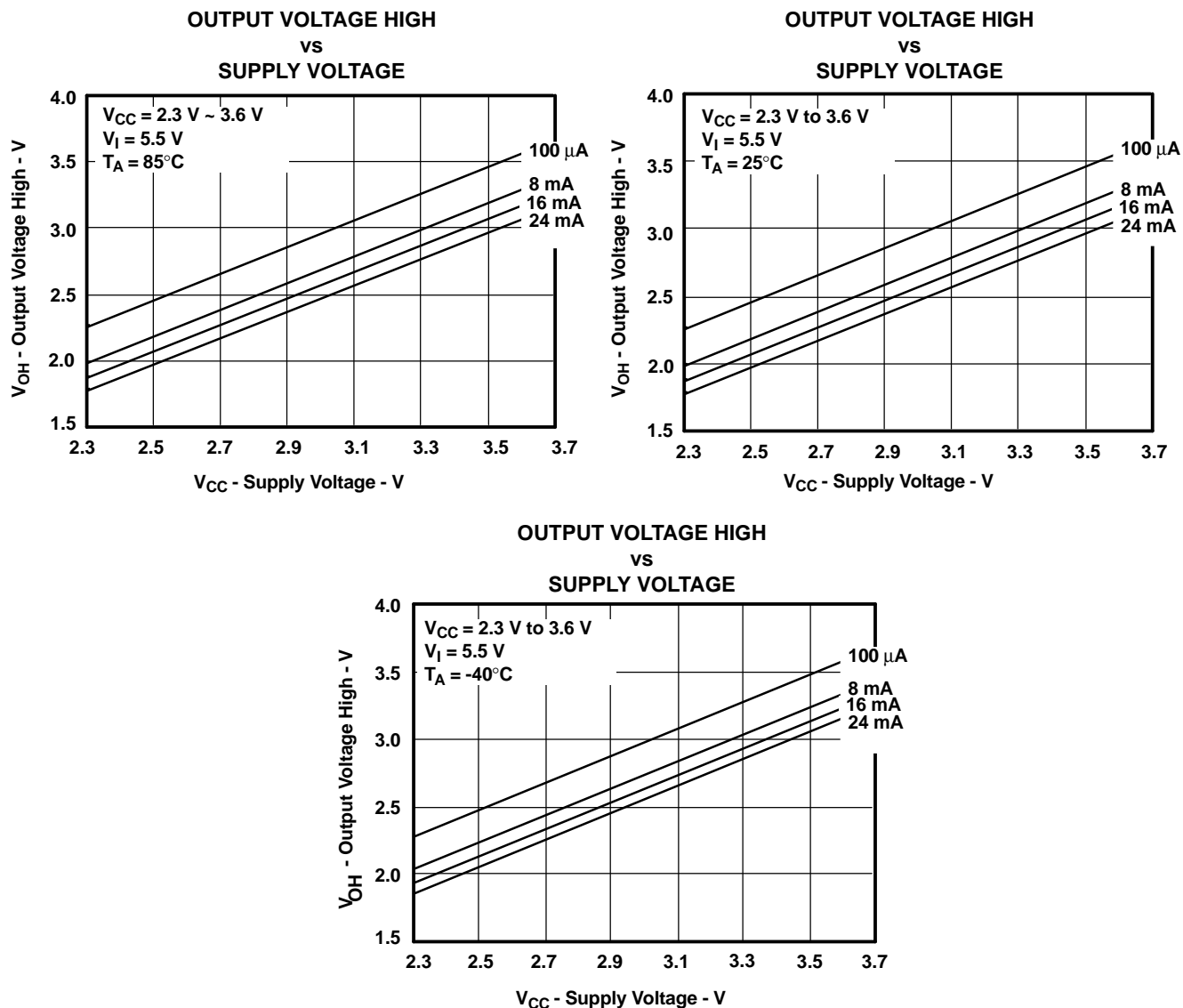


Figure 4.  $V_{OH}$  Values

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CB3T3306DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3T3306DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3T3306DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3306DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3306DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3306DCUR	US8	DCU	8	3000	180.0	9.2	2.25	3.35	1.05	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3306DCUR	US8	DCU	8	3000	202.0	201.0	28.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



## NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

## DCT (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-187 variation DA.

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