

TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
850 μV Max at T_A = 25°C (TLC225xA)
- **Macromodel Included**
- **Performance Upgrades for the TS27L2/L4 and TLC27L2/L4**
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards**

description

The TLC2252 and TLC2254 are dual and quaduple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC225x family consumes only 35 μA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Looking at Figure 1, the TLC225x has a noise level of 19 nV/√Hz at 1kHz; four times lower than competitive micropower solutions.

The TLC225x amplifiers, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC225xA family is available and has a maximum input offset voltage of 850 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2252/4 also makes great upgrades to the TLC27L2/L4 or TS27L2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage ranges, see the TLV2432 and TLV2442 devices. If the design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

**EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY**

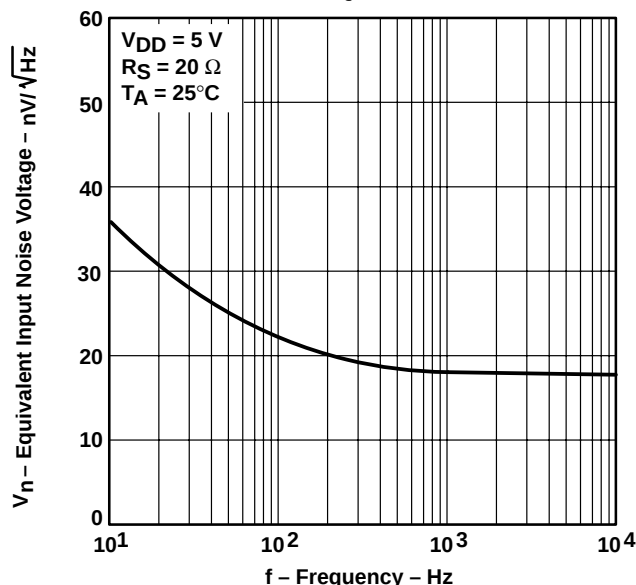


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2252 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	1500 µV	TLC2252CD	—	—	TLC2252CP	TLC2252CPW	—
–40°C to 125°C	850 µV 1500 µV	TLC2252AID TLC2252ID	— —	— —	TLC2252AIP TLC2252IP	TLC2252AIPW —	— —
–40°C to 125°C	850 µV 1500 µV	TLC2252AQD TLC2252QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLC2252AMFK TLC2252MFK	TLC2252AMJG TLC2252MJG	— —	— —	TLC2252AMU TLC2252MU

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR).

‡ The PW package is available only left-ended taped and reeled.

§ Chip forms are tested at 25°C only.

TLC2254 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLATPACK (W)
0°C to 70°C	1500 µV	TLC2254CD	—	—	TLC2254CN	TLC2254CPW	—
–40°C to 125°C	850 µV 1500 µV	TLC2254AID TLC2254ID	— —	— —	TLC2254AIN TLC2254IN	TLC2254AIPW —	— —
–40°C to 125°C	850 µV 1500 µV	TLC2254AQD TLC2254QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLC2254AMFK TLC2254MFK	TLC2254AMJ TLC2254MJ	— —	— —	TLC2254AMW TLC2254MW

† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2254CDR).

‡ The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

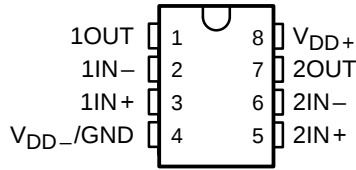
§ Chip forms are tested at 25°C only.



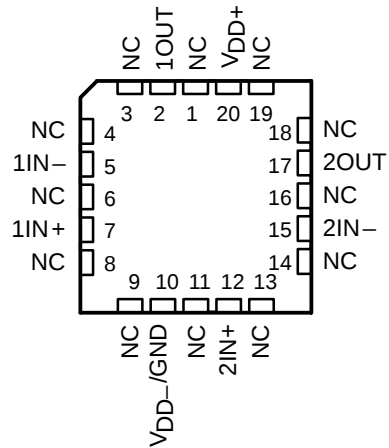
TLC225x, TLC225xA
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SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

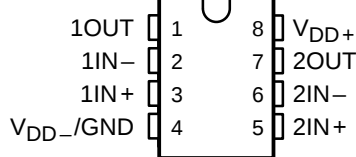
TLC2252C, TLC2252AC
TLC2252I, TLC2252AI
TLC2252Q, TLC2252AQ
D, P, OR PW PACKAGE
(TOP VIEW)



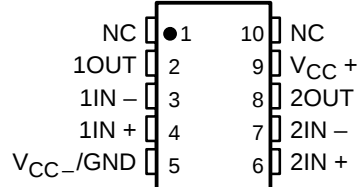
TLC2252M, TLC2252AM . . . FK PACKAGE
(TOP VIEW)



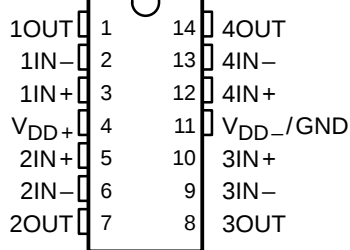
TLC2252M, TLC2252AM . . . JG PACKAGE
(TOP VIEW)



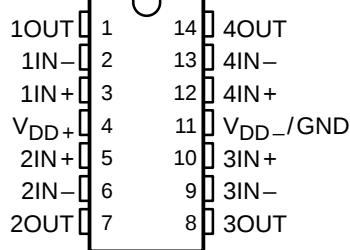
TLC2262M, TLC2252AM . . . U PACKAGE
(TOP VIEW)



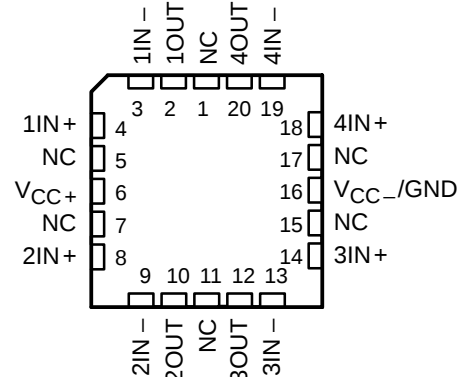
TLC2254C, TLC2254AC
TLC2254I, TLC2254AI
TLC2254Q, TLC2254AQ
D, N, OR PW PACKAGE
(TOP VIEW)



TLC2254M, TLC2254AM
J OR W PACKAGE
(TOP VIEW)



TLC2254M, TLC2254AM
FK PACKAGE
(TOP VIEW)



NC – No internal connection

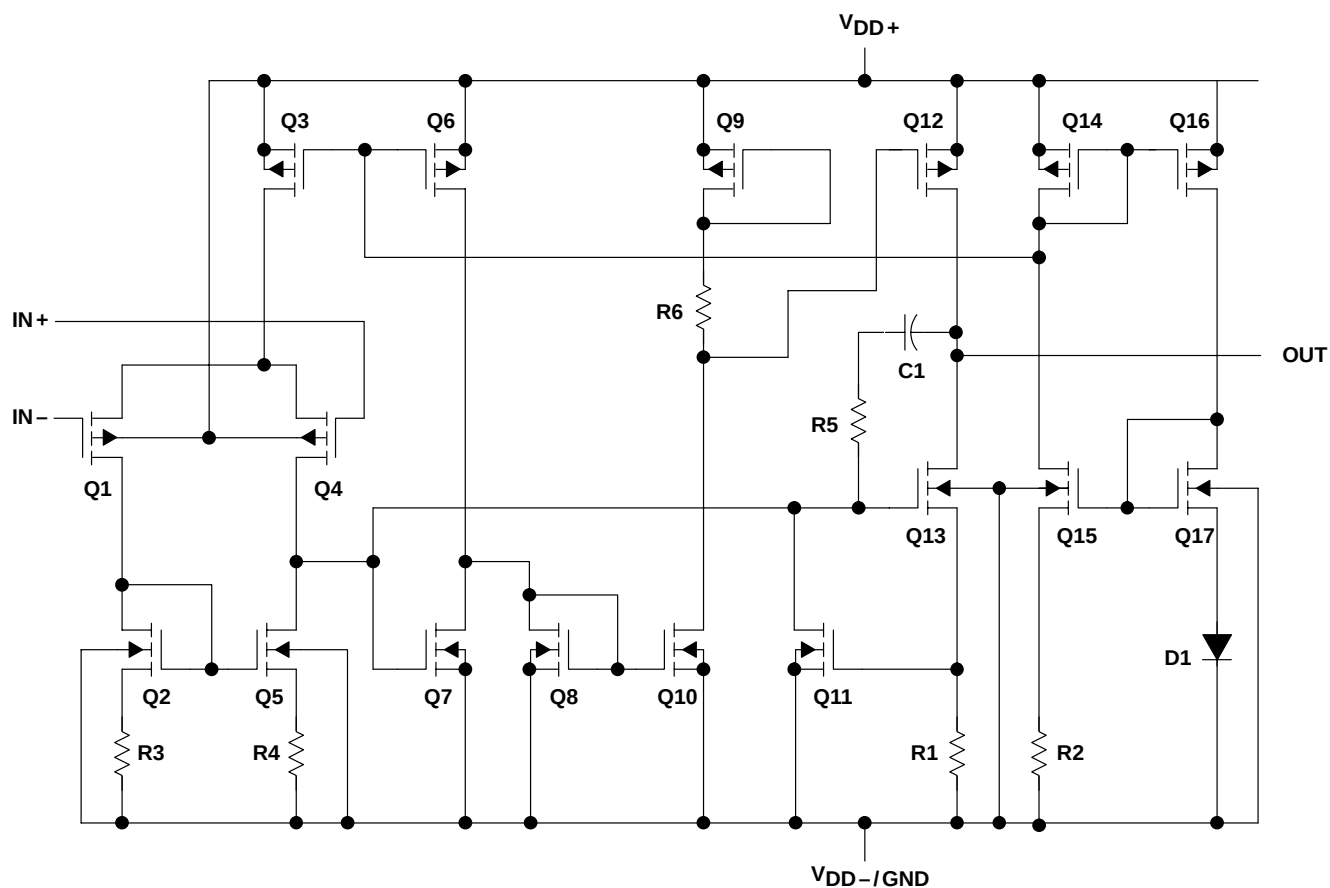
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SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2252	TLC2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	724 mW	5.8 mW/°C	464 mW	377 mW	144 mW
D–14	950 mW	7.6 mW/°C	608 mW	450 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	—
PW–14	700 mW	5.6 mW/°C	448 mW	448 mW	—
U	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW
W	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C

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SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C		200	1500	μV
		Full range			1750	
αV_{IO} Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	–0.3 to 4.2		V
		Full range	0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94	
		Full range		4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88	
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$	25°C		0.01		V
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15	
		Full range			0.15	
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 1\text{ mA}$	25°C		0.2	0.3	
		Full range			0.3	
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 4\text{ mA}$	25°C		0.7	1	
		Full range			1.2	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	V/mV
			Full range	10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700	
r_{id} Differential input resistance		25°C		10^{12}		Ω
r_{ic} Common-mode input resistance		25°C		10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz},$ P package	25°C		8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz},$ $A_V = 10$	25°C		200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83		dB
		Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95		dB
		Full range	80			
I_{DD} Supply current	$V_O = 2.5\text{ V},$ No load	25°C		70	125	μA
		Full range			150	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12	V/μs	
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36		nV/√Hz	
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6		fA/√Hz	
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2		MHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30		kHz	
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] ,	C _L = 100 pF [‡]	25°C	63°			
Gain margin				25°C	15		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

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VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad V_O = 0,$ $R_S = 50 \, \Omega$	25°C		200	1500	μV
		Full range			1750	
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu V/mo$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5 \text{ mV}, \quad R_S = 50 \, \Omega$	25°C	–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \, \mu A$	25°C		4.98		V
	$I_O = -100 \, \mu A$	25°C		4.9	4.93	
		Full range		4.7		
	$I_O = -200 \, \mu A$	25°C		4.8	4.86	
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, \quad I_O = 50 \, \mu A$	25°C		–4.99		V
	$V_{IC} = 0, \quad I_O = 500 \, \mu A$	25°C		–4.85	–4.91	
		Full range		–4.85		
	$V_{IC} = 0, \quad I_O = 1 \text{ mA}$	25°C		–4.7	–4.8	
		Full range		–4.7		
	$V_{IC} = 0, \quad I_O = 4 \text{ mA}$	25°C		–4	–4.3	
		Full range		–3.8		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4 \text{ V}$	$R_L = 100 \text{ k}\Omega$	25°C	45	650	V/mV
			Full range	10		
		$R_L = 1 \text{ M}\Omega$	25°C	3000		
r_{id} Differential input resistance		25°C		10^{12}		Ω
r_{ic} Common-mode input resistance		25°C		10^{12}		Ω
C_{ic} Common-mode input capacitance	$f = 10 \text{ kHz}, \quad \text{P package}$	25°C		8		pF
Z_O Closed-loop output impedance	$f = 25 \text{ kHz}, \quad A_V = 10$	25°C		190		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5 \text{ V to } 2.7 \text{ V},$ $V_O = 0, \quad R_S = 50 \, \Omega$	25°C		75	88	dB
		Full range		75		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = 2.2 \text{ V to } \pm 8 \text{ V},$ $V_{IC} = 0, \quad \text{No load}$	25°C		80	95	dB
		Full range		80		
I_{DD} Supply current	$V_O = 0, \quad \text{No load}$	25°C		80	125	μA
		Full range			150	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12	V/μs	
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38		nV/√Hz	
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6		fA/√Hz	
THD + N	Total harmonic distortion pulse duration	V _O = ±2.3 V, f = 10 kHz, R _L = 50 kΩ	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21		MHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14		kHz	
φ _m	Phase margin at unity gain	R _L = 50 kΩ,	C _L = 100 pF	25°C	63°			
Gain margin				25°C	15		dB	

[†] Full range is 0°C to 70°C.

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SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, V_{DD} \pm \pm 2.5\text{ V}, R_S = 50\ \Omega$	25°C		200	1500	μV
		Full range			1750	
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	–0.3 to 4.2		V
		Full range		0 to 3.5		
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94	
		Full range		4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88	V
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		0.01		
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15	
		Full range			0.15	
	$V_{IC} = 2.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C		0.2	0.3	
		Full range			0.3	
	$V_{IC} = 2.5\text{ V}, I_{OL} = 4\text{ mA}$	25°C		0.7	1	
		Full range			1.2	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	V/mV
			Full range	10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C		8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C		200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C		70	83	dB
		Full range		70		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C		80	95	dB
		Full range		80		
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}, \text{ No load}$	25°C		140	250	μA
		Full range			300	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.4 V to 2.6 V R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12	V/μs	
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36		nV/√Hz	
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6		fA/√Hz	
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2		MHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30		kHz	
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] ,	C _L = 100 pF [‡]	25°C	63°			
	Gain margin				25°C	15		dB

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$	25°C		200	1500	μV
		Full range			1750	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 70°C		0.5		$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu V/mo$
I_{IO} Input offset current		25°C		0.5	60	pA
		Full range			100	
I_{IB} Input bias current		25°C		1	60	pA
		Full range			100	
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5$ mV, $R_S = 50 \Omega$	25°C	–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \mu A$	25°C		4.98		V
	$I_O = -100 \mu A$	25°C		4.9	4.93	
		Full range		4.7		
	$I_O = -200 \mu A$	25°C		4.8	4.86	
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50 \mu A$	25°C		–4.99		V
	$V_{IC} = 0, I_O = 500 \mu A$	25°C		–4.85	–4.91	
		Full range		–4.85		
	$V_{IC} = 0, I_O = 1$ mA	25°C		–4.7	–4.8	
		Full range		–4.7		
	$V_{IC} = 0, I_O = 4$ mA	25°C		–4	–4.3	
		Full range		–3.8		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 100$ k Ω	25°C	40	150	V/mV
			Full range	10		
		$R_L = 1$ M Ω	25°C		3000	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10$ kHz, N package	25°C		8		pF
z_O Closed-loop output impedance	$f = 25$ kHz, $A_V = 10$	25°C		190		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0, R_S = 50 \Omega$	25°C		75	88	dB
		Full range		75		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = 0$, No load	25°C		80	95	dB
		Full range		80		
I_{DD} Supply current (four amplifiers)	$V_O = 0$, No load	25°C		160	250	μA
		Full range			300	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		V/μs
				Full range	0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			nV/√Hz
		f = 1 kHz		25°C	19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I _n	Equivalent input noise current			25°C	0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ± 2.3 V, f = 20 kHz, R _L = 50 kΩ	A _V = 1	25°C	0.2%			
			A _V = 10		1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ,	C _L = 100 pF	25°C	63°			
Gain margin					25°C	15		

[†] Full range is 0°C to 70°C.

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω		25°C	200	1500		200	850	μV	
	Full range			1750			1000				
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 85°C	0.5			0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				Full range	1000			1000			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				Full range	1000			1000			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2	V		
			Full range	0 to 3.5		0 to 3.5					
V _{OH}	High-level output voltage	I _{OH} = −20 μA	25°C	4.98			4.98			V	
		I _{OH} = −75 μA	25°C	4.9	4.94		4.9	4.94			
			Full range	4.8			4.8				
		I _{OH} = −150 μA	25°C	4.8	4.88		4.8	4.88			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA	25°C	0.01			0.01			V	
		V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.09	0.15		0.09	0.15			
			Full range	0.15			0.15				
		V _{IC} = 2.5 V, I _{OL} = 4 mA	25°C	0.8	1		0.7	1			
			Full range	1.2			1.2				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 100 kΩ [‡]	25°C	100	350		100	350	V/mV	
				Full range	10			10			
			R _L = 1 MΩ [‡]	25°C	1700			1700			
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _{ic}	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8			8			pF
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	200			200			Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω		25°C	70	83		70	83	dB	
				Full range	70			70			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	70	125		70	125	μA	
				Full range	150			150			

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A †	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, R _L = 50 kΩ [‡] ,	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] , C _L = 100 pF [‡]		25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200	1500		200	850	μV	
	Full range			1750			1000				
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 85°C	0.5			0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				Full range	1000			1000			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				Full range	1000			1000			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2	V	
				Full range	−5 to 3.5			−5 to 3.5			
V _{OM+}	Maximum positive peak output voltage	I _O = −20 μA		25°C	4.98			4.98			V
		I _O = −100 μA		25°C	4.9	4.93		4.9	4.93		
				Full range	4.7			4.7			
		I _O = −200 μA		25°C	4.8	4.86		4.8	4.86		
V _{OM−}	Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA		25°C	−4.99			−4.99			V
		V _{IC} = 0, I _O = 500 μA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V _{IC} = 0, I _O = 4 mA		25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
		A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 50 kΩ	25°C	40	150		40	
	Full range				10			10			
R _L = 1 MΩ	25°C				3000			3000			
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _{ic}	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8			8			pF
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	190			190			Ω
CMRR	Common-mode rejection ratio	V _{IC} = −5 V to 2.7 V, V _O = 0, R _S = 50 Ω		25°C	75	88		75	88	dB	
				Full range	75			75			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	80	125		80	125	μA	
				Full range	150			150			

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A †	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 10 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f=10 kHz, R _L = 50 kΩ, C _L = 100 pF		25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, A _V = 1, R _L = 50 kΩ, C _L = 100 pF		25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ, C _L = 100 pF		25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is -40°C to 125°C .

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254I			TLC2254AI			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	V _{DD} ± = ±2.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200		1500	200		850	μV	
	Full range					1750	1000					
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C	0.5				0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003				0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5		60	0.5		60	pA	
				Full range			1000	1000				
I _{IB}	Input bias current			25°C	1		60	1		60	pA	
				Full range			1000	1000				
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤5 mV	25°C	0 to 4	−0.3 to 4.2			0 to 4	−0.3 to 4.2	V		
			Full range	0 to 3.5		0 to 3.5						
V _{OH}	High-level output voltage	I _{OH} = −20 μA		25°C	4.98		4.98		V			
		I _{OH} = −75 μA		25°C	4.9	4.94	4.9	4.94				
				Full range	4.8		4.8					
		I _{OH} = −150 μA		25°C	4.8	4.88	4.8	4.88				
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA	25°C	0.01		0.01		V				
		V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.09	0.15	0.09	0.15					
			Full range	0.15		0.15						
		V _{IC} = 2.5 V, I _{OL} = 4 mA	25°C	0.8	1	0.7	1					
			Full range	1.2		1.2						
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 100 kΩ [‡]	25°C	100	350	100	350	V/mV			
				Full range	10		10					
			R _L = 1 MΩ [‡]	25°C	1700		1700					
r _{i(d)}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω			
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω			
c _{i(c)}	Common-mode input capacitance	f = 10 kHz, N package	25°C	8		8		pF				
z _o	Closed-loop output impedance	f = 25 kHz, A _V = 10	25°C	200		200		Ω				
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω	25°C	70	83	70	83	dB				
			Full range	70		70						
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load	25°C	80	95	80	95	dB				
			Full range	80		80						
I _{DD}	Supply current (four amplifiers)	V _O = 2.5 V, No load	25°C	140	250	140	250	μA				
			Full range	300		300						

† Full range is -40°C to 125°C .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.4\text{ V to }2.6\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$		25°C	0.07	0.12		0.07	0.12		V/ μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		36			36		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		0.7			0.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$	$C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200	1500	200	850	μV		
	Full range			1750			1000				
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C	0.5			0.5		μV/°C	
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003		μV/mo	
I _{IO}	Input offset current			25°C	0.5	60	0.5	60	pA		
				Full range	1000			1000			
I _{IB}	Input bias current			25°C	1	60	1	60	pA		
				Full range	1000			1000			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	–5 to 4	–5.3 to 4.2	–5 to 4	–5.3 to 4.2	V		
				Full range	–5 to 3.5		–5 to 3.5				
V _{OM+}	Maximum positive peak output voltage	I _O = –20 μA		25°C	4.98		4.98		V		
		I _O = –100 μA		25°C	4.9	4.93	4.9	4.93			
				Full range	4.7		4.7				
		I _O = –200 μA		25°C	4.8	4.86	4.8	4.86			
V _{OM–}	Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA		25°C	–4.99		–4.99		V		
		V _{IC} = 0, I _O = 500 μA		25°C	–4.85	–4.91	–4.85	–4.91			
				Full range	–4.85		–4.85				
		V _{IC} = 0, I _O = 4 mA		25°C	–4	–4.3	–4	–4.3			
				Full range	–3.8		–3.8				
A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 100 kΩ	25°C	40	150	40	150	V/mV		
				Full range	10		10				
			R _L = 1 MΩ	25°C	3000		3000				
r _{i(d)}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _{i(c)}	Common-mode input capacitance	f = 10 kHz,	N package	25°C	8		8		pF		
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	190		190		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = –5 V to 2.7 V, V _O = 0, R _S = 50 Ω		25°C	75	88	75	88	dB		
				Full range	75		75				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ±2.2 V to ±8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95	80	95	dB		
				Full range	80		80				
I _{DD}	Supply current (four amplifiers)	V _O = 0, No load		25°C	160	250	160	250	μA		
				Full range	300		300				

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±1.9 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 20 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ, C _L = 100 pF		25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is -40°C to 125°C .

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98			4.98			V
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		4.9	4.94		
		Full range	4.8			4.8			
	$I_{OH} = -150\ \mu\text{A}$	25°C	4.8	4.88		4.8	4.88		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01			V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C	0.8	1		0.7	1		
		Full range		1.2			1.2		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	100	350		V/mV
			Full range	10		10			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	1700		1700			
r_{id} Differential input resistance		25°C	10^{12}			10^{12}			Ω
r_{ic} Common-mode input resistance		25°C	10^{12}			10^{12}			Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$, $f = 10\text{ kHz}$	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200			200			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C	70	125		70	125		μA
		Full range		150			150		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05		0.05				
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] ,	C _L = 100 pF [‡]	25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.98			4.98			V
	$I_O = -100\ \mu\text{A}$	25°C	4.9	4.93		4.9	4.93		
		Full range	4.7			4.7			
	$I_O = -200\ \mu\text{A}$	25°C	4.8	4.86		4.8	4.86		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C	–4.99			–4.99			V
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	25°C	–4.85	–4.91		–4.85	–4.91		
		Full range	–4.85			–4.85			
	$V_{IC} = 0, I_O = 4\text{ mA}$	25°C	–4	–4.3		–4	–4.3		
		Full range	–3.8			–3.8			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 100\text{ k}\Omega$	25°C	40	150	40	150		V/mV
			Full range	10		10			
		$R_L = 1\text{ M}\Omega$	25°C	3000		3000			
r_{id} Differential input resistance		25°C	10^{12}			10^{12}			Ω
r_{ic} Common-mode input resistance		25°C	10^{12}			10^{12}			Ω
C_{ic} Common-mode input capacitance	$f = 10\text{ kHz}, \text{ P package}$	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C	190			190			Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = 0, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	80	125		80	125		μA
		Full range		150			150		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS
SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±2 V, R _L = 100 kΩ, C _L = 100 pF		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 10 kHz		25°C	0.2%			0.2%			
		A _V = 1 A _V = 10			1%			1%			
Gain-bandwidth product		f = 10 kHz, R _L = 50 kΩ, C _L = 100 pF		25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ, A _V = 1, C _L = 100 pF		25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ, C _L = 100 pF		25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500		200	850	μV
		Full range			1750			1000	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C		0.5			0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		125°C			1000			1000	
I_{IB} Input bias current		25°C		1	60		1	60	pA
		125°C			1000			1000	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98			4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94		4.9	4.94	
		Full range		4.8			4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88		4.8	4.88	
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15		0.09	0.15	
		Full range			0.15			0.15	
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C		0.8	1		0.7	1	
		Full range			1.2			1.2	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to } 4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350		100	350	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700			1700	
$r_{i(d)}$ Differential input resistance		25°C		10 ¹²			10 ¹²		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10 ¹²			10 ¹²		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C		200			200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to } 16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C		140	250		140	250	μA
		Full range			300			300	

† Full range is –40°C to 125°C for Q suffix, –55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 0.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$		25°C	0.07	0.12		0.07	0.12		V/ μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		36			36		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		0.7			0.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$	$C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		125°C		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		125°C		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.98			4.98			V
	$I_O = -100\ \mu\text{A}$	25°C	4.9	4.93		4.9	4.93		
		Full range	4.7			4.7			
	$I_O = -200\ \mu\text{A}$	25°C	4.8	4.86		4.8	4.86		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C	–4.99			–4.99			V
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	25°C	–4.85	–4.91		–4.85	–4.91		
		Full range	–4.85			–4.85			
	$V_{IC} = 0, I_O = 4\text{ mA}$	25°C	–4	–4.3		–4	–4.3		
		Full range	–3.8			–3.8			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 100\text{ k}\Omega$	25°C	40	150	40	150		V/mV
			Full range	10		10			
		$R_L = 1\text{ M}\Omega$	25°C	3000		3000			
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²			Ω
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²			Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C	190			190			Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 0, \text{ No load}$	25°C	160	250		160	250		μA
		Full range		300			300		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS
SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±2 V, C _L = 100 pF	R _L = 100 kΩ,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 20 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ,	C _L = 100 pF	25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	2 – 5 6, 7
αV_{IO}	Input offset voltage temperature coefficient	Distribution	8 – 11
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	12
V_I	Input voltage range	vs Supply voltage vs Free-air temperature	13 14
V_{OH}	High-level output voltage	vs High-level output current	15
V_{OL}	Low-level output voltage	vs Low-level output current	16, 17
V_{OM+}	Maximum positive peak output voltage	vs Output current	18
V_{OM-}	Maximum negative peak output voltage	vs Output current	19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	21 22
V_O	Output voltage	vs Differential input voltage	23, 24
	Differential gain	vs Load resistance	25
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26, 27 28, 29
z_o	Output impedance	vs Frequency	30, 31
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	32 33
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	34, 35 36
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	37 38
SR	Slew rate	vs Load capacitance vs Free-air temperature	39 40
V_O	Inverting large-signal pulse response		41, 42
V_O	Voltage-follower large-signal pulse response		43, 44
V_O	Inverting small-signal pulse response		45, 46
V_O	Voltage-follower small-signal pulse response		47, 48
V_n	Equivalent input noise voltage	vs Frequency	49, 50
	Noise voltage (referred to input)	Over a 10-second period	51
	Integrated noise voltage	vs Frequency	52
THD + N	Total harmonic distortion plus noise	vs Frequency	53
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	54 55
ϕ_m	Phase margin	vs Frequency vs Load capacitance	26, 27 56
A_m	Gain margin	vs Load capacitance	57
B_1	Unity-gain bandwidth	vs Load capacitance	58
	Overestimation of phase margin	vs Load capacitance	59

TYPICAL CHARACTERISTICS

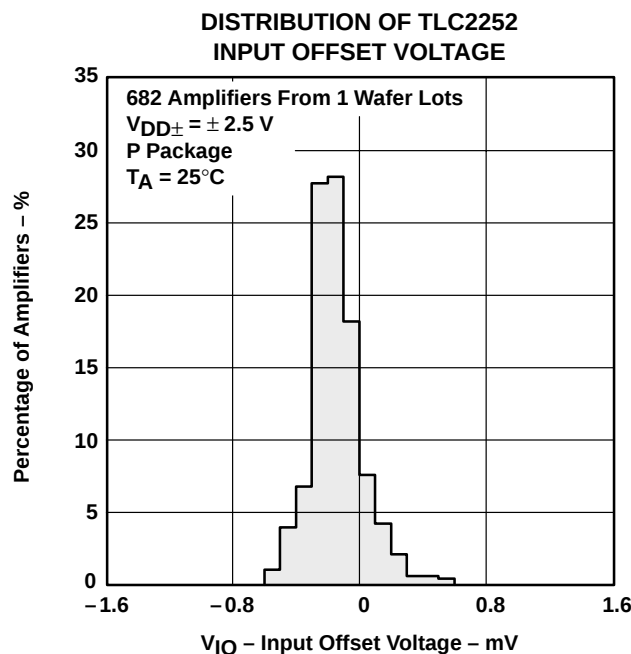


Figure 2

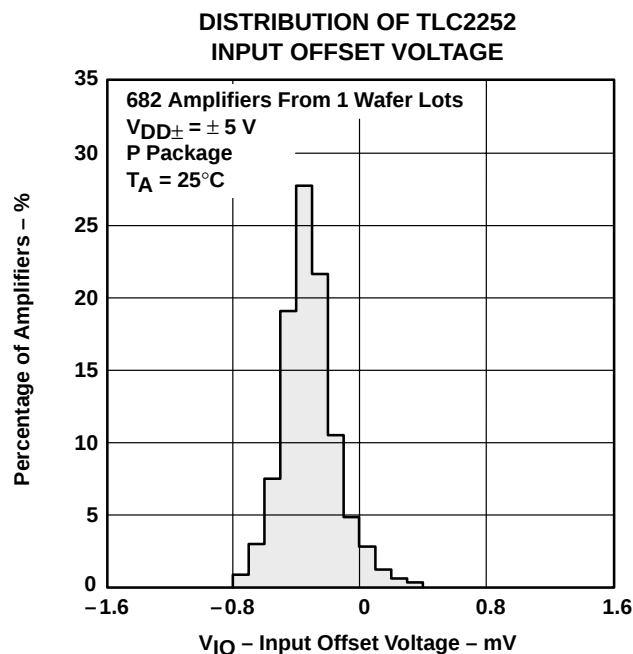


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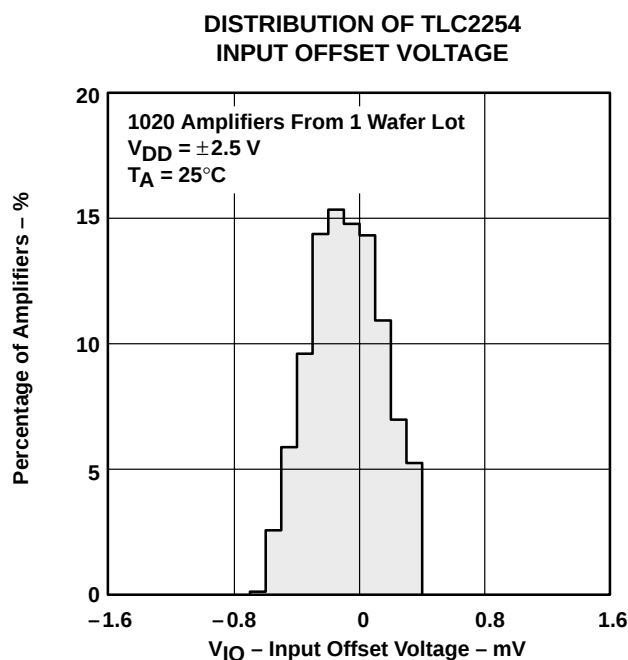


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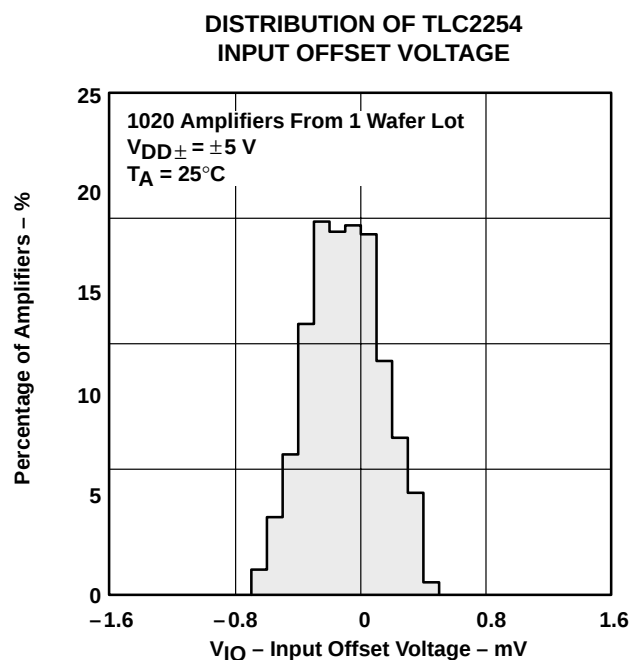


Figure 5

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

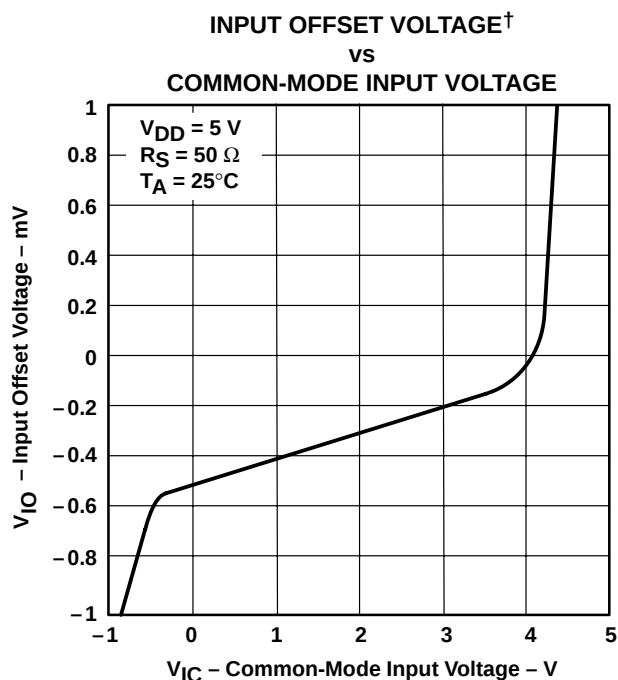


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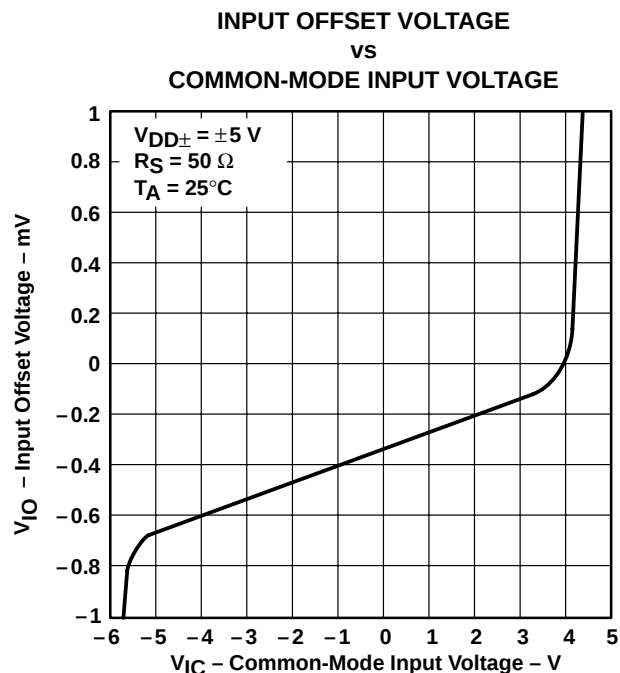


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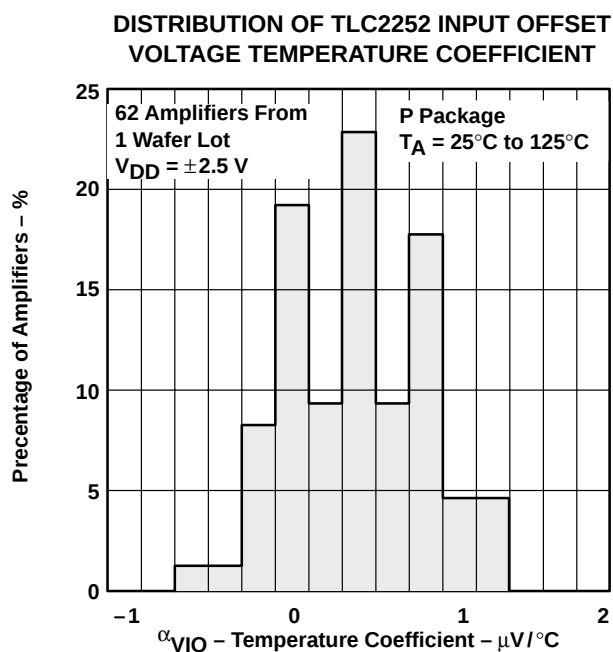


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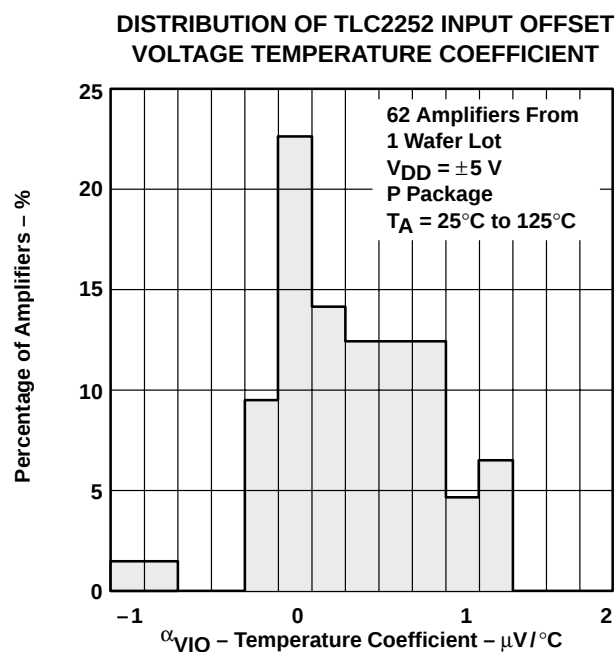


Figure 9

[†] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

TYPICAL CHARACTERISTICS

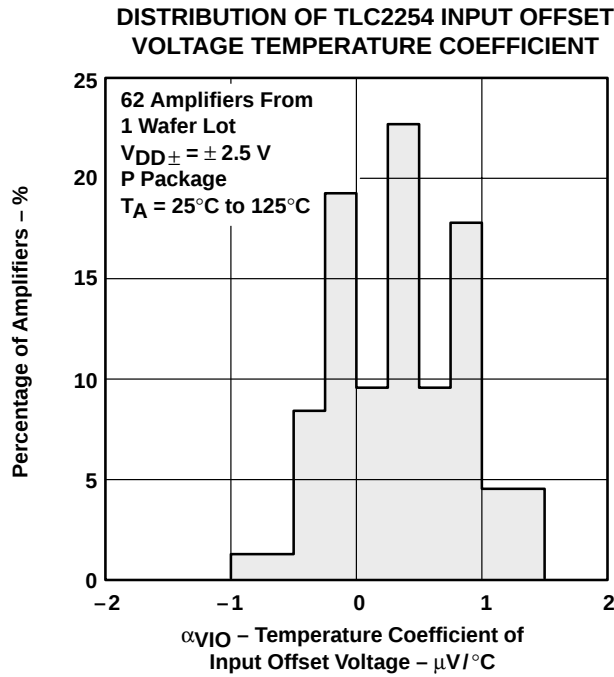


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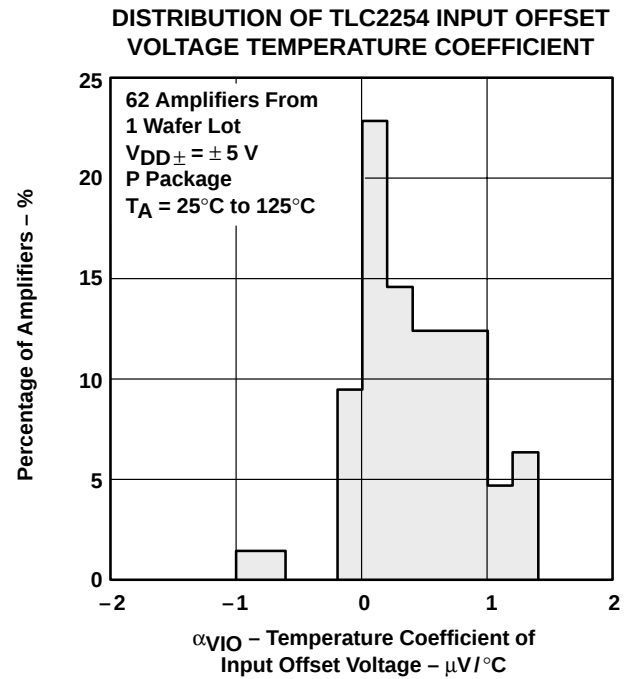


Figure 11

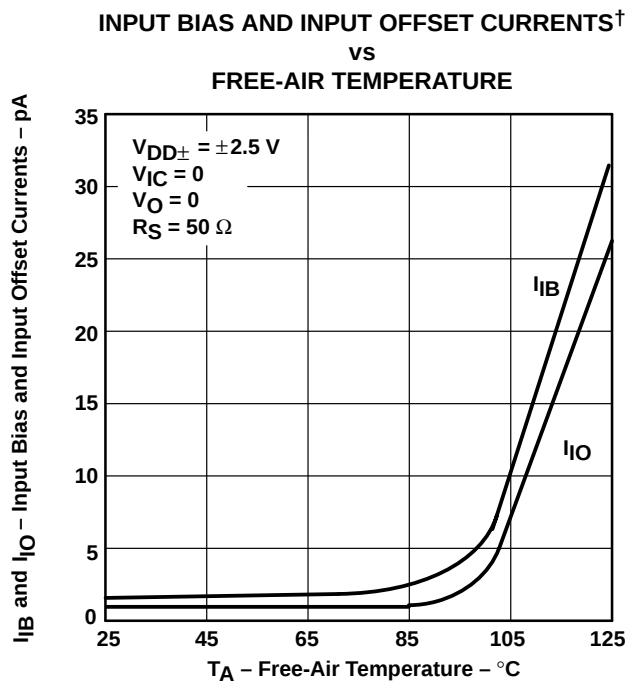


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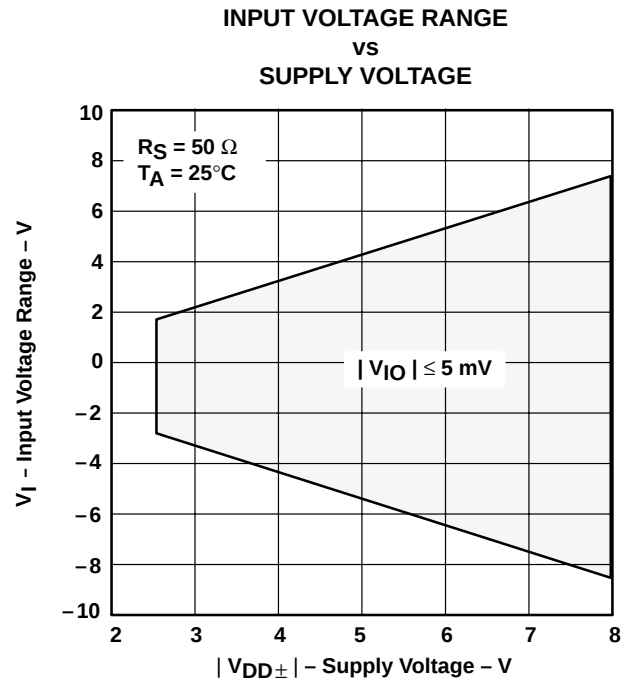


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

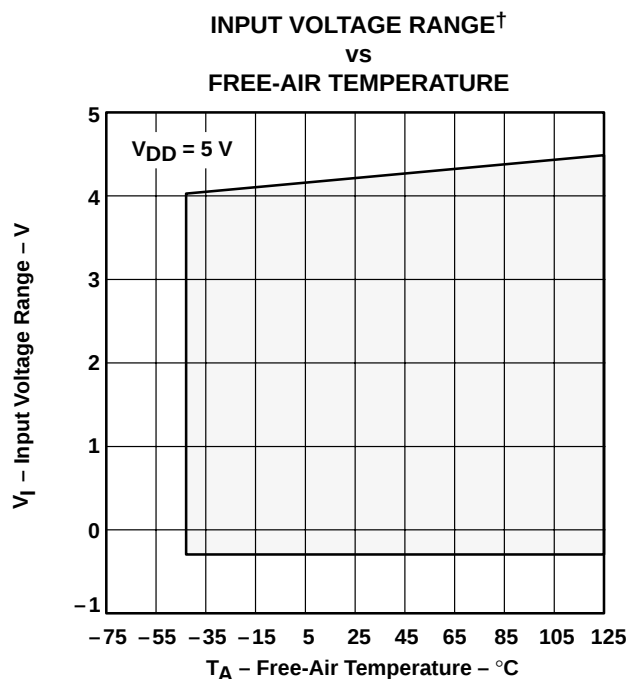


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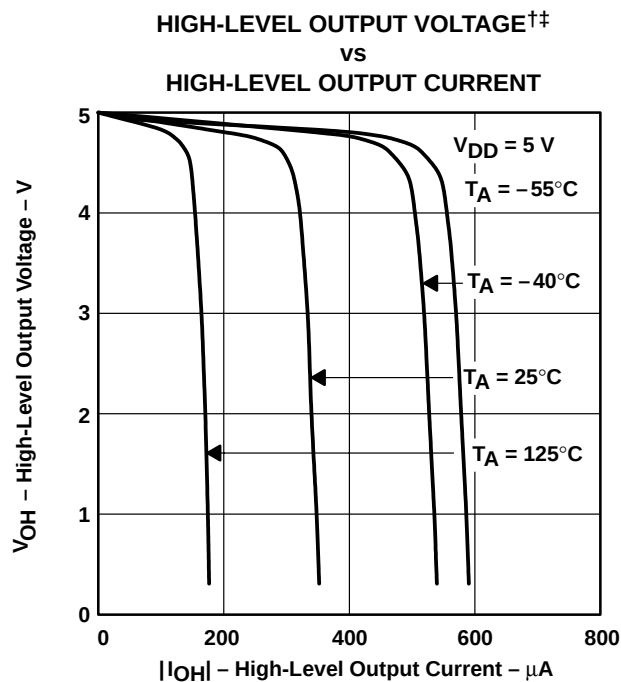


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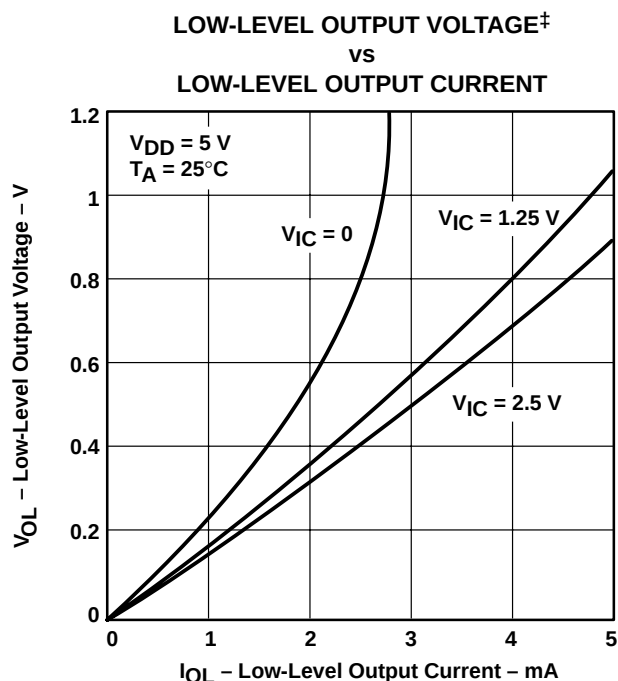


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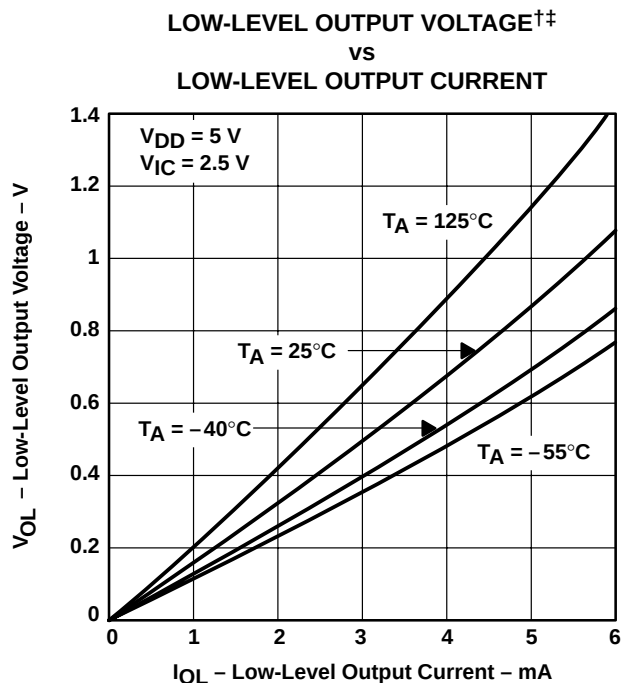
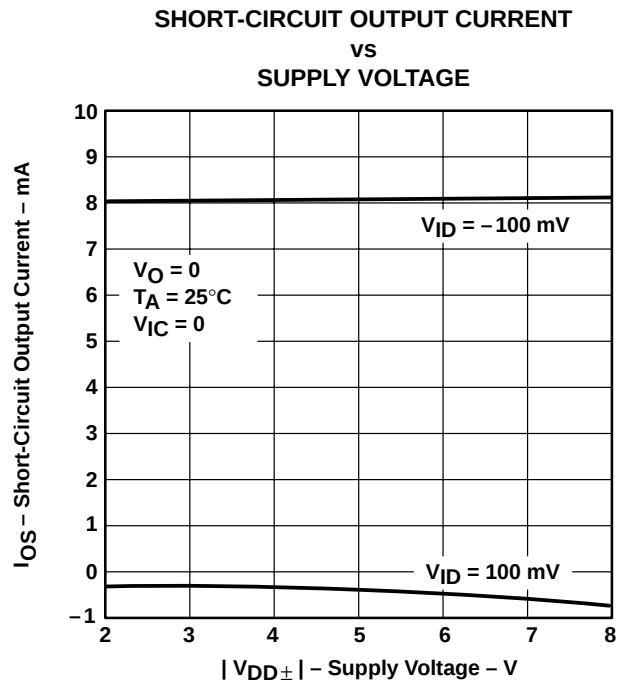
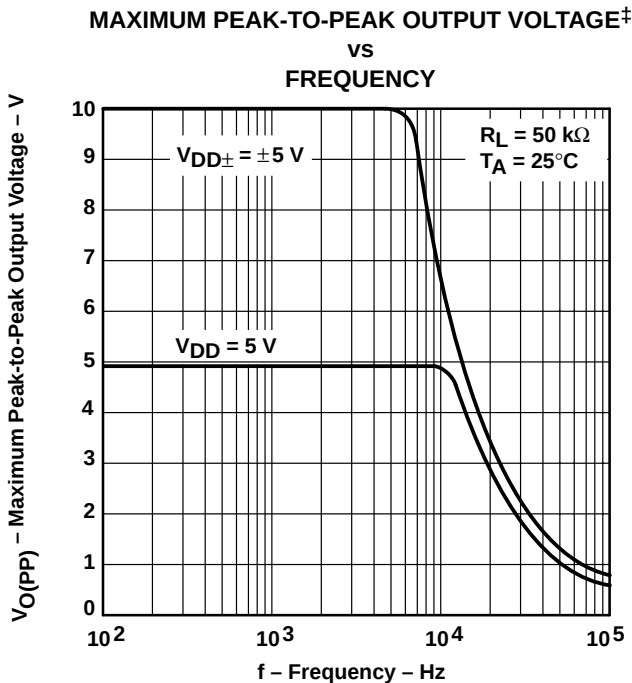
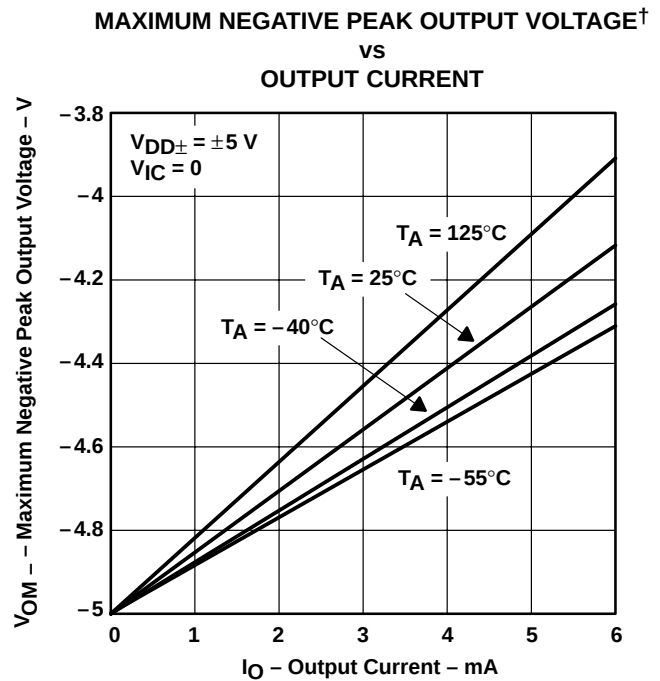
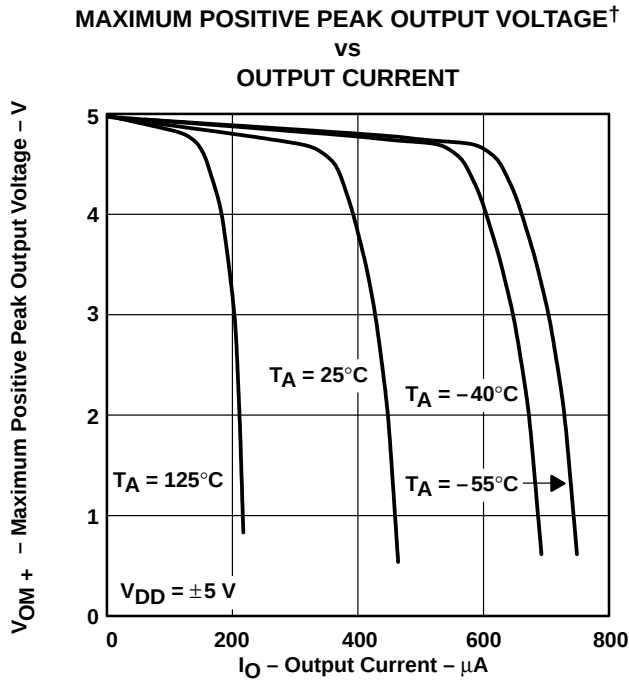


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

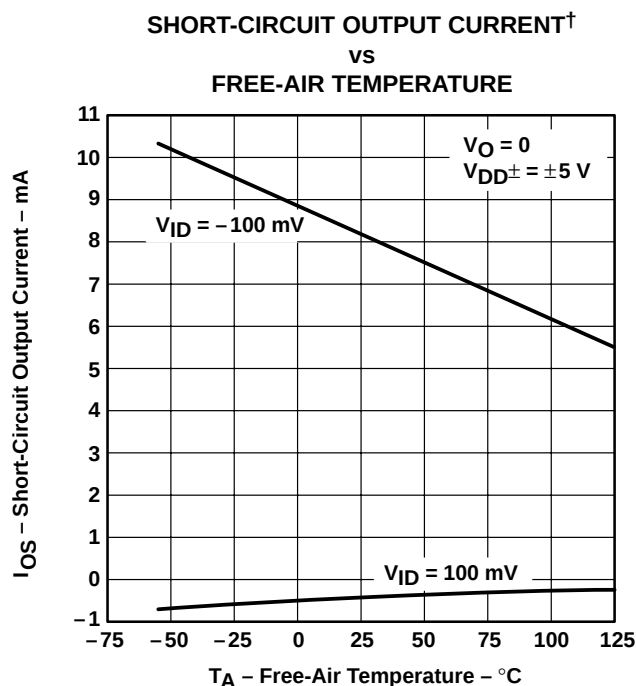


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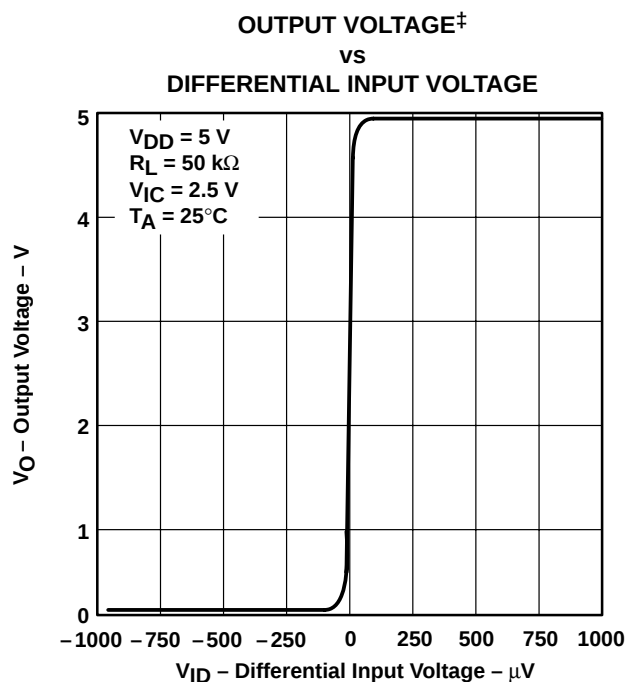


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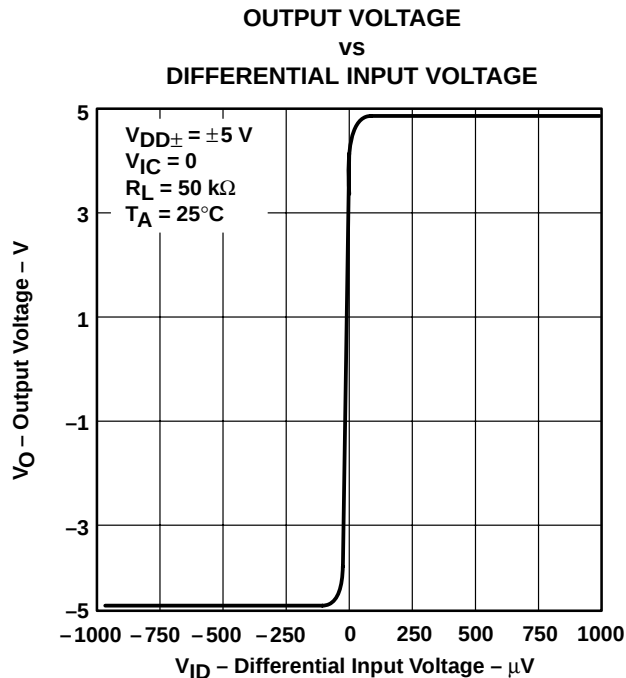


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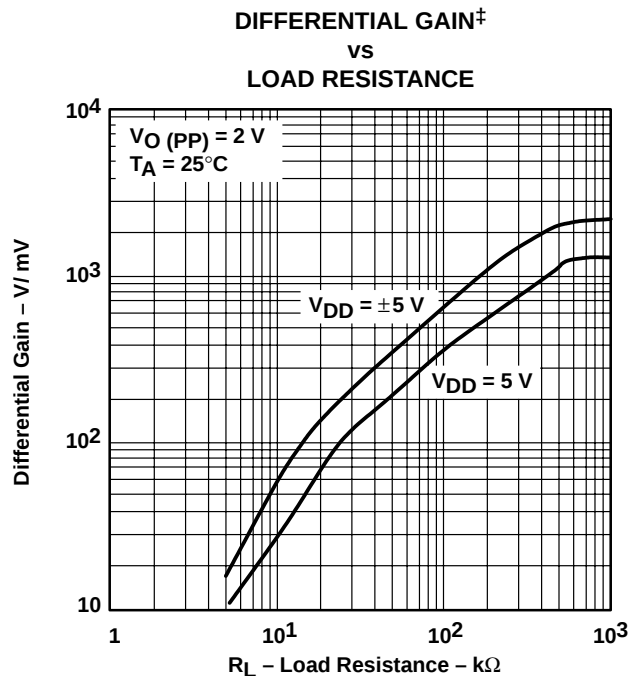


Figure 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†

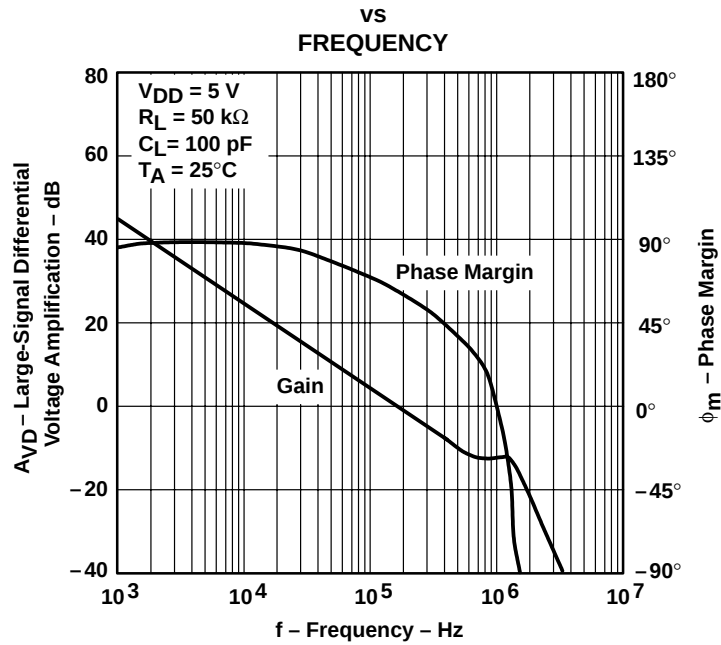


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

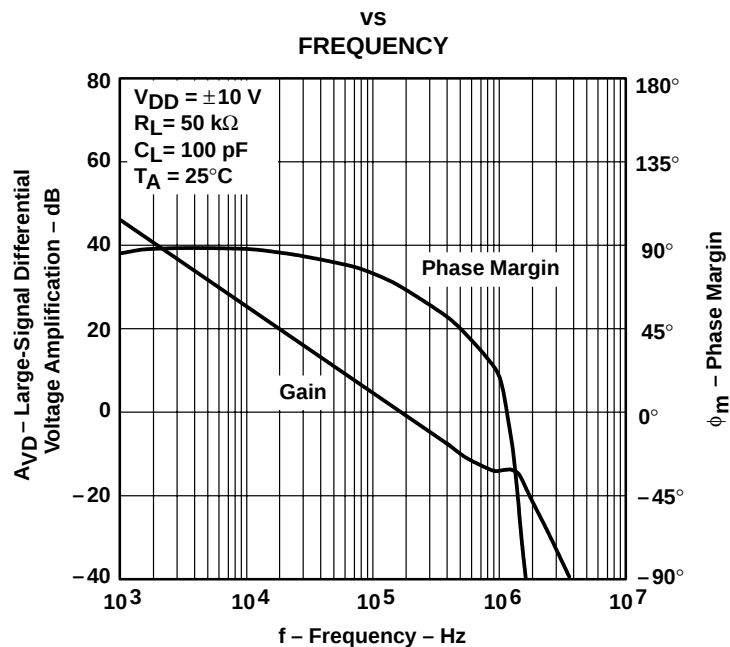


Figure 27

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TLC225x, TLC225xA Advanced LinCMOS™ RAIL-TO-RAIL VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

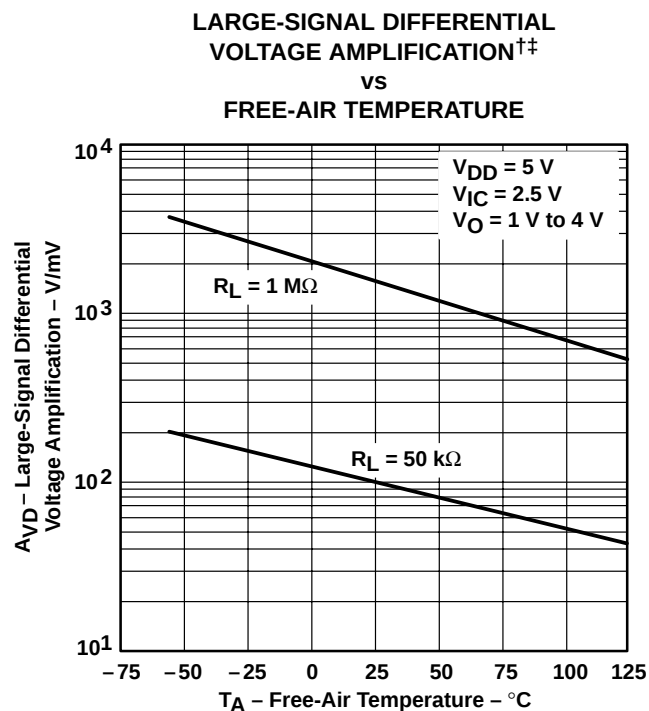


Figure 28

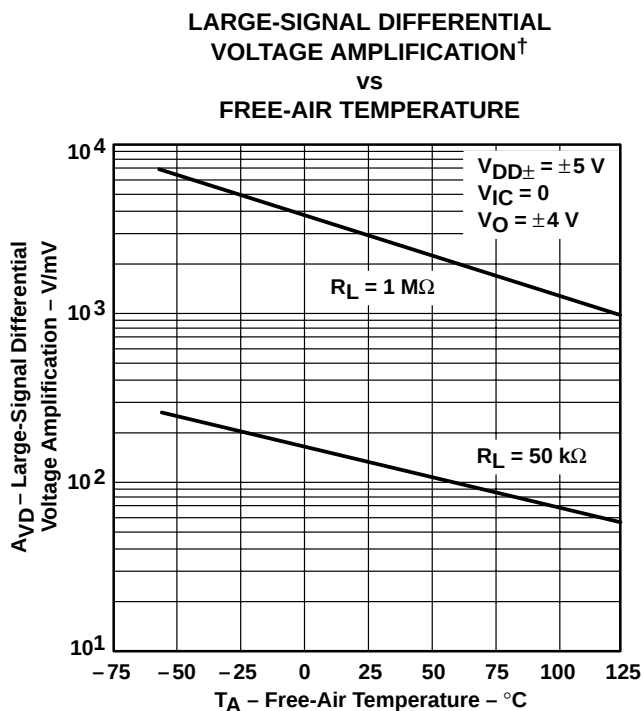


Figure 29

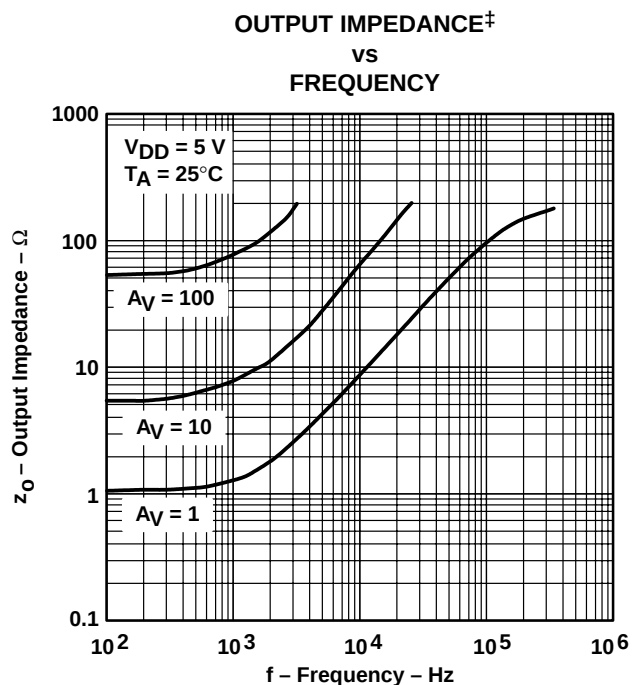


Figure 30

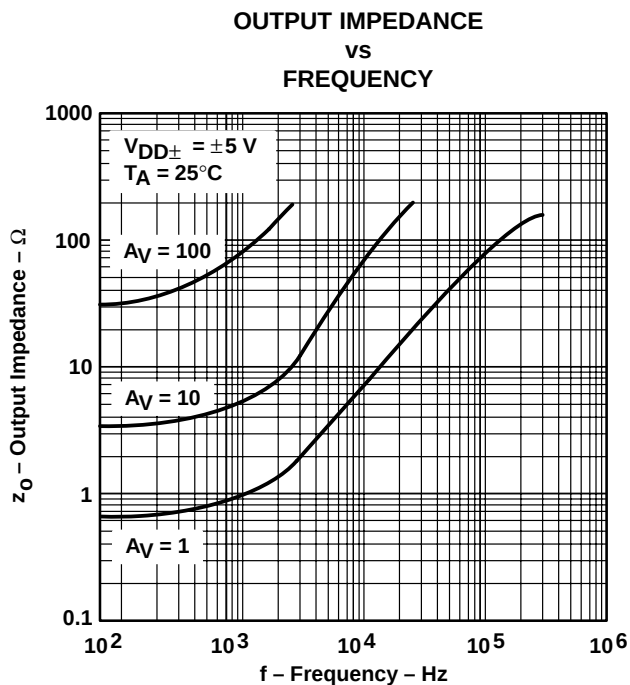


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

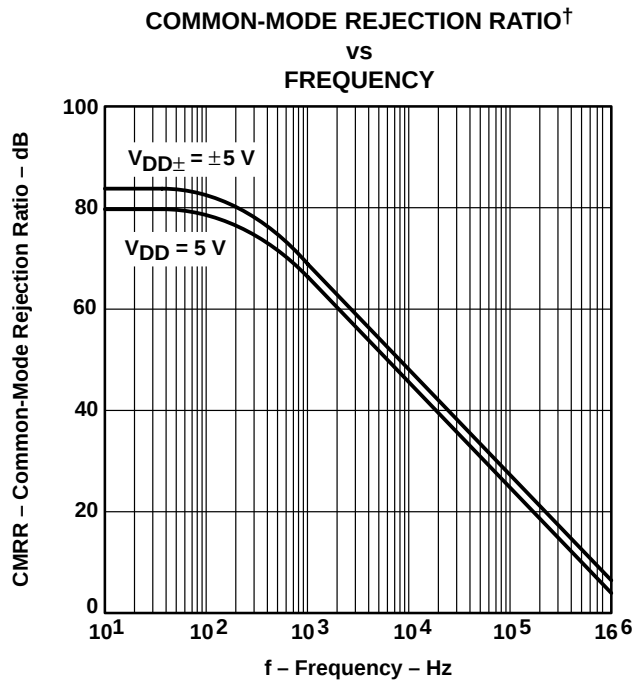


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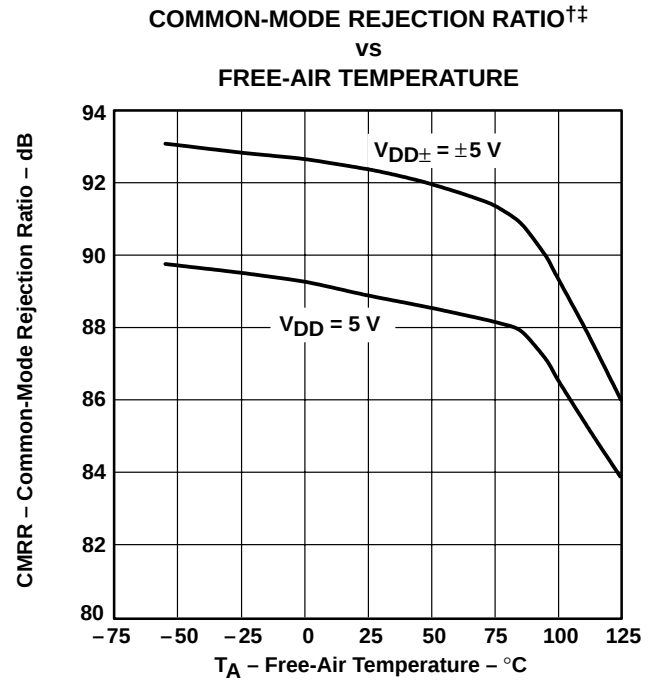


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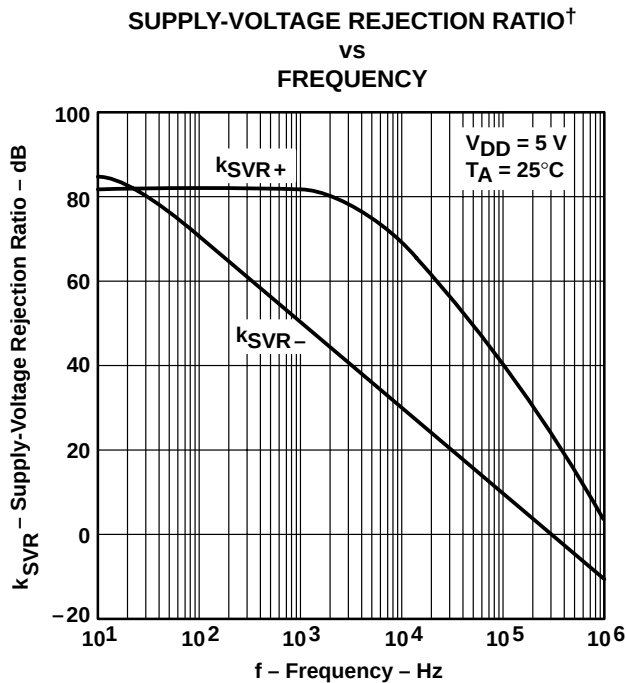


Figure 34

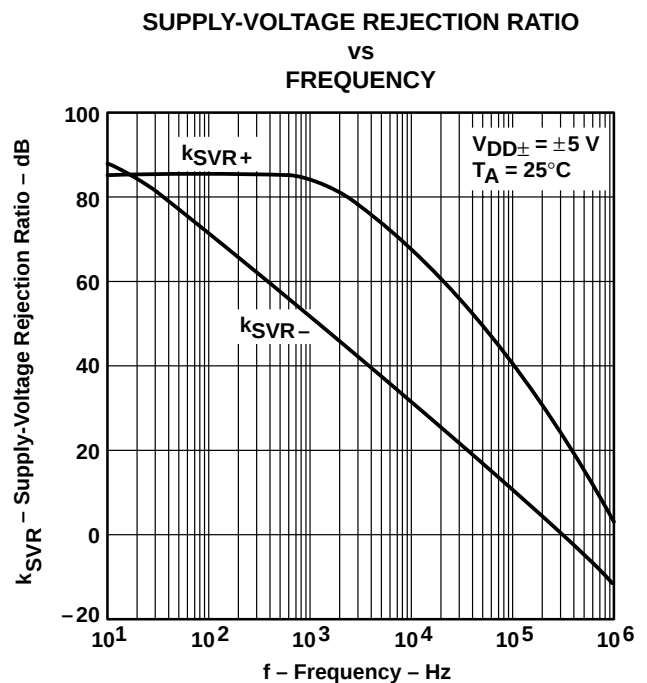


Figure 35

[†] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

[‡] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC225x, TLC225xA Advanced LinCMOS™ RAIL-TO-RAIL VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

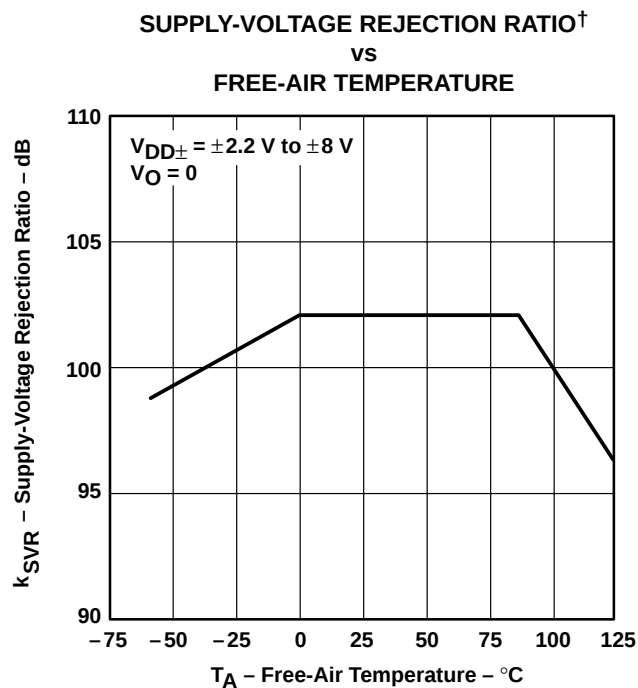


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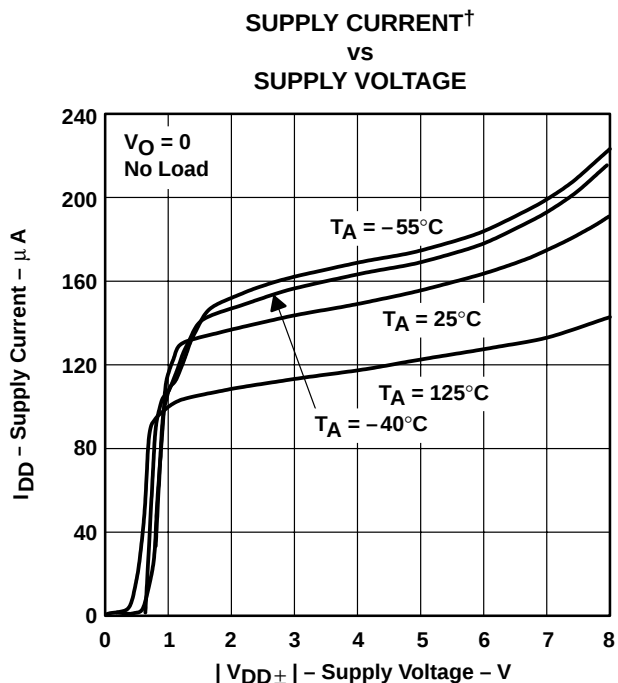


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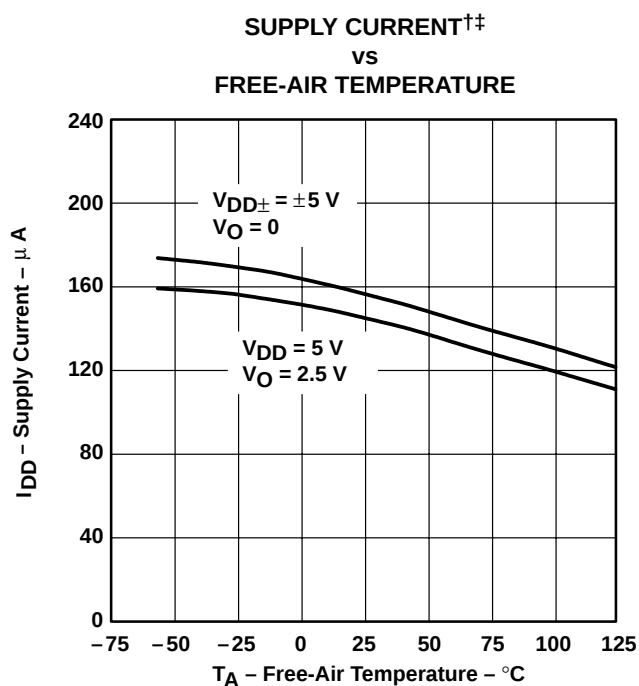


Figure 38

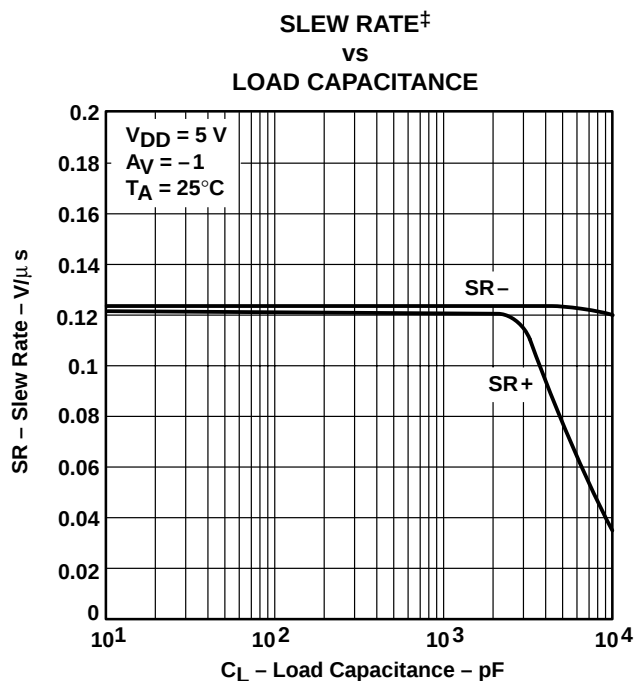
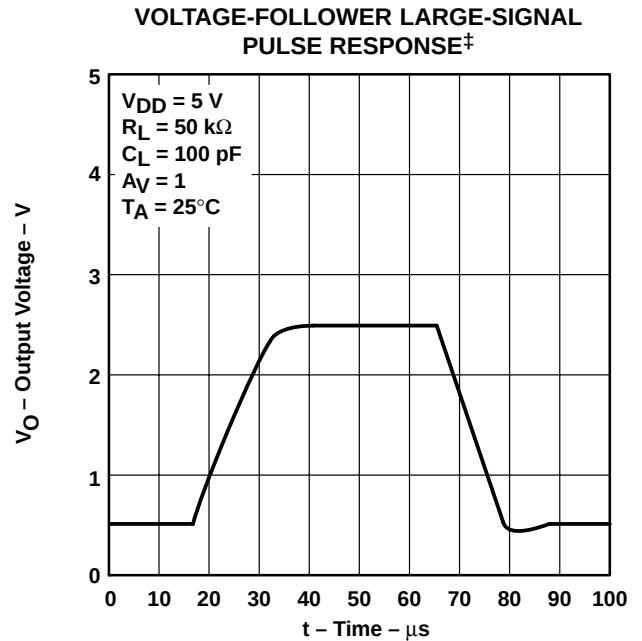
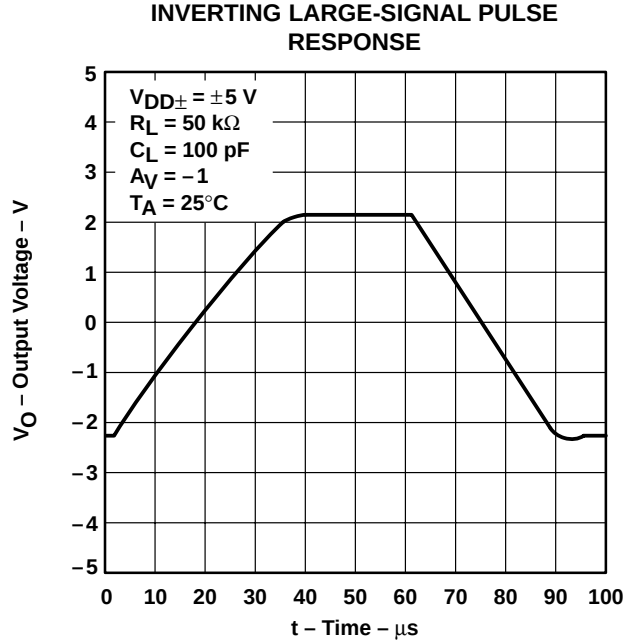
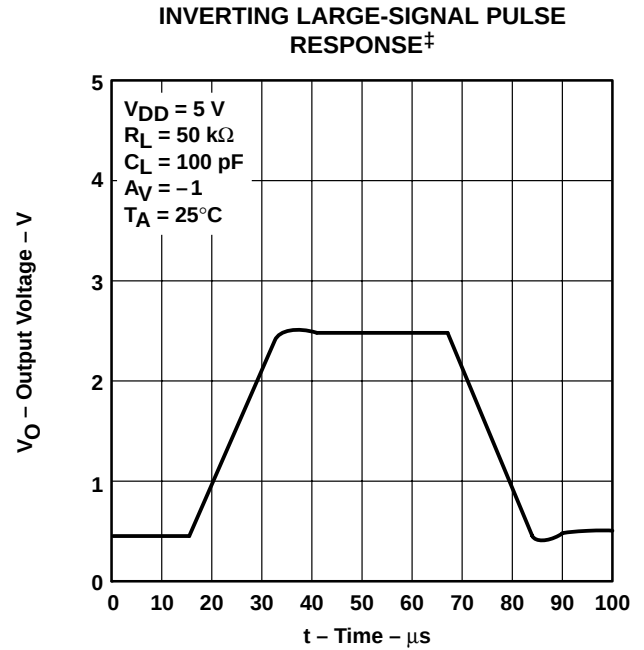
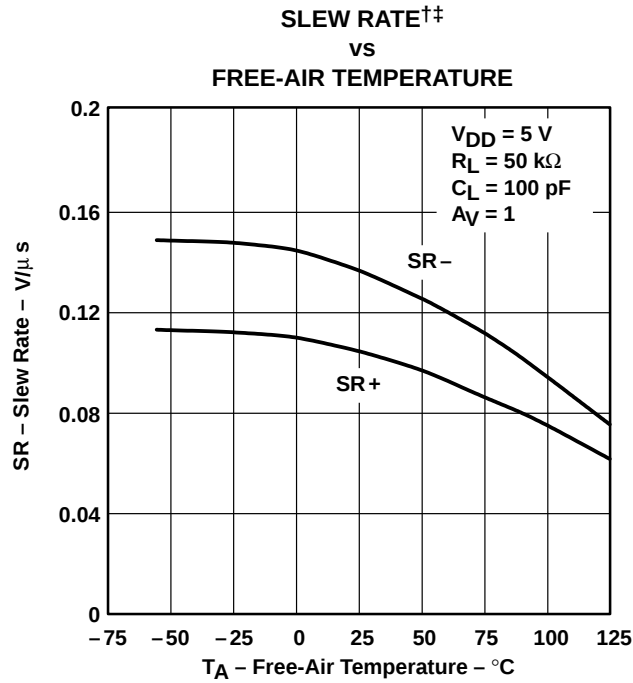


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

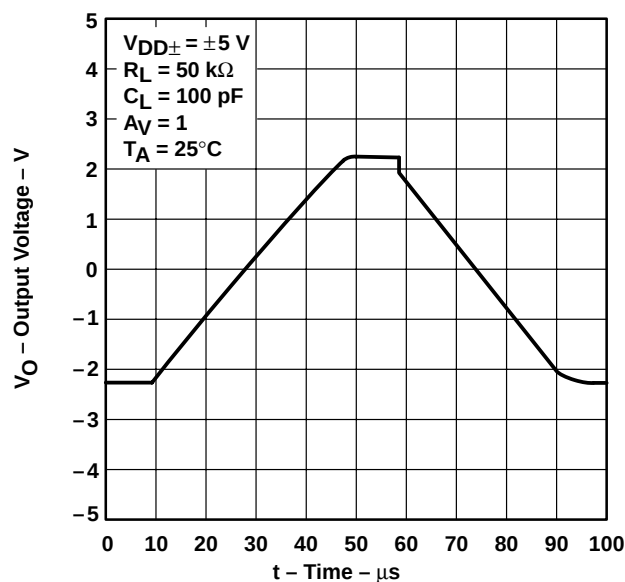


Figure 44

INVERTING SMALL-SIGNAL PULSE RESPONSE†

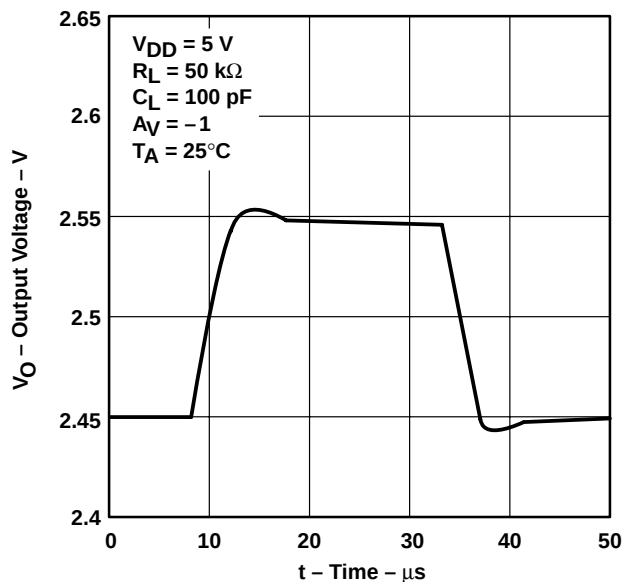


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE

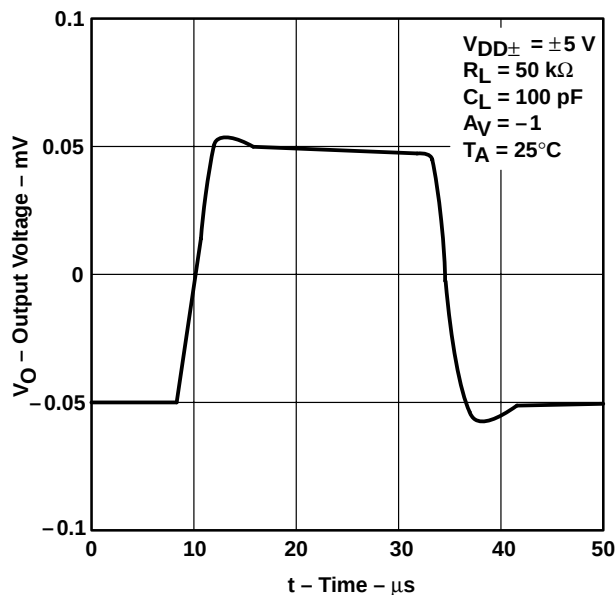


Figure 46

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

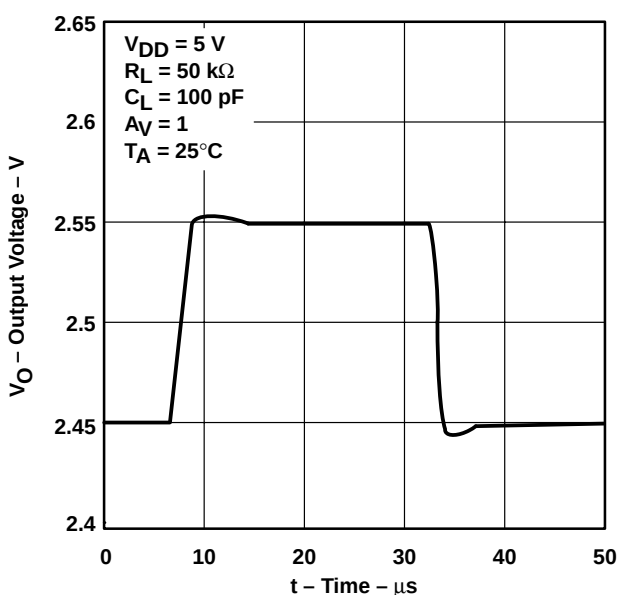


Figure 47

† For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

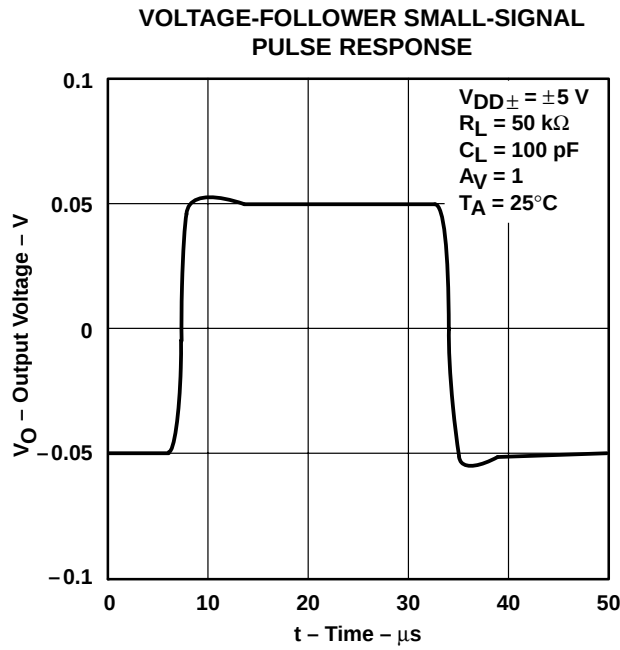


Figure 48

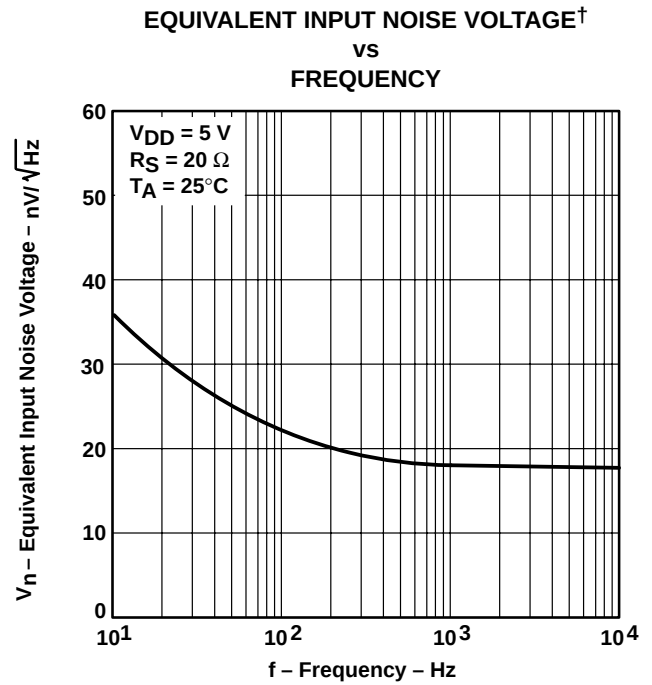


Figure 49

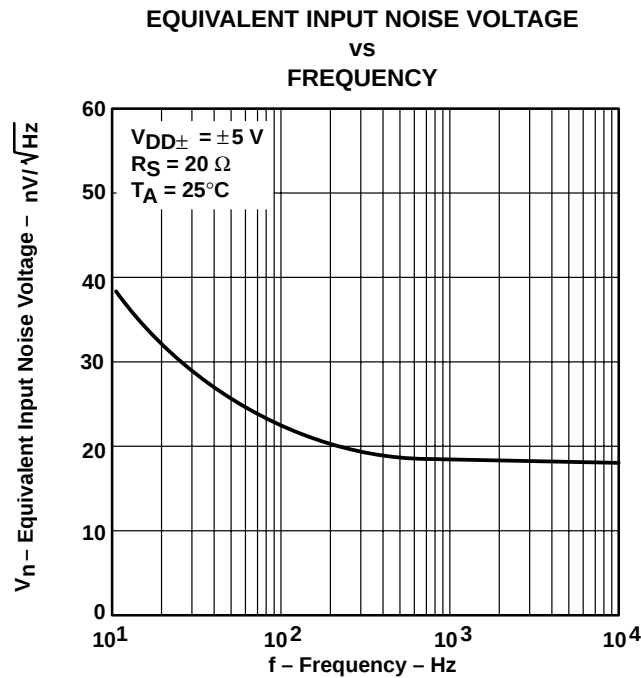


Figure 50

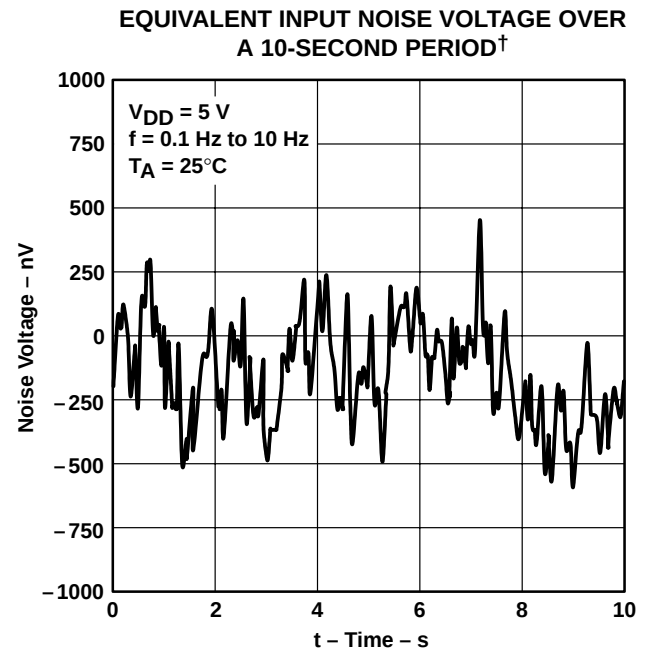


Figure 51

† For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V .

TLC225x, TLC225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

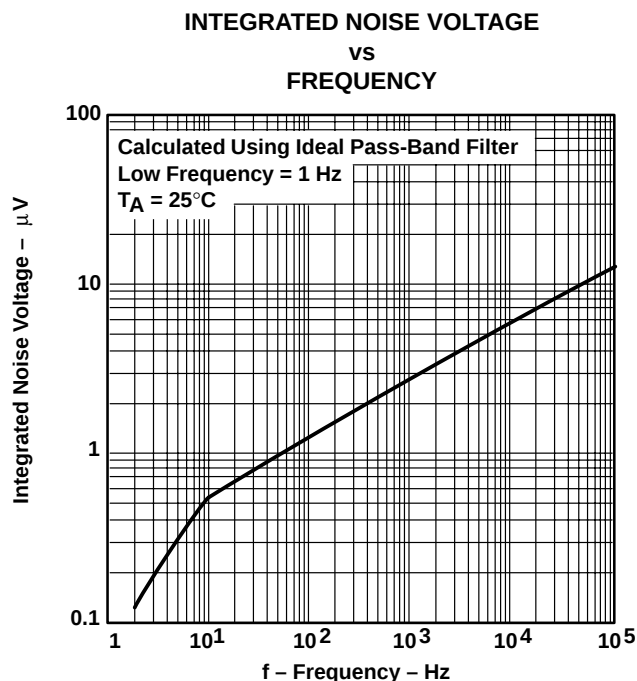


Figure 52

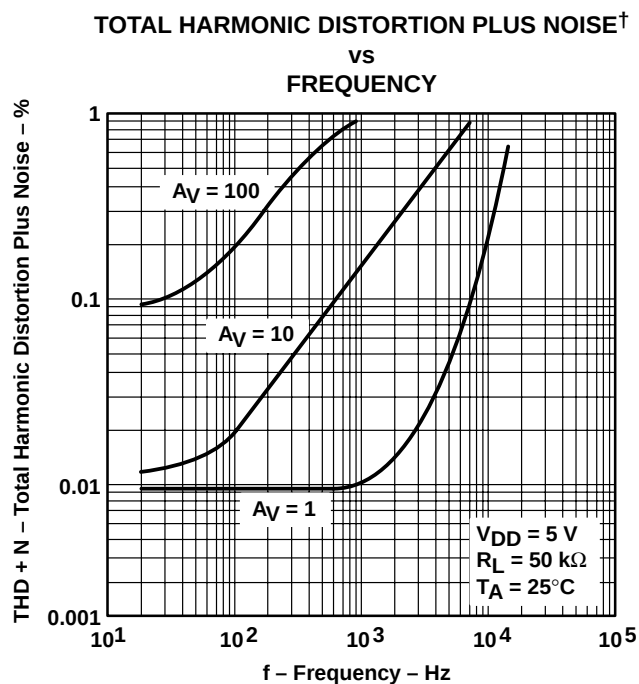


Figure 53

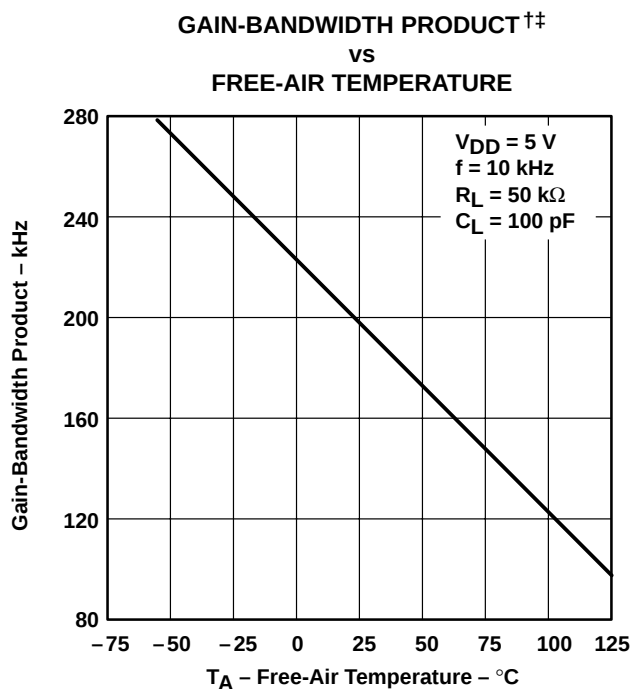


Figure 54

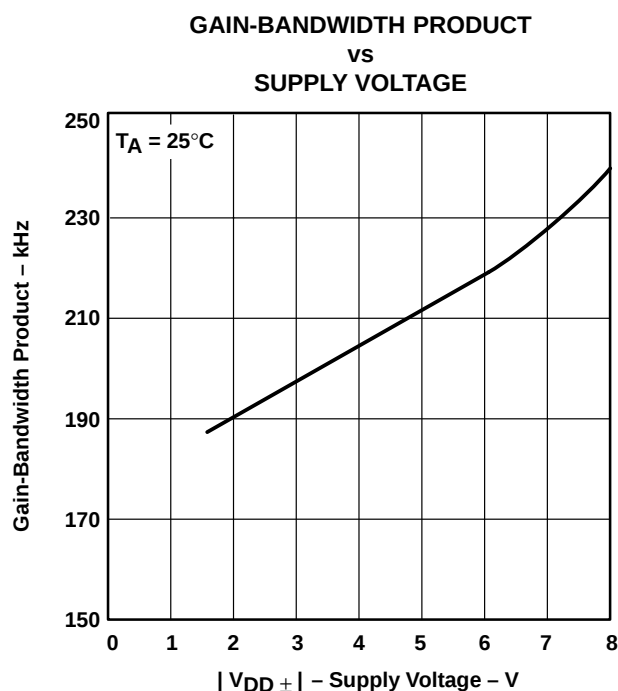
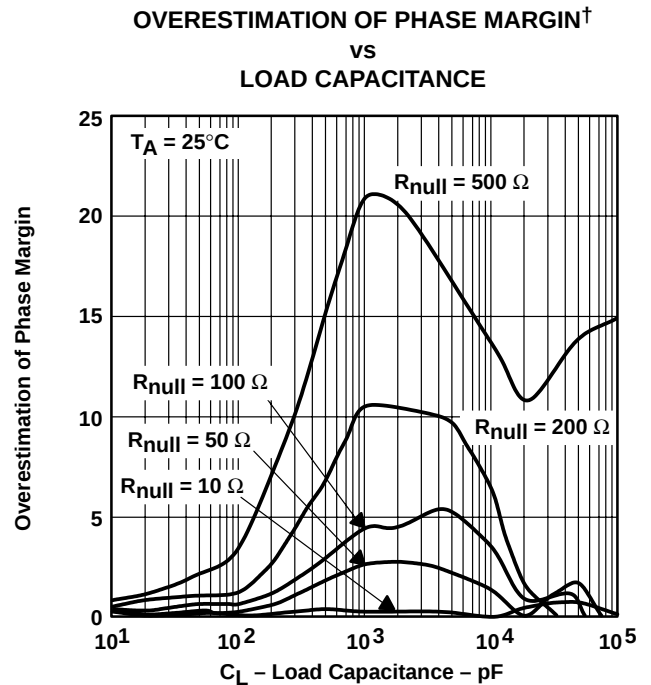
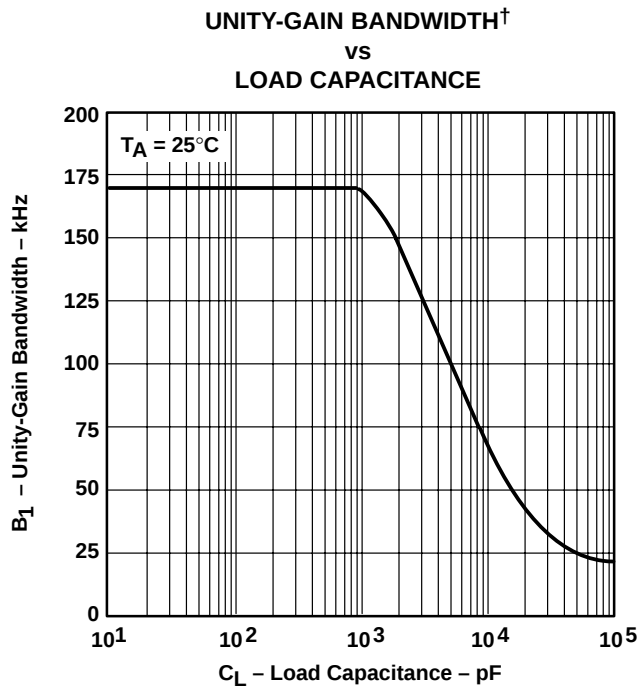
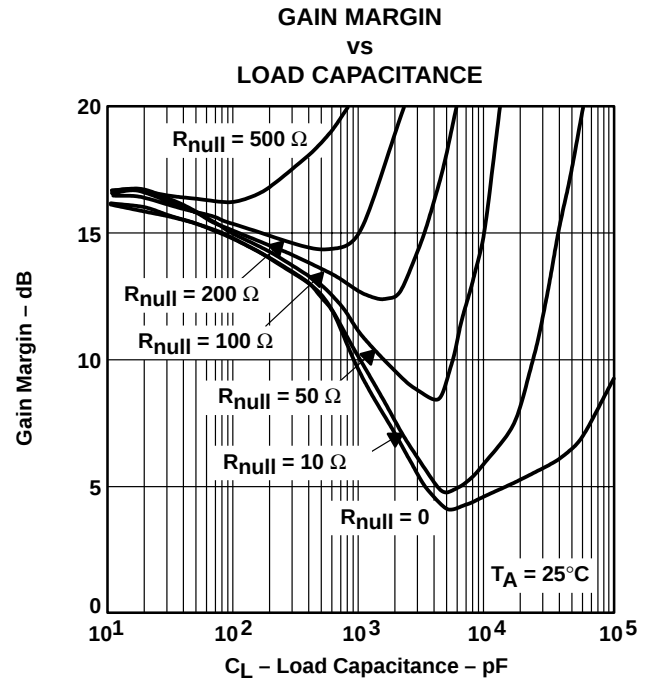
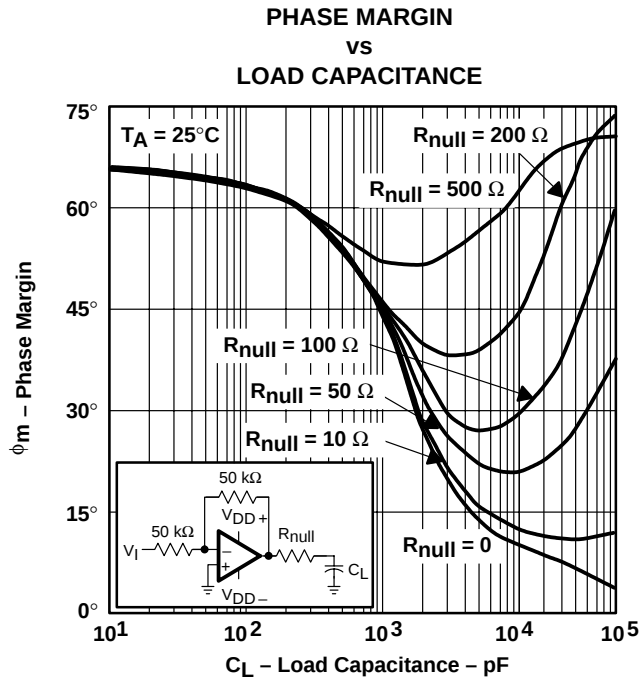


Figure 55

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC225x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 56 and Figure 57 show the effects of adding series resistances of 10 Ω , 50 Ω , 100 Ω , 200 Ω , and 500 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

- $\Delta\phi_{m1}$ = Improvement in phase margin
- UGBW = Unity-gain bandwidth frequency
- R_{null} = Output series resistance
- C_L = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

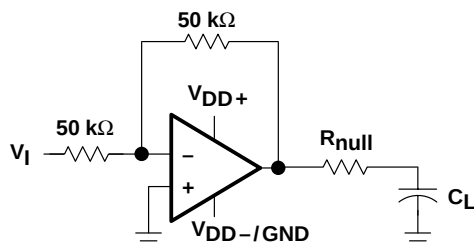


Figure 60. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using MicroSim *Parts*™, the model generation software used with MicroSim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLC225x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

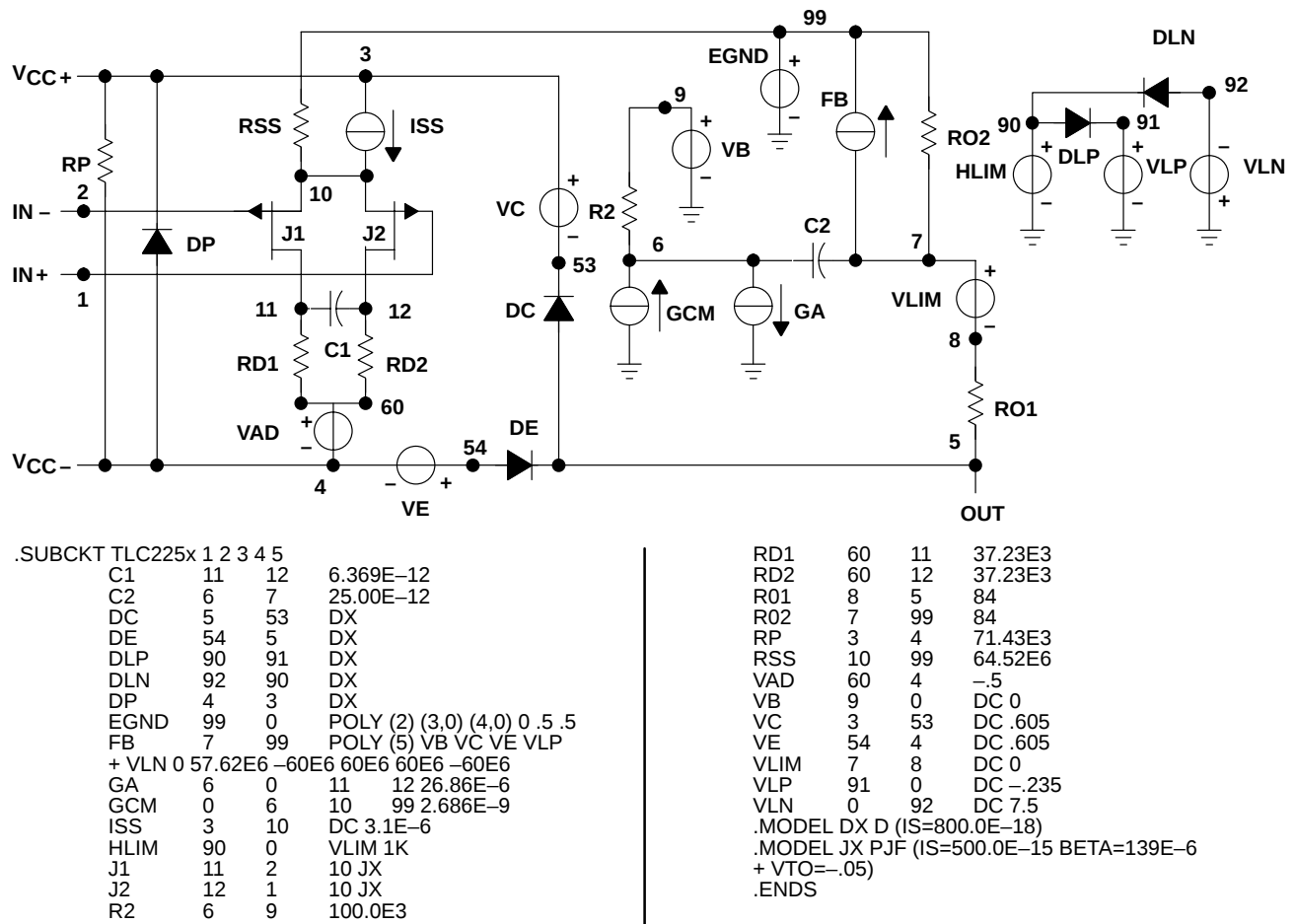


Figure 61. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9564001NXD	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
5962-9564001NXDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
5962-9564001Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9564001QHA	ACTIVE	CFP	U	10	1	TBD	Call TI	Call TI	
5962-9564001QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-9564002NYDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
5962-9564002Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9564002QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-9564002QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
5962-9564003NXD	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
5962-9564003NXDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
5962-9564003Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9564003QHA	ACTIVE	CFP	U	10	1	TBD	Call TI	Call TI	
5962-9564003QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-9564004NYDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
5962-9564004Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9564004QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-9564004QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
TLC2252AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TLC2252AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2252AIP4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2252AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AIPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC2252AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2252AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC2252AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	
TLC2252AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2252CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2252CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TLC2252CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC2252CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2252IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2252MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2252MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC2252MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	
TLC2252QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2252QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TLC2254AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2254AINE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2254AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AIPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
TLC2254AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2254AMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
TLC2254AMWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
TLC2254AQD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM	
TLC2254AQDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254AQDR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM	
TLC2254AQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
TLC2254CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
TLC2254CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
TLC2254CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
TLC2254CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2254CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2254CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TLC2254CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
TLC2254CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2254INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2254MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2254MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
TLC2254MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
TLC2254QD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM	
TLC2254QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2254QDR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM	
TLC2254QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

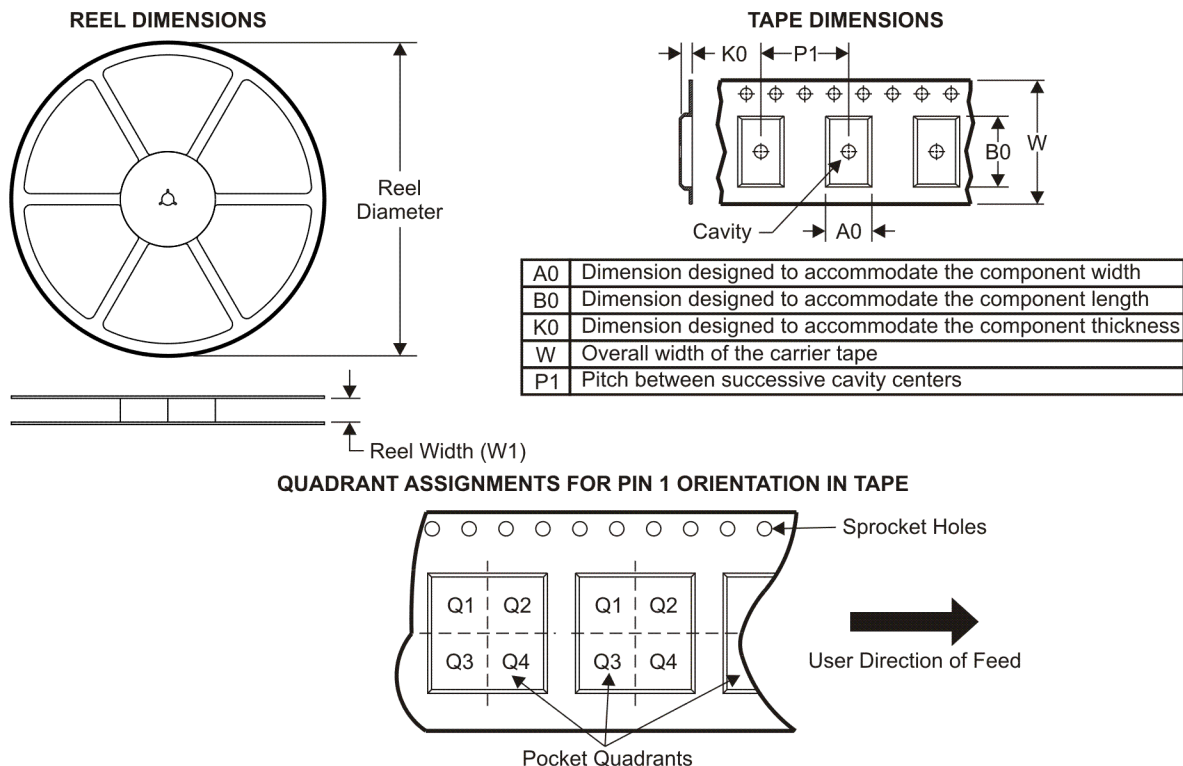
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC2252, TLC2252A, TLC2252AM, TLC2252M, TLC2254, TLC2254A, TLC2254AM, TLC2254M :

- Catalog: [TLC2252A](#), [TLC2252](#), [TLC2254A](#), [TLC2254](#)
- Automotive: [TLC2252-Q1](#), [TLC2252A-Q1](#), [TLC2252A-Q1](#), [TLC2252-Q1](#), [TLC2254-Q1](#), [TLC2254A-Q1](#), [TLC2254A-Q1](#), [TLC2254-Q1](#)
- Enhanced Product: [TLC2252-EP](#), [TLC2252A-EP](#), [TLC2252A-EP](#), [TLC2252-EP](#), [TLC2254-EP](#), [TLC2254A-EP](#), [TLC2254A-EP](#), [TLC2254-EP](#)
- Military: [TLC2252M](#), [TLC2252AM](#), [TLC2254M](#), [TLC2254AM](#)

NOTE: Qualified Version Definitions:

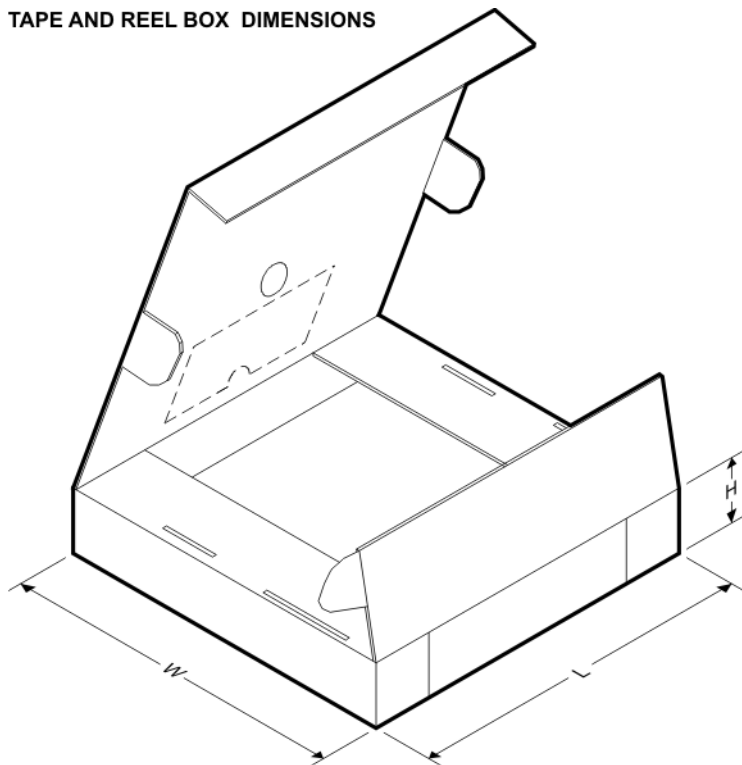
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962-9564001NXDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
5962-9564002NYDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
5962-9564003NXDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
5962-9564004NYDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2252AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2252CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2252IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2254AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2254AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2254IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

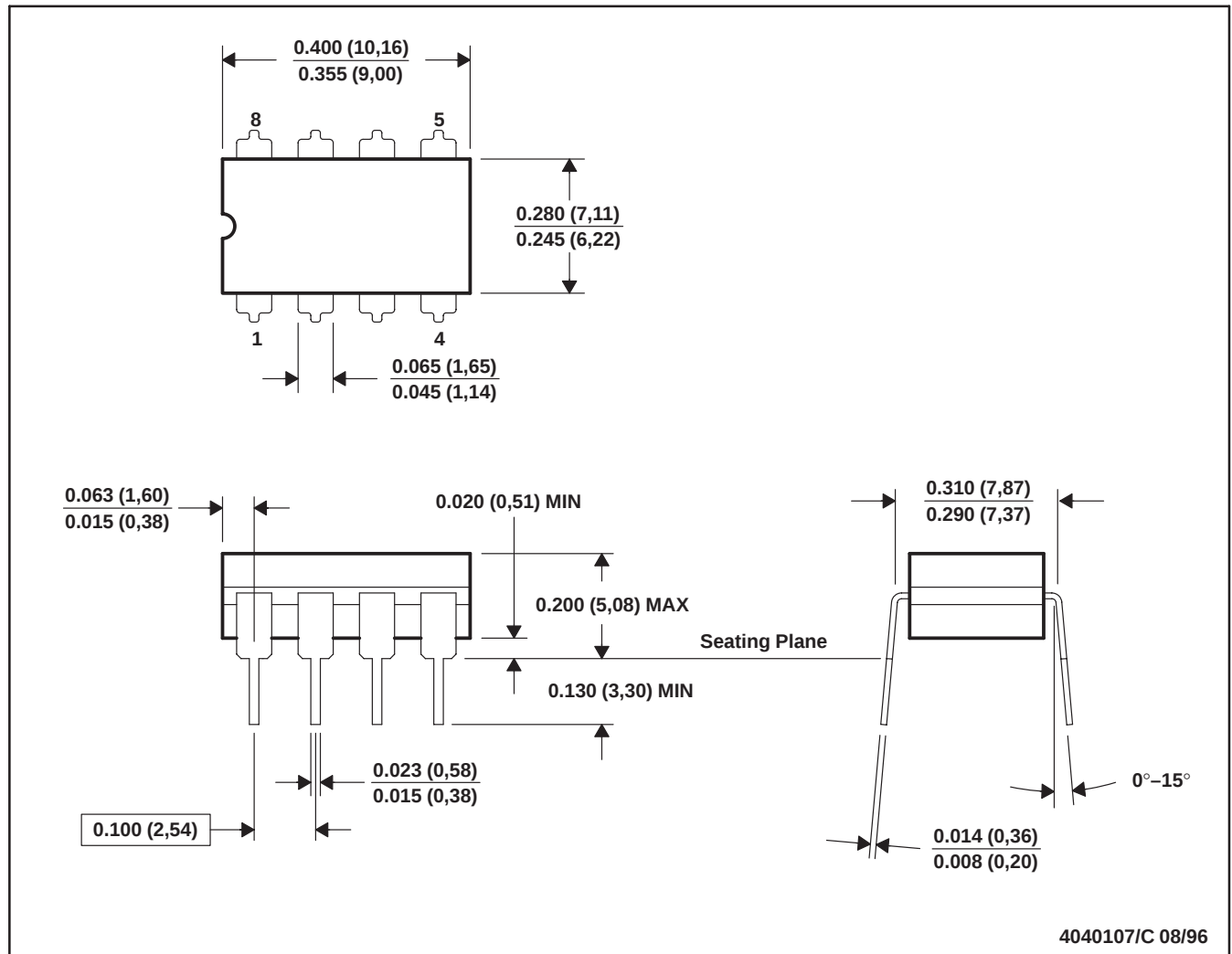


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962-9564001NXDR	SOIC	D	8	2500	346.0	346.0	29.0
5962-9564002NYDR	SOIC	D	14	2500	346.0	346.0	33.0
5962-9564003NXDR	SOIC	D	8	2500	346.0	346.0	29.0
5962-9564004NYDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2252AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2252AIPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TLC2252CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2252CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TLC2252IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2254AIDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2254AIPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLC2254AQDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2254CDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2254CPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLC2254IDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2254QDR	SOIC	D	14	2500	346.0	346.0	33.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

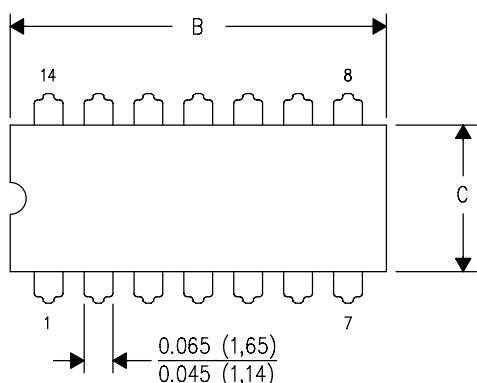


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

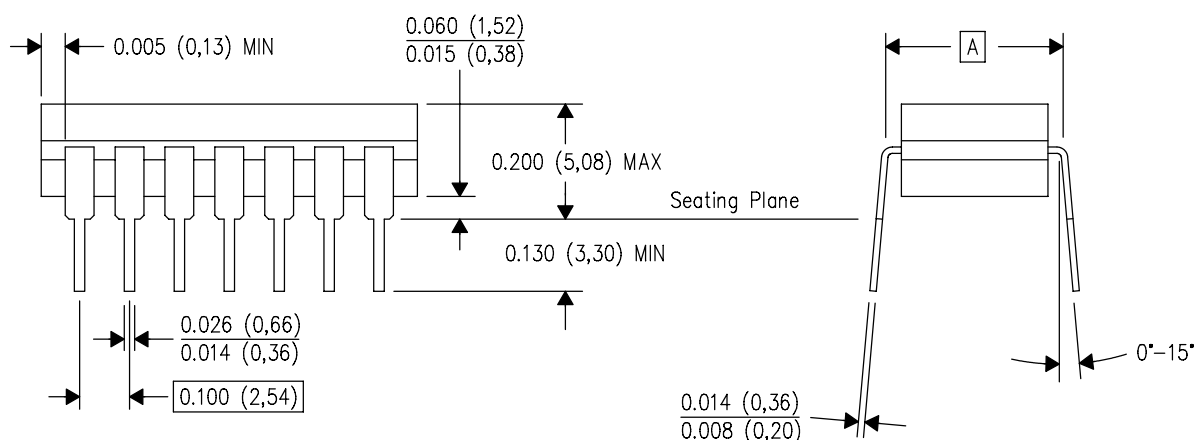
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

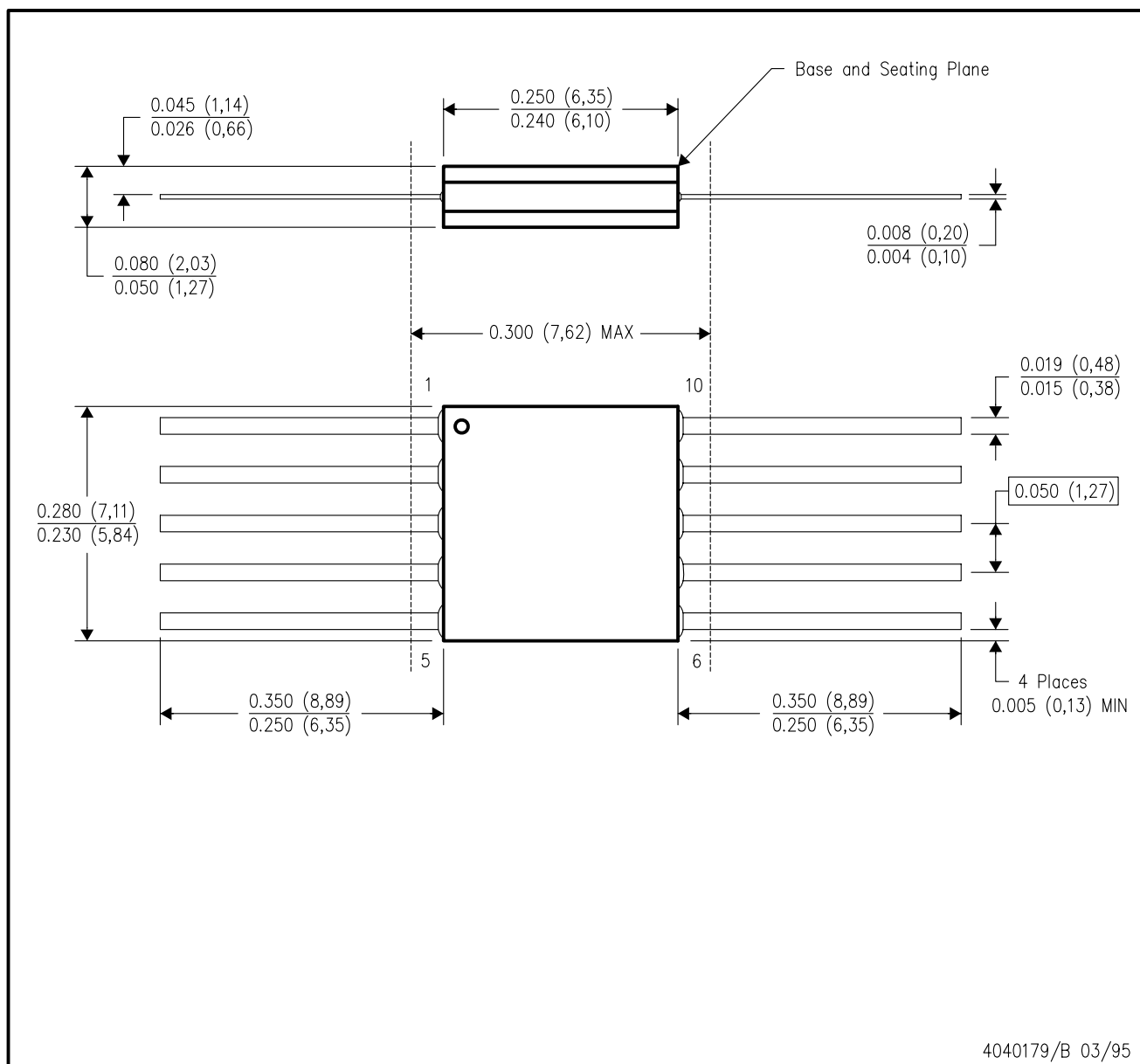


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

U (S-GDFP-F10)

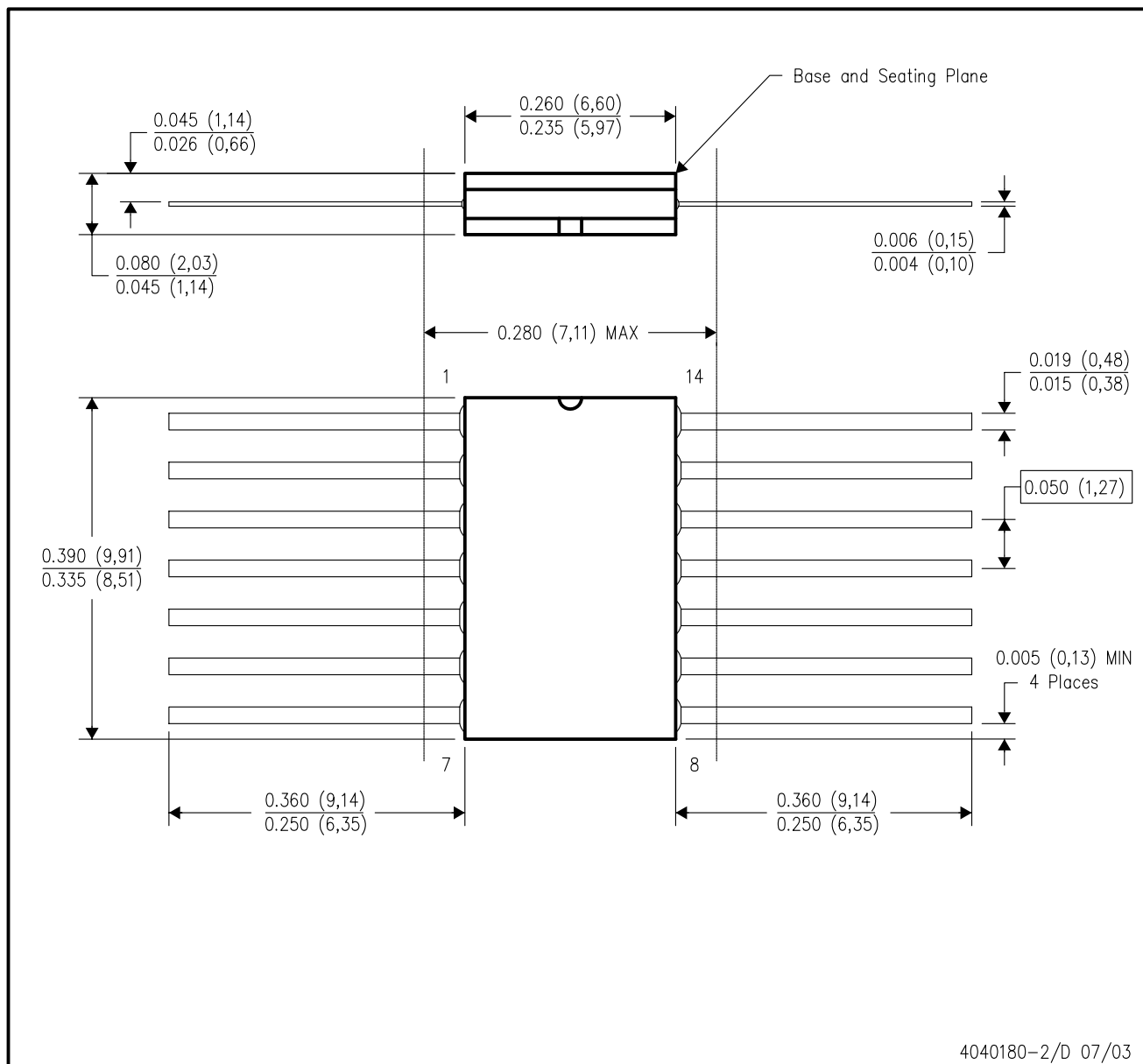
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

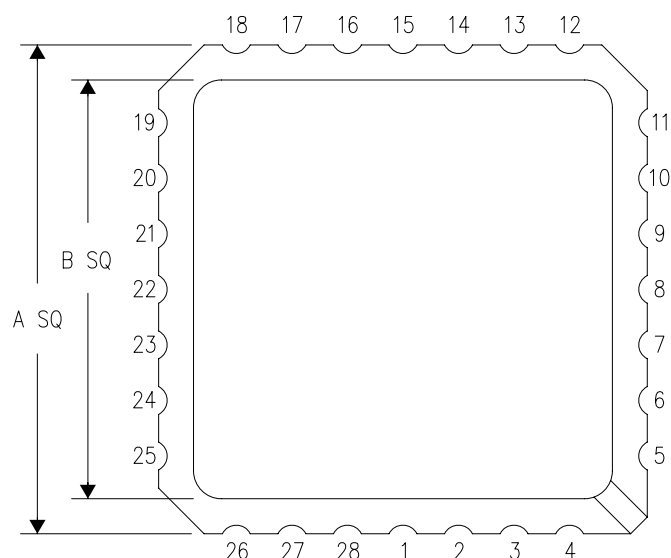


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

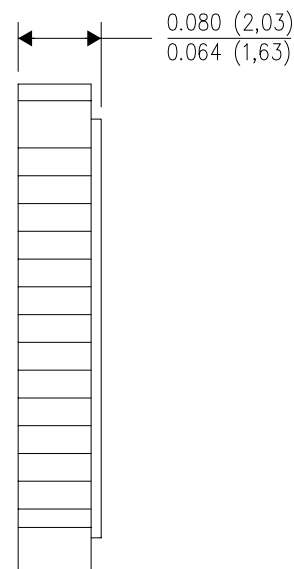
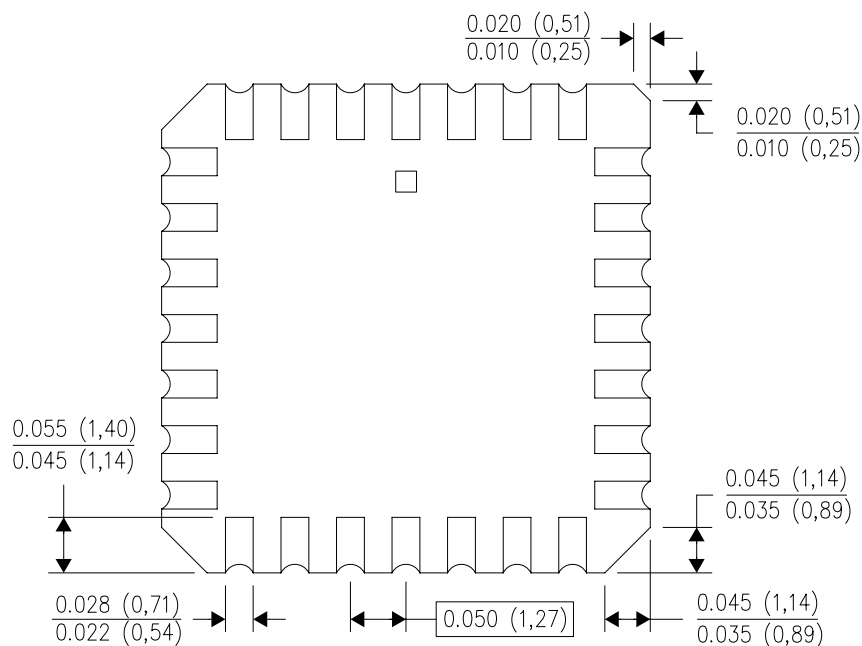
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

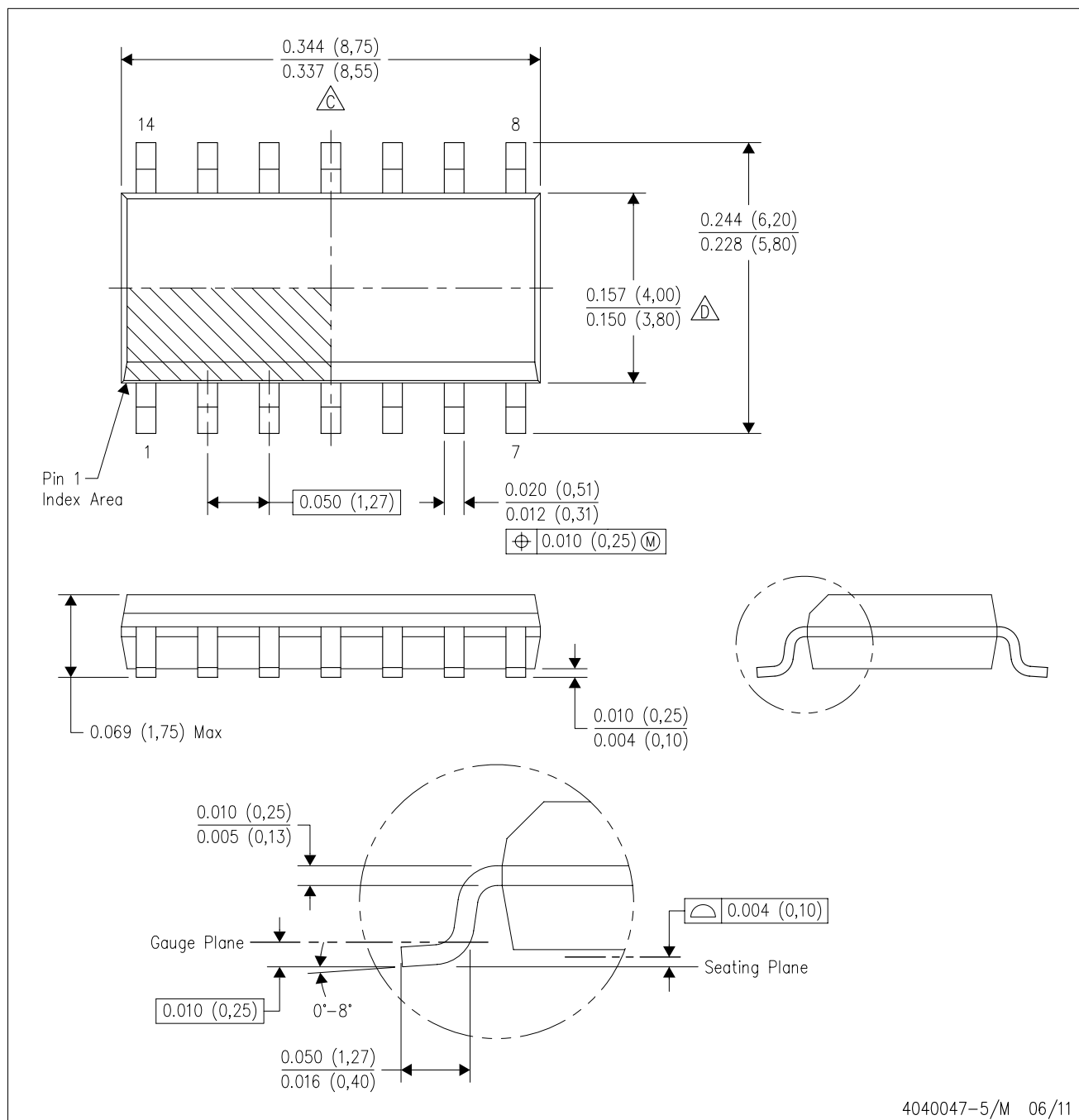
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



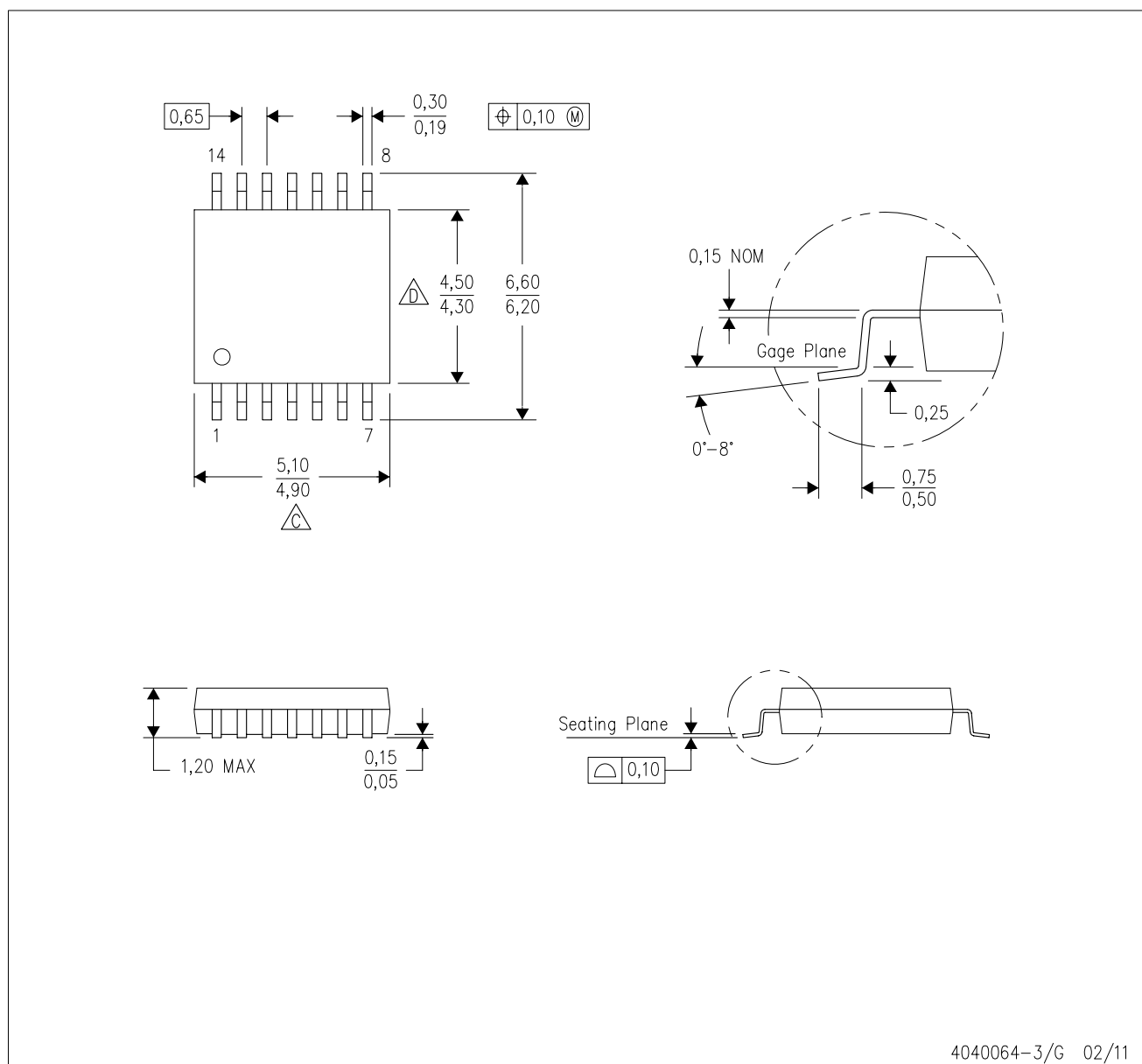
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

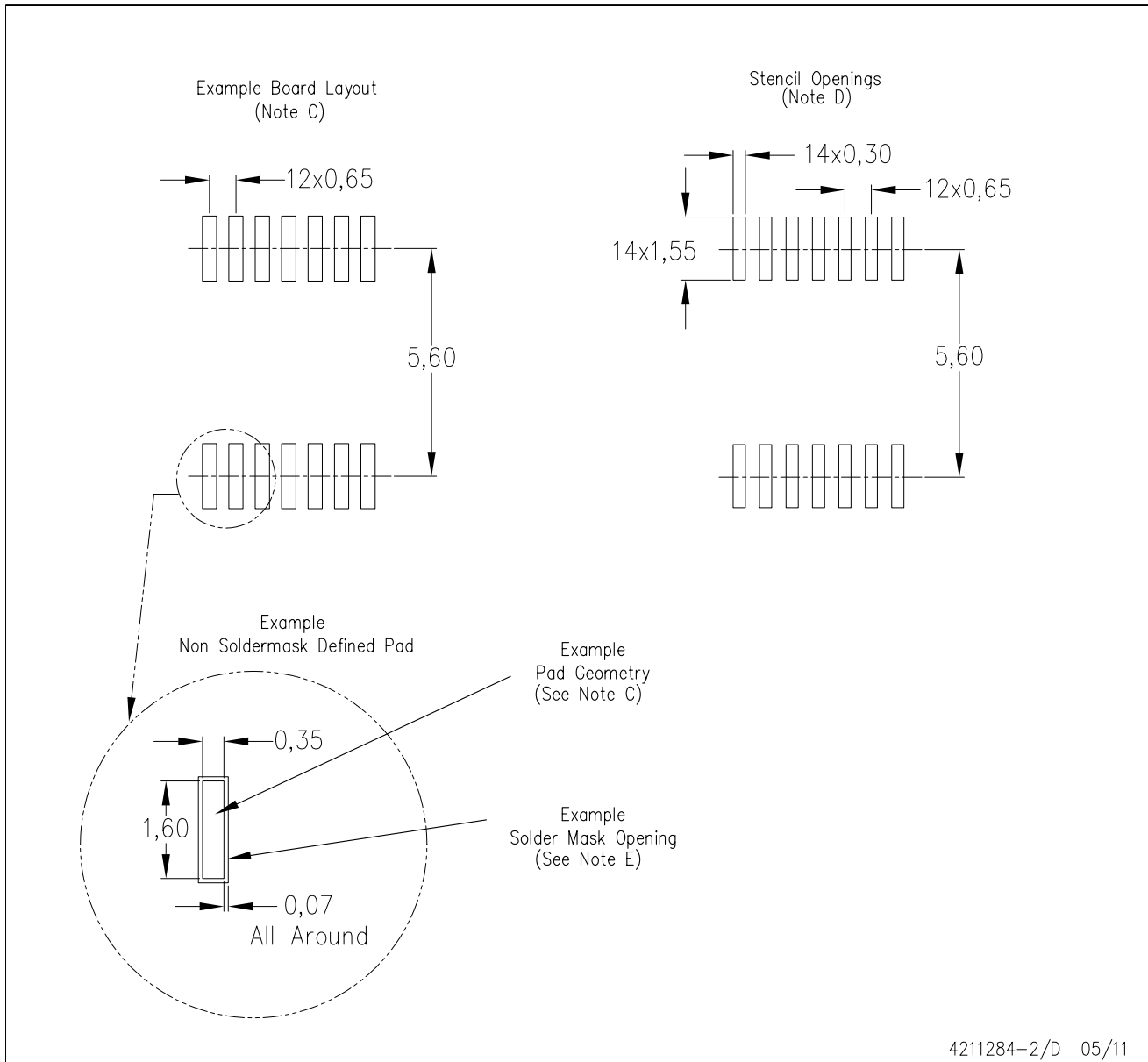
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

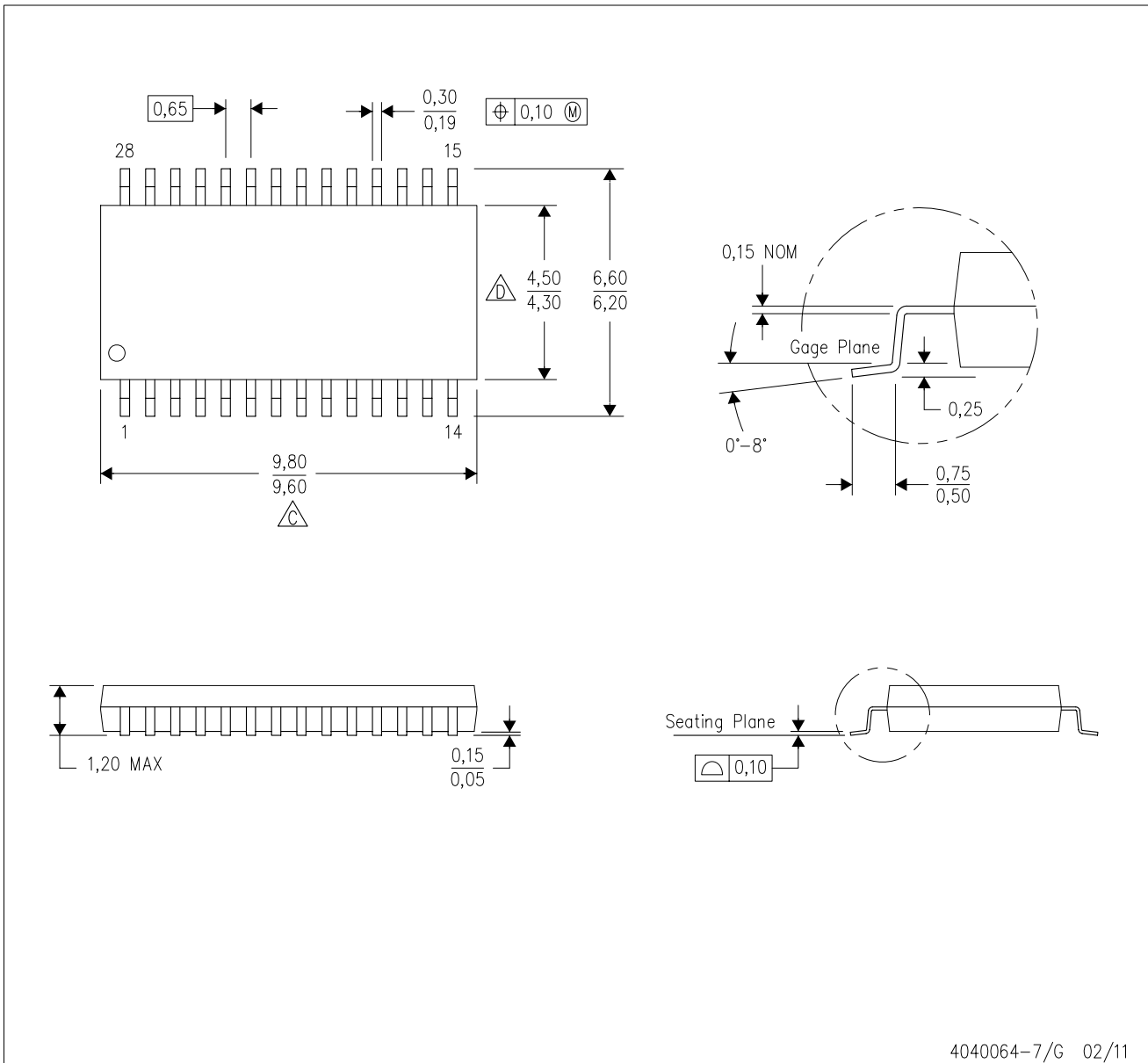
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28)

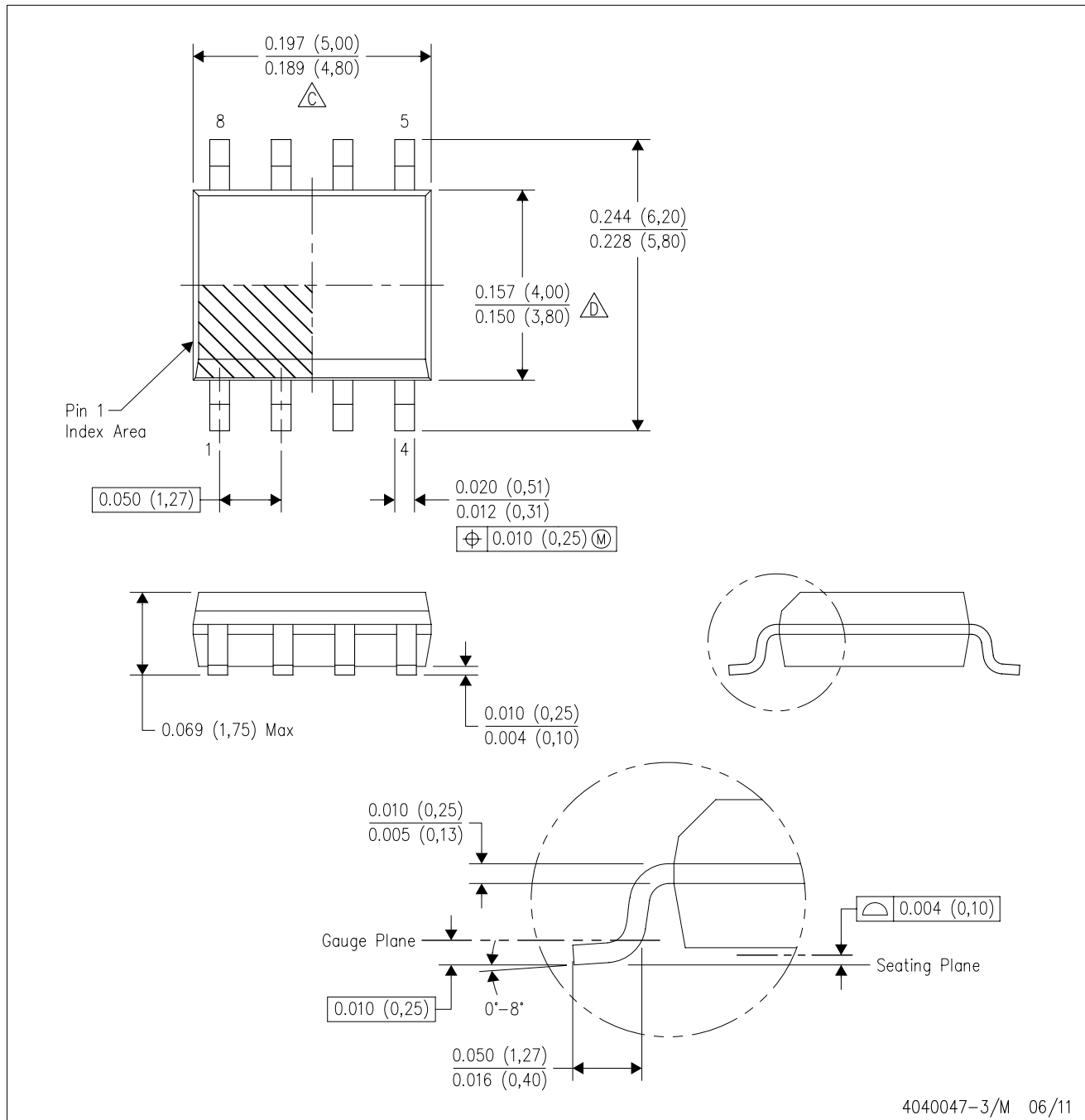
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

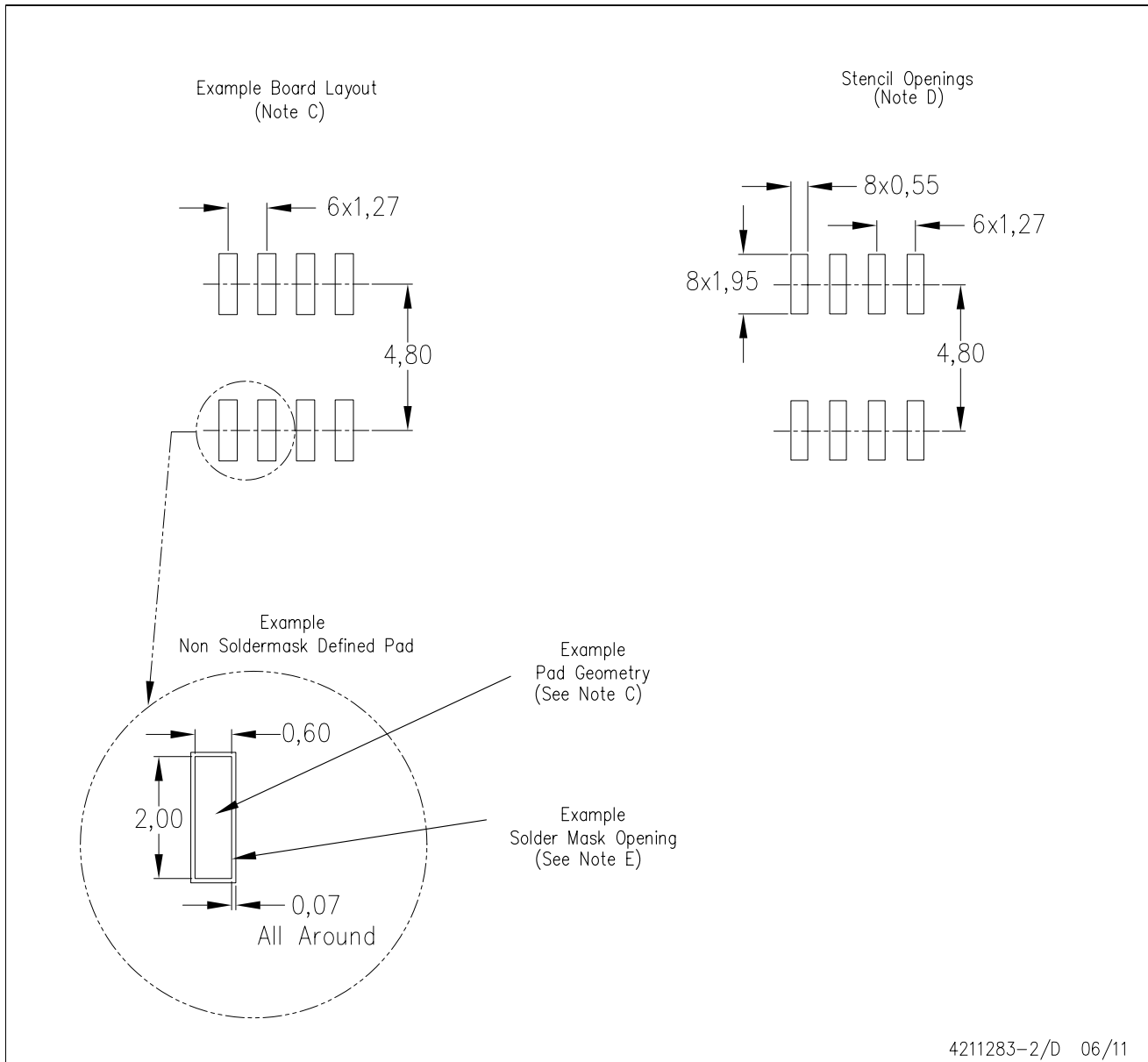
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

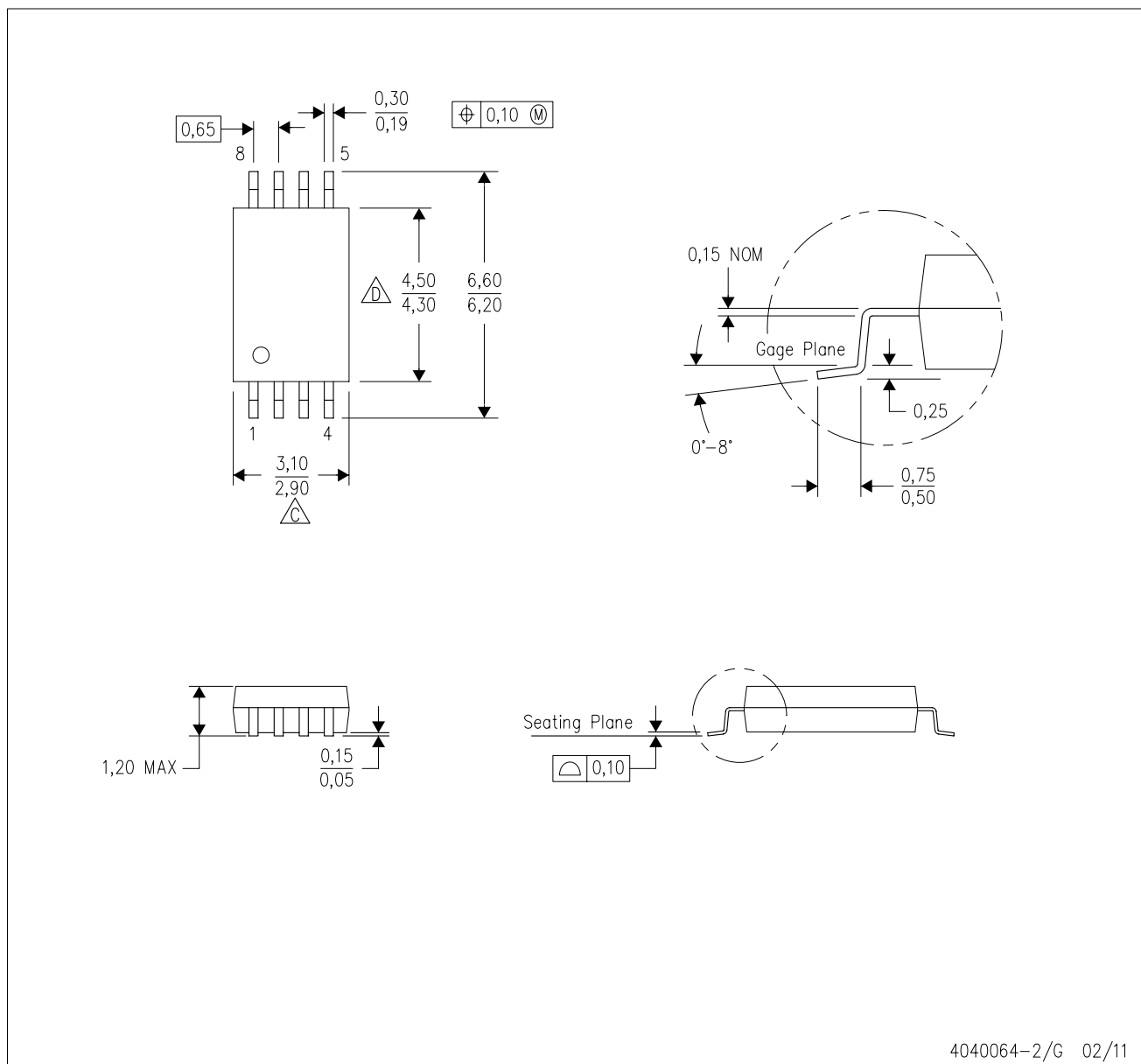


4211283-2/D 06/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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