

REVISIONS																				
LTR	DESCRIPTION									DATE (YR-MO-DA)				APPROVED						
A	Add vendor CAGE F8859. Add device class V criteria. Editorial changes throughout. – gap									00-01-05				Raymond Monnin						
B	Add case outline X. Add delta limits, table III. Update boilerplate. – cfs									00-09-18				Monica L. Poelking						
C	Add case outline Z. Update boilerplate to MIL-PRF-38535 requirements. – jak									01-08-07				Thomas M. Hess						
D	Add radiation features, section 1.5. Add radiation criteria in table I. Change case outline X lead temperature in section 1.3. Correct the waveforms in figure 5. Update boilerplate to include radiation hardness assured requirements. - jak									05-05-27				Thomas M. Hess						
E	Add die for device type 01 and die appendix A. Update radiation features in section 1.5 and SEP test limits table IB. Update boilerplate paragraphs to current MIL-PRF-38535 requirements. – MAA									10-11-24				Thomas M. Hess						
F	Update dimensions of case outline X to figure 1. - LTG									12-07-25				Thomas M. Hess						

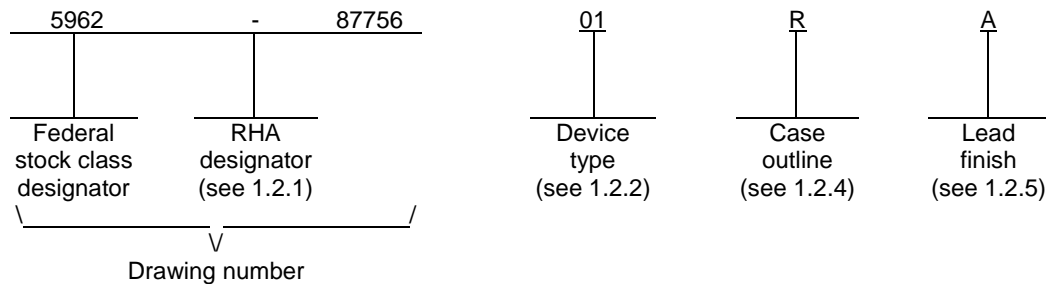
REV																				
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REV	F	F	F	F	F	F	F	F	F											
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS				REV			F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A				PREPARED BY Marcia B. Kelleher						DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil										
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY William J. Johnson																
				APPROVED BY Michael A. Frye						MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL D-TYPE FLIP-FLOP WITH MASTER RESET, MONOLITHIC SILICON										
				DRAWING APPROVAL DATE 88-12-06																
				REVISION LEVEL F						SIZE A	CAGE CODE 67268	5962-87756								
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1. SCOPE

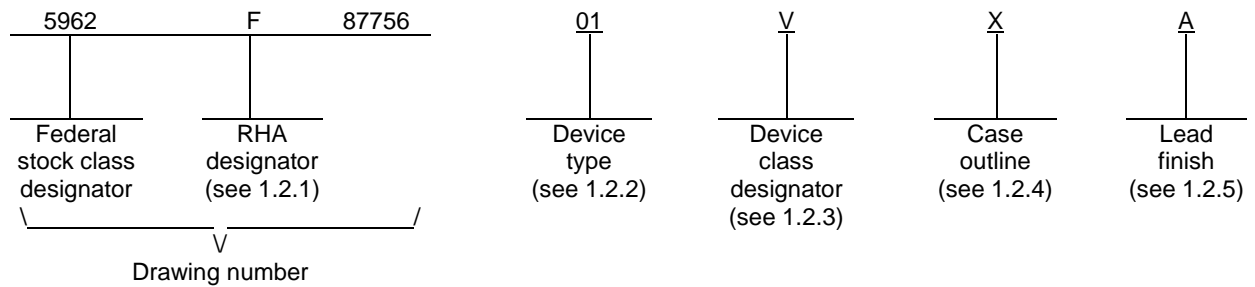
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC273	Octal D-type flip-flop with master reset

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
X	See figure 1	20	Flat pack
Z	GDFP1-G20	20	Flat pack with gull-wing
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/, 2/, 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC input clamp current (I_{IK} , I_{OK})	± 20 mA
DC output current (per pin) (I_{OUT})	± 50 mA
DC V_{CC} or GND current (per output pin) (I_{CC} , I_{GND})	± 50 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds):	
Case outline X	+260°C
All other case outlines except case X	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions. 2/, 3/, 5/

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise or fall time rate ($\Delta t/\Delta V$):	
$V_{CC} = 3.6$ V to 5.5 V	0 to 8 ns/V
Minimum setup time, Dn to CP (t_s):	
$T_C = +25^\circ\text{C}$, $V_{CC} = 3.0$ V	6.5 ns
$T_C = +25^\circ\text{C}$, $V_{CC} = 4.5$ V	4.0 ns
$T_C = -55^\circ\text{C}$ to +125°C, $V_{CC} = 3.0$ V	8.0 ns
$T_C = -55^\circ\text{C}$ to +125°C, $V_{CC} = 4.5$ V	5.0 ns
Minimum hold time, Dn to CP (t_h):	
$T_C = +25^\circ\text{C}$, $V_{CC} = 3.0$ V	1.0 ns
$T_C = +25^\circ\text{C}$, $V_{CC} = 4.5$ V	1.0 ns
$T_C = -55^\circ\text{C}$ to +125°C, $V_{CC} = 3.0$ V	1.0 ns
$T_C = -55^\circ\text{C}$ to +125°C, $V_{CC} = 4.5$ V	1.0 ns

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1.4 Recommended operating conditions - Continued. 2/, 3/, 5/

Minimum pulse width, CP (t_w):

$T_C = +25^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	5.5 ns
$T_C = +25^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	5.0 ns
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	6.5 ns
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	5.0 ns

Maximum frequency (f_{\max}):

$T_C = +25^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	90 MHz
$T_C = +25^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	95 MHz
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	75 MHz
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	90 MHz

Minimum pulse width, MR (t_w):

$T_C = +25^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	8.0 ns
$T_C = +25^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	5.0 ns
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	10.0 ns
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	6.5 ns

Minimum recovery time, MR to CP (t_{rec}):

$T_C = +25^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	5.0 ns
$T_C = +25^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	3.5 ns
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$	6.0 ns
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$	4.0 ns

1.5 Radiation features.

Device type 01:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	300 krad (Si) <u>6/</u>
Single Event Latch-up (SEL) at LET (see 4.4.4.2)	$\geq 93\text{ MeV-cm}^2/\text{mg}$ <u>6/</u>

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to $+125^\circ\text{C}$.
- 4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
- 5/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back-up systems. Data retention implies no input transition and no stored data loss with the following conditions: $V_{IH} \geq 70\%$ of V_{CC} , $V_{IL} \leq 30\%$ of V_{CC} , $V_{OH} \geq 70\%$ of V_{CC} @ $-20\mu\text{A}$, $V_{OL} \leq 30\%$ of V_{CC} @ $20\mu\text{A}$.
- 6/ These limits were obtained during technology characterization and qualification, and are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201).

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at <http://www.astm.org/> or from ASTM International, P. O. Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with figure 1 and 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

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TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +3.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class <u>4/</u>	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Positive input clamp voltage 3022	V _{IC+}	For input under test, I _{IN} = 1.0 mA	All V	0.0 V	1	0.4	1.5	V
Negative input clamp voltage 3022	V _{IC-}	For input under test, I _{IN} = -1.0 mA	All V	Open	1	-0.4	-1.5	V
High level output voltage 3006	V _{OH} <u>6/</u>	V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OH} = -50 μA	All	3.0 V	1, 2, 3	2.9		V
			All	4.5 V	1, 2, 3	4.4		
			All	5.5 V	1, 2, 3	5.4		
		V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OH} = -12 mA	All	3.0 V	1	2.56		
					2, 3	2.40		
		V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OH} = -24 mA	All	4.5 V	1	3.86		
					2, 3	3.70		
		V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OH} = -24 mA	All	5.5 V	1	4.86		
					2, 3	4.70		
		V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OH} = -50 mA	All	5.5 V	1, 2, 3	3.85		
Low level output voltage 3007	V _{OL} <u>6/</u>	V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OL} = 50 μA	All	3.0 V	1, 2, 3		0.1	V
			All	4.5 V	1, 2, 3		0.1	
			All	5.5 V	1, 2, 3		0.1	
		V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OL} = 12 mA	All	3.0 V	1		0.36	
					2, 3		0.50	
		V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OL} = 24 mA	All	4.5 V	1		0.36	
					2, 3		0.50	
		V _{IN} = V _{IH} (min) or V _{IL} (max). I _{OL} = 24 mA	All	5.5 V	1		0.36	
					2, 3		0.50	
High level input voltage	V _{IH} <u>7/</u>		All	3.0 V	1, 2, 3	2.1		V
			All	4.5 V	1, 2, 3	3.15		
			All	5.5 V	1, 2, 3	3.85		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +3.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class <u>4/</u>	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit	
						Min	Max		
Low level input voltage	V _{IL} <u>7/</u>		All All	3.0 V	1, 2, 3		0.9	V	
				4.5 V	1, 2, 3		1.35		
				5.5 V	1, 2, 3		1.65		
Input leakage current low 3009	I _{IL}	For input under test, V _{IN} = GND For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1		-0.1	μA	
					2, 3		-1.0		
Input leakage current high 3010	I _{IH}	For input under test, V _{IN} = 5.5 V For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1		0.1	μA	
					2, 3		1.0		
Quiescent supply current, output high 3005	I _{CCH}	V _{IN} = V _{CC} or GND Output open	All All	5.5 V	1		4	μA	
					2, 3		80		
					M, D, P, L, R, F <u>8/</u>	01 Q, V	1		
Quiescent supply current, output low 3005	I _{CCL}	V _{IN} = V _{CC} or GND Output open	All All	5.5 V	1		4	μA	
					2, 3		80		
					M, D, P, L, R, F <u>8/</u>	01 Q, V	1		
Input capacitance 3012	C _{IN}	See 4.4.1c T _C = +25°C	All All	GND	4		10	pF	
Power dissipation capacitance	C _{PD} <u>9/</u>	See 4.4.1c T _C = +25°C, f = 1 MHz	All All	5.0 V	4		80	pF	
Functional tests 3014	<u>10/</u>	V _{IN} = V _{IH} or V _{IL} Verify output V _{OUT} See 4.4.1b	All All	3.0 V	7, 8	L	H		
				5.5 V	7, 8	L	H		
Propagation delay time, CP to Qn 3003	t _{PHL1} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	All All	3.0 V	9	1.0	13.0	ns	
					10, 11	1.0	16.0		
				4.5 V	9	1.5	10.0		
					10, 11	1.5	11.5		
	t _{PLH1} <u>11/</u>			3.0 V	9	1.0	12.5		
					10, 11	1.0	15.0		
				4.5 V	9	1.5	9.0		
					10, 11	1.5	11.0		
	Propagation delay time, $\overline{\text{MR}}$ to Qn 3003			t _{PHL2} <u>11/</u>	3.0 V	9	1.0		13.0
						10, 11	1.0		16.0
4.5 V		9	1.5		10.0				
		10, 11	1.5		11.5				

1/ For tests not listed in the referenced MIL-STD-883, [e.g. V_{IH}, V_{IL}], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

- V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.
- V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.
- All I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

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TABLE IA. Electrical performance characteristics - Continued.

- 3/ RHA parts for this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However this device is only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level for any device, $T_A = +25^\circ\text{C}$.
- 4/ The word "All" in the device type and device class column means non-RHA limits for all device types and classes.
- 5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at $3.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ and $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$.
- 6/ The V_{OH} and V_{OL} tests shall be tested at $V_{CC} = 3.0\text{ V}$, 4.5 V and 5.5 V . The V_{OH} and V_{OL} tests are guaranteed, if not tested, for other values of V_{CC} . Limits shown apply to operation at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ and $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$. Tests with output current at $+50\text{ mA}$ or -50 mA are performed on only one output at a time with duration not to exceed 10 ms. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = V_{IH}$ minimum and V_{IL} maximum. Values for subgroup 1 shall be guaranteed, if not tested, to the limits specified in table I except class V products.
- 7/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.
- 8/ The maximum limit for this parameter at 100 krad(Si) is $4.0\text{ }\mu\text{A}$.
- 9/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where:

$$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$$

$$I_S = (C_{PD} + C_L)V_{CC}f + I_{CC}$$
 f is the frequency of the input signal and C_L is the external output load capacitance.
- 10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For V_{OUT} measurements, $L \leq 0.3V_{CC}$ and $H \geq 0.7V_{CC}$.
- 11/ AC limits at $V_{CC} = 5.5\text{ V}$ are equal to the limits at $V_{CC} = 4.5\text{ V}$ and guaranteed by testing at $V_{CC} = 4.5\text{ V}$. AC limits at $V_{CC} = 3.6\text{ V}$ are equal to limits at $V_{CC} = 3.0\text{ V}$ and guaranteed by testing at $V_{CC} = 3.0\text{ V}$. Minimum ac limits for $V_{CC} = 5.5\text{ V}$ are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5\text{ V}$ minimum limits to 1.5 ns . For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	Bias for Single event latch-up (SEL) test $V_{CC} = 4.5\text{ V}$ No SEL at effective LET = 3/ 4/
01	LET $\leq 93\text{ [MeV/(mg/cm}^2\text{)]}$

- 1/ For SEP test conditions, see 4.4.4.2 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- 3/ Tested for SEL at operating temperature, $T_A = +125^\circ\text{C} \pm 10^\circ\text{C}$.
- 4/ Tested to an effective LET $\leq 93\text{ MeV/(mg/cm}^2\text{)}$ and no SEL occur.

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Note: Deviation from MIL-STD-1835 REF. F-9, CONFIG. B the dimension c is 0.003 inches minimum instead of 0.004 inches minimum and dimension Q is 0.010 inches Minimum instead of 0.026 inches minimum.

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Device type	01
Case outlines	R, S, X, Z, and 2
Terminal number	Terminal symbol
1	$\overline{\text{MR}}$
2	Q_0
3	D_0
4	D_1
5	Q_1
6	Q_2
7	D_2
8	D_3
9	Q_3
10	GND
11	CP
12	Q_4
13	D_4
14	D_5
15	Q_5
16	Q_6
17	D_6
18	D_7
19	Q_7
20	V_{CC}

FIGURE 2. Terminal connections.

Inputs			Outputs	Operating mode
$\overline{\text{MR}}$	CP	Dn	Qn	
L	X	X	L	Reset (Clear)
H	\uparrow	h	H	Load '1'
H	\uparrow	l	L	Load '0'

H = High voltage level
 L = Low voltage level
 l = Low one setup time prior to clock pulse
 h = High one setup time prior to clock pulse
 X = Immaterial
 \uparrow = Low-to-high clock transition

FIGURE 3. Truth table.

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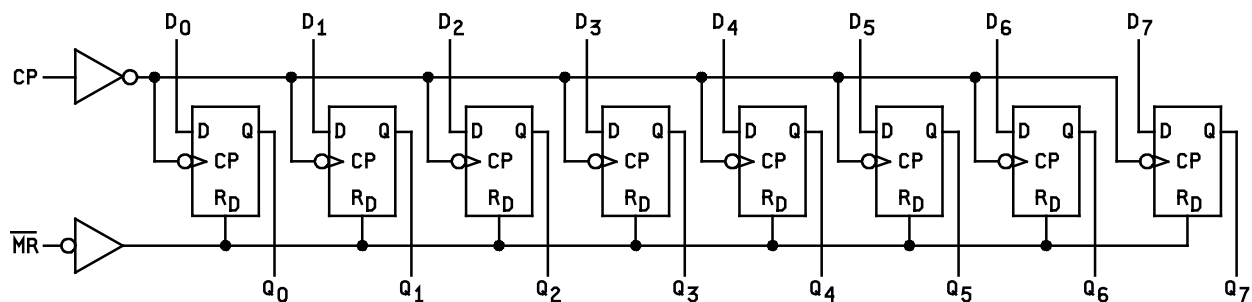


FIGURE 4. Logic diagram.

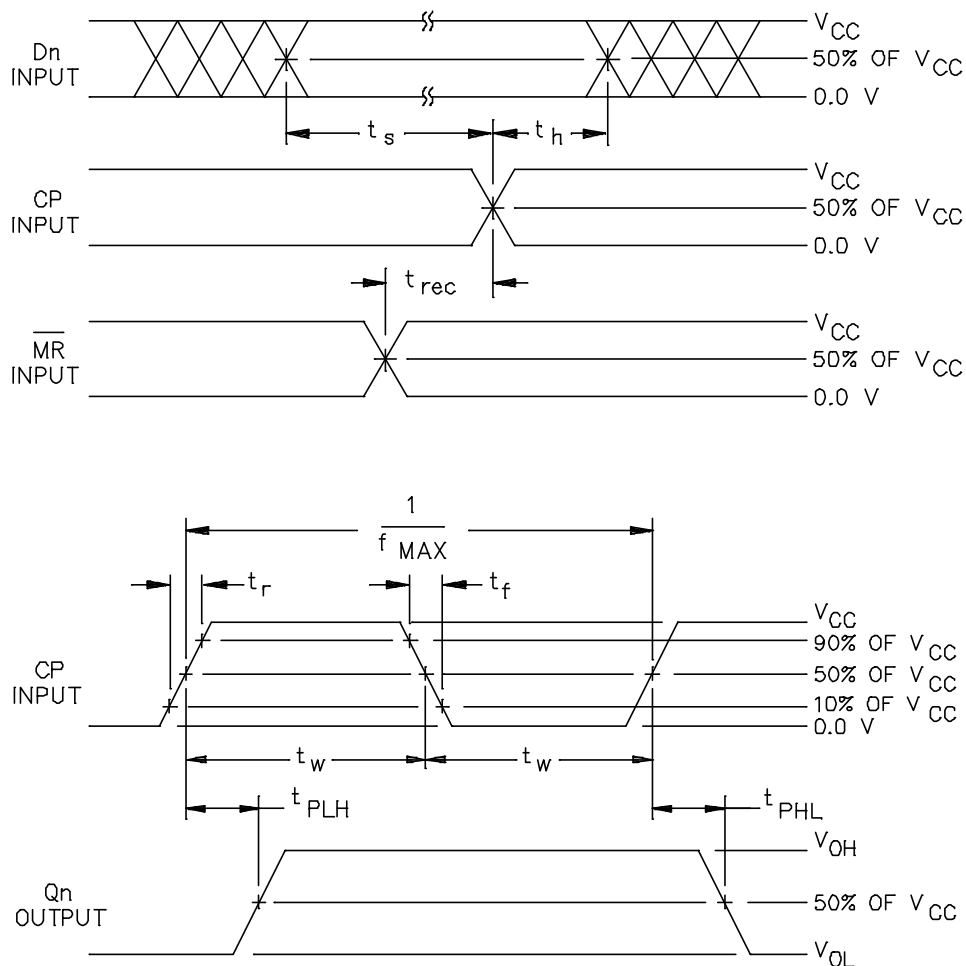


FIGURE 5. Switching waveforms and test circuit.

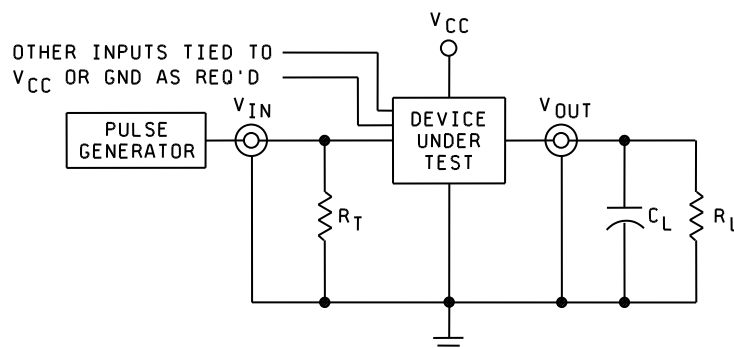
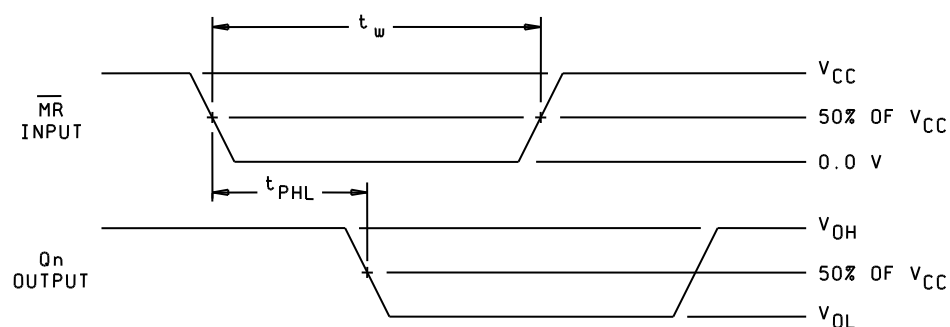
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NOTES:

1. $C_L = 50 \text{ pF}$ minimum or equivalent, (includes test jig and probe capacitance).
2. $R_T = 50\Omega$ or equivalent, $R_L = 500\Omega$ or equivalent.
3. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to V_{CC} ; $PRR \leq 1 \text{ MHz}$; $Z_O = 50\Omega$; $t_r \leq 3.0 \text{ ns}$; $t_f \leq 3.0 \text{ ns}$; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC} , respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table IA herein. For C_{IN} and C_{PD} , test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9	<u>1/</u> 1, 2, 3, 7, 8, 9	<u>2/ 3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1, 7, and deltas.

3/ Delta limits, as specified in table IIB shall be required, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C). 1/

Parameter <u>2/</u>	Symbol	Delta limits
Supply current	I _{CCH} , I _{CCL}	±300 nA
Input current low level	I _{IL}	±20 nA
Input current high level	I _{IH}	±20 nA
Output voltage low level (V _{CC} = 5.5 V, I _{OL} = 24 mA)	V _{OL}	±0.04 V
Output voltage high level (V _{CC} = 5.5 V, I _{OH} = -24 mA)	V _{OH}	±0.20 V

1/ This table is a representation of what vendor CAGE F8859 has experienced and is guaranteed and not meant to be construed as a quality assurance requirement for any other vendor.

2/ These parameters shall be recorded before and after the required Burn-in and life tests to determine the delta limits.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- T_A = +125°C, minimum.
- Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A, and as specified herein.

- a. Inputs tested high, $V_{CC} = 5.5 \text{ V dc} \pm 5\%$, $V_{IN} = 5.0 \text{ V dc} + 10\%$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.
- b. Inputs tested low, $V_{CC} = 5.5 \text{ V dc} \pm 5\%$, $V_{IN} = 0.0 \text{ V dc}$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be $+25^{\circ}\text{C}$ for the upset measurements and the maximum rated operating temperature $\pm 10^{\circ}\text{C}$ for the latch-up measurements.
- f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEP).
- d. Number of transients (SEP).
- e. Occurrence of latchup (SEP).

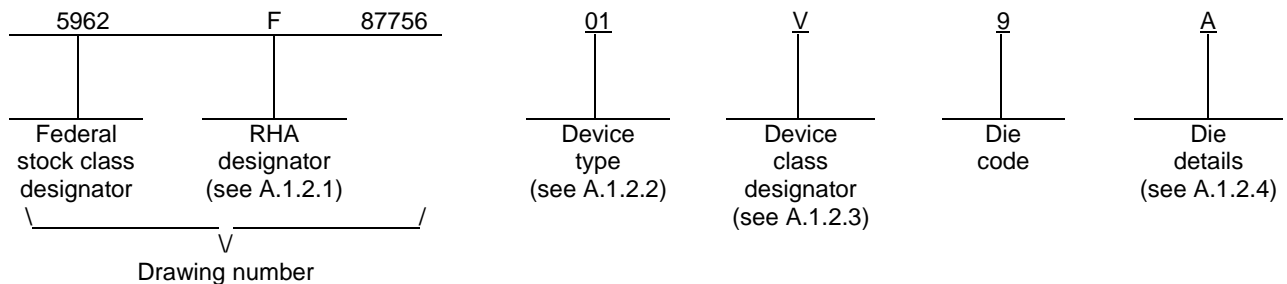
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN shall be as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AC273	Octal D-type flip-flop with master reset

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

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A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

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A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table(s). The truth table(s) shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Irradiation test connections. The irradiation test connections shall be as defined within paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4. VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer Lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

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A.5. DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6. NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0540.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-87756

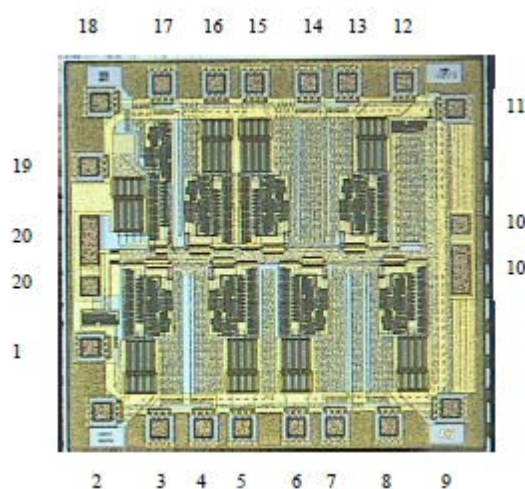


FIGURE A-1. Die bonding pad locations and electrical functions.

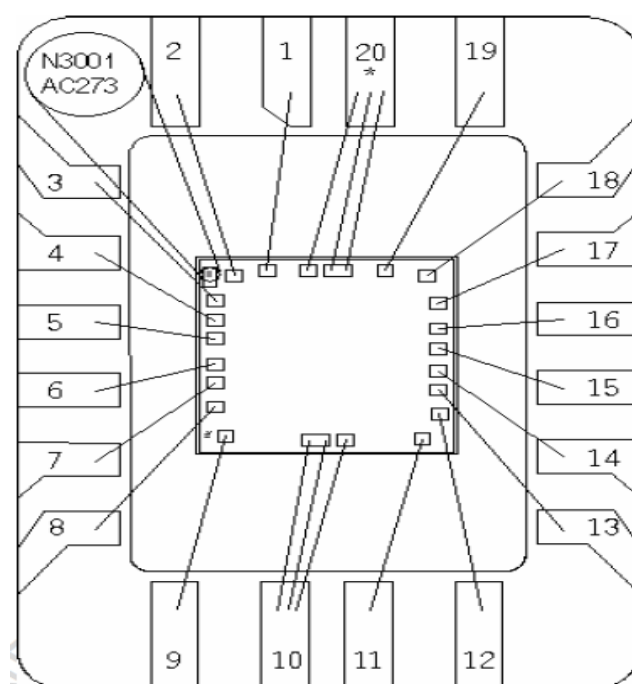


FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

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APPENDIX A
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o DIE PHYSICAL DIMENSIONS

Die size: X = 2529 μm
 Y = 2357 μm

Gross die per wafer: 650

Pad size1: 100 X 100 μm
Pad size 2: 100 X 280 μm

Sawing street: 90 μm (X); 76 μm (Y)

Wafer dia = 6 inch

Wafer thickness. 285 μm \pm 25 μm

Die finish back. Lapped Si

Die finish front. Pvpox 5000 \AA + Nitride 7000 \AA

Metallization:
1= Al (98.5%)/Si (1%)/Cu (0.5%) and thickness: 0.53 μm
2= Al (98.5%)/Si (1%)/Cu (0.5%) and thickness: 0.85 μm

FIGURE A-1. Die technical and mechanical characteristics - Continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-07-25

Approved sources of supply for SMD 5962-877560 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8775601RA	0C7V7	54AC273DMQB
5962-87756012A	0C7V7	54AC273LMQB
5962-8775601SA	0C7V7	54AC273FMQB
5962-8775601ZA	0C7V7	54AC273WG-QML
5962-8775601VSA	<u>3</u> /	54AC273
5962-8775601XA	<u>3</u> /	54AC273K02Q
5962-8775601XC	<u>3</u> /	54AC273K01Q
5962-8775601VXA	<u>3</u> /	54AC273K02V
5962-8775601VXC	<u>3</u> /	54AC273K01V
5962F8775601RA	F8859	RHFAC273D04Q
5962F8775601RC	F8859	RHFAC273D03Q
5962F8775601VRA	F8859	RHFAC273D04V
5962F8775601VRC	F8859	RHFAC273D03V
5962F8775601VXA	F8859	RHFAC273K02V
5962F8775601VXC	F8859	RHFAC273K01V
5962F8775601XA	F8859	RHFAC273K02Q
5962F8775601XC	F8859	RHFAC273K01Q
5962F8775601V9A	F8859	AC273DIE2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 12-07-25

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
0C7V7	E2V Aerospace and Defense, Inc. dba QP Semiconductor, Inc. 765 Sycamore Drive Milpitas, CA 95035
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2-FRANCE

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