REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, pages 4 and 5, change: V_{OH} from 2.5 V to 2.4 V. f_{MAX} (Min), subgroup 9, from 100 MHz to 90 MHz and subgroups 10 and 11 from 90 MHz to 75 MHz. t_{PLH4}, subgroups 10 and 11 from 15.5 ns to 16.5 ns. Add "5962" to the military drawing number in 6.4. Editorial changes on pages 2 and 8. Change code ident. to 67268.	87-07-24	D. R. Cool
B	Technical changes in 1.4, recommended operating conditions. Increased setup and hold time. Delete footnote 2/ from table I. Table I f_{MAX} test from 75 MHz to 60 MHz. Table I t_{PHL2} through t_{PHL4} increase maximum limits. Made editorial changes throughout document. Change in table II. Add CAGE 27014 to all packages. Add figure 5. - ltg	89-01-03	D. R. Cool
C	Table I, maximum clock frequency, symbol column, add "2/". Add footnote 2/ at the end of the table as follows: "2/ f_{MAX}, if not tested shall be guaranteed to the specified limits." - tvn	93-05-05	Monica L. Poelking
D	Update to reflect latest changes in format and requirements. Change $\overline{LOAD}$ to $\overline{PE}$ on Figure 4. Editorial changes throughout. - les	02-03-07	Raymond Monnin
E	Update drawing to current requirements. Editorial changes throughout. - gap	09-04-14	Joseph D. Rodenbeck

CURRENT CAGE CODE IS 67268

The original first sheet of this drawing has been replaced.

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY David W. Queenan	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY N. A. Hauck	
	APPROVED BY N. A. Hauck	MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, TTL, BINARY COUNTER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 87-01-28	
AMSC N/A	REVISION LEVEL E	SIZE A / CAGE CODE **14933** / **5962-86072**
		SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86072	01	E	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F169	synchronous 4-bit up/down binary counter

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or GDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or GDFP3-F16	16	Flat
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.2 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/	413 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, D_n to CP:	
T_C = +25°C	4.0 ns
T_C = -55°C, +125°C	4.5 ns
Minimum hold time, D_n to CP:	
T_C = +25°C	3.0 ns
T_C = -55°C, +125°C	3.5 ns

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}. Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

Minimum setup time, $\overline{CEP}$ or $\overline{CET}$ to CP:
T_C = +25°C ..... 7.0 ns
T_C = -55°C, +125°C ..... 8.0 ns
Minimum hold time, $\overline{CEP}$ or $\overline{CET}$ to CP ..... 1.0 ns
Minimum setup time, $\overline{PE}$ to CP:
T_C = +25°C ..... 8.0 ns
T_C = -55°C, +125°C ..... 10.0 ns
Minimum hold time, $\overline{PE}$ to CP ..... 1.0 ns
Minimum setup time, U/$\overline{D}$ to CP:
T_C = +25°C ..... 11.0 ns
T_C = -55°C, +125°C ..... 14.0 ns
Minimum hold time, U/$\overline{D}$ to CP ..... 0.0 ns
Minimum width of clock pulse ..... 9.0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Counting sequence. The counting sequence shall be as specified on figure 4.

3.2.6 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V		1, 2, 3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V		1, 2, 3		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IH} = -18 mA		1, 2, 3		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V		1, 2, 3		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.5 V	$\overline{CET}$ input	1, 2, 3		-1.2	mA
			other inputs	1, 2, 3		-0.6	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_{OS} = 0.0 V 1/		1, 2, 3	-60	-150	mA
Supply current	I_{CC}	V_{CC} = 5.5 V		1, 2, 3		75	mA
Functional tests		See 4.3.1c		7, 8			
Maximum clock frequency	f_{MAX} 2/	V_{CC} = 5.0 V R_L = 500Ω		9	90		MHz
				10, 11	60		MHz
Propagation delay time, CP to Q_n ($\overline{PE}$ high or low)	t_{PLH1}	C_L = 50 pF See figures 4 and 5		9		9	ns
				10, 11		12	ns
	t_{PHL1}			9		12	ns
				10, 11		16	ns
Propagation delay time, CP to $\overline{TC}$	t_{PLH2}			9		16	ns
				10, 11		21	ns
	t_{PHL2}			9		12	ns
				10, 11		15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, $\overline{CET}$ to $\overline{TC}$	t_{PLH3}	V_{CC} = 5.0 V	9		6	ns
		R_L = 500 Ω	10, 11		9	ns
	t_{PHL3}	C_L = 50 pF	9		11	ns
		See figures 4 and 5	10, 11		12	ns
Propagation delay time, U/$\overline{D}$ to $\overline{TC}$	t_{PLH4}		9		15	ns
			10, 11		16.5	ns
	t_{PHL4}		9		12	ns
			10, 11		14	ns

1/ Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.
2/ f_{MAX}, if not tested, shall be guaranteed to the specified limits.

Device type 01		
Case outlines	E and F	2
Terminal number	Terminal symbols	
1	$U/\overline{D}$	NC
2	CP	$U/\overline{D}$
3	D_0	CP
4	D_1	D_0
5	D_2	D_1
6	D_3	NC
7	$\overline{CEP}$	D_2
8	GND	D_3
9	$\overline{PE}$	$\overline{CEP}$
10	$\overline{CET}$	GND
11	Q_3	NC
12	Q_2	$\overline{PE}$
13	Q_1	$\overline{CET}$
14	Q_0	Q_3
15	$\overline{TC}$	Q_2
16	V_{CC}	NC
17		Q_1
18		Q_0
19		$\overline{TC}$
20		V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on rising clock edge
L	X	X	X	Load (D_n-Q_n)
H	L	L	H	Count up (Increment)
H	L	L	L	Count down (Decrement)
H	H	X	X	No change (hold)
H	X	H	X	No change (hold)

H = High voltage level
L = Low voltage level
X = Irrelevant

Operating mode	Inputs						Outputs	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	See note
	↑	X	X	X	l	h	H	See note
Count up	↑	h	l	l	h	X	Count up	See note
Count down	↑	l	l	l	h	X	Count down	See note
Hold (do nothing)	↑	X	h	X	h	X	q_n	See note
	↑	X	X	h	h	X	q_n	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Irrelevant
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTE: $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at terminal count. Terminal count when counting up is HHHH, and terminal count when counting down is LLLL.

FIGURE 2. Truth tables.

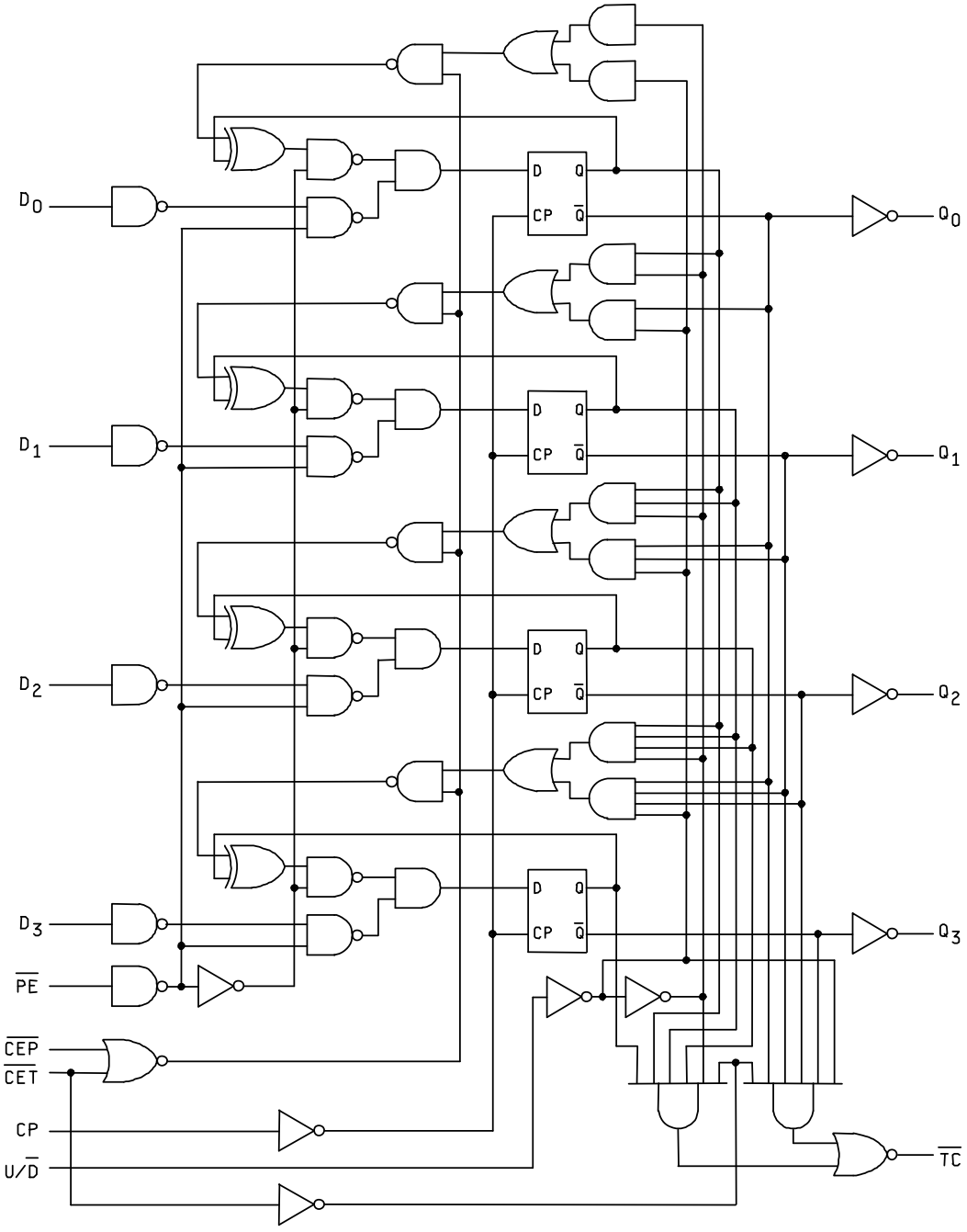
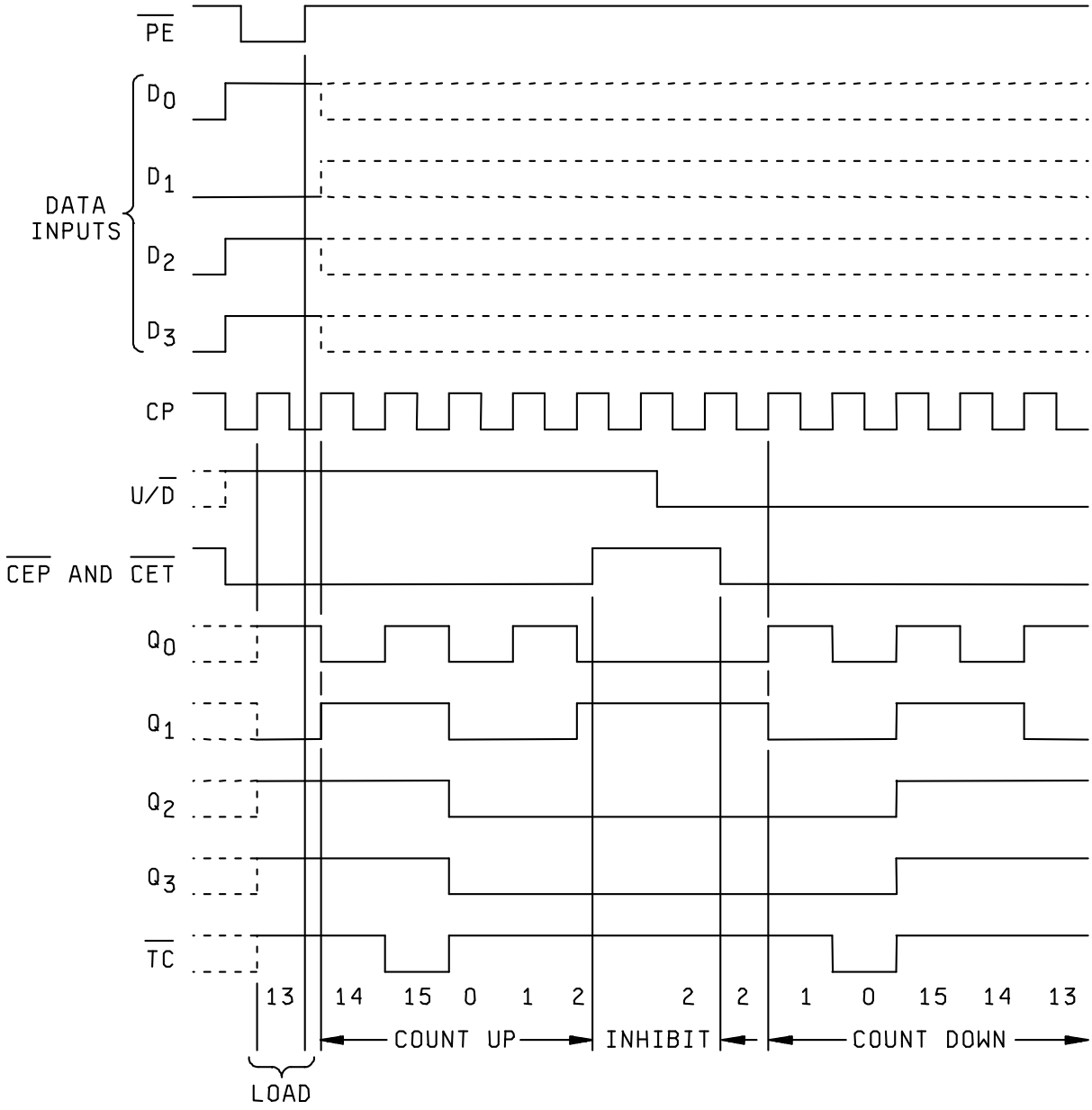
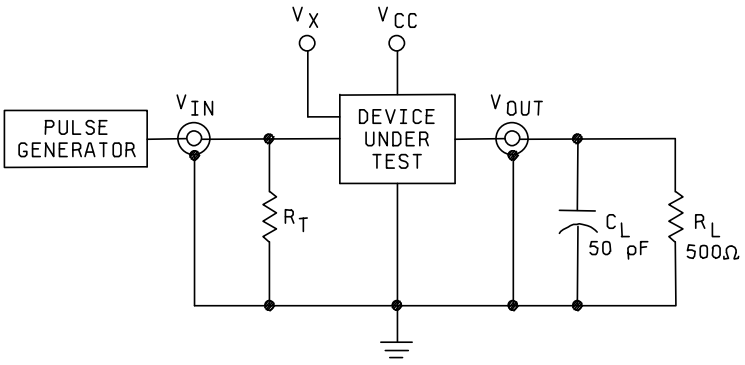


FIGURE 3. Logic diagram.

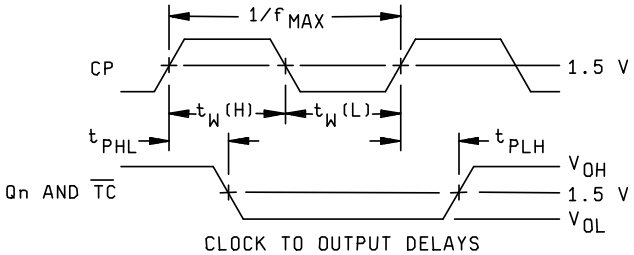


NOTES:
1. Load (presser) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

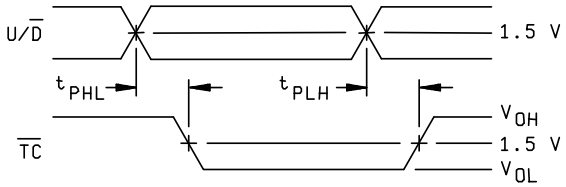
FIGURE 4. Counting sequence.



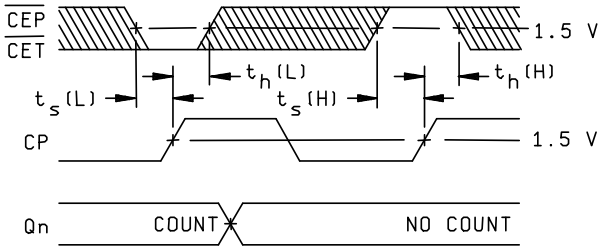
TEST CIRCUIT OR EQUIVALENT TEST CIRCUIT



CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



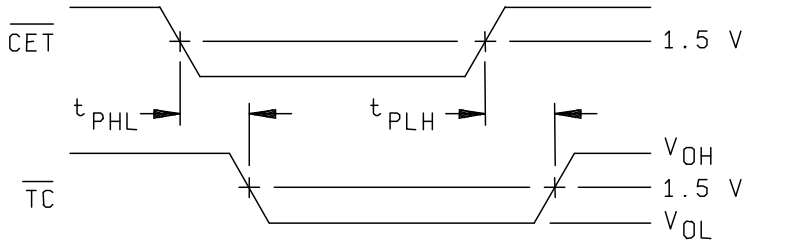
PROPAGATION DELAYS U/D CONTROL TO TERMINAL COUNT OUTPUT



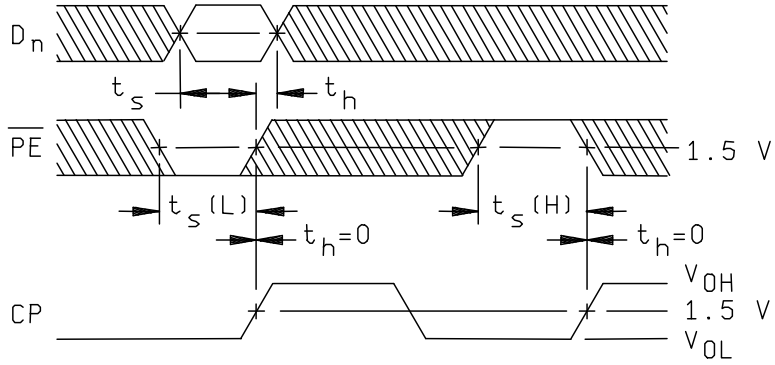
COUNT ENABLE SETUP AND HOLD TIMES

See notes at end of next page.

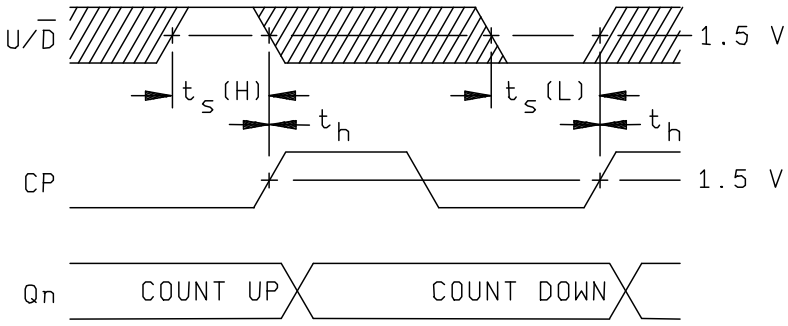
FIGURE 5. Test circuit and switching waveforms.



PROPAGATION DELAYS $\overline{CET}$ INPUT
TO TERMINAL COUNT OUTPUT



PARALLEL DATA AND PARALLEL ENABLE
SETUP AND HOLD TIMES



UP/DOWN CONTROL SETUP AND HOLD TIMES

Notes:
1. C_L = Load capacitance includes probe and jig capacitance.
2. R_T = Termination resistance should be equivalent to Z_{OUT} of pulse generators.
3. V_X = Unlocked pins must be held at ≤ 0.8 V, ≥ 2.7 V or open per function table.
4. All input pulses have the following characteristics; PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f$ = 2.5 ns ±1 ns.

FIGURE 5. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-04-14

Approved sources of supply for SMD 5962-86072 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8607201EA	0C7V7	54F169DMQB
	3/	54F169/BEA
5962-8607201FA	0C7V7	54F169FMQB
	3/	54F169/BFA
5962-86072012A	0C7V7	54F169LMQB
	3/	54F169/B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.