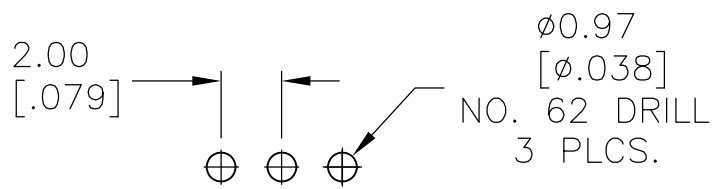
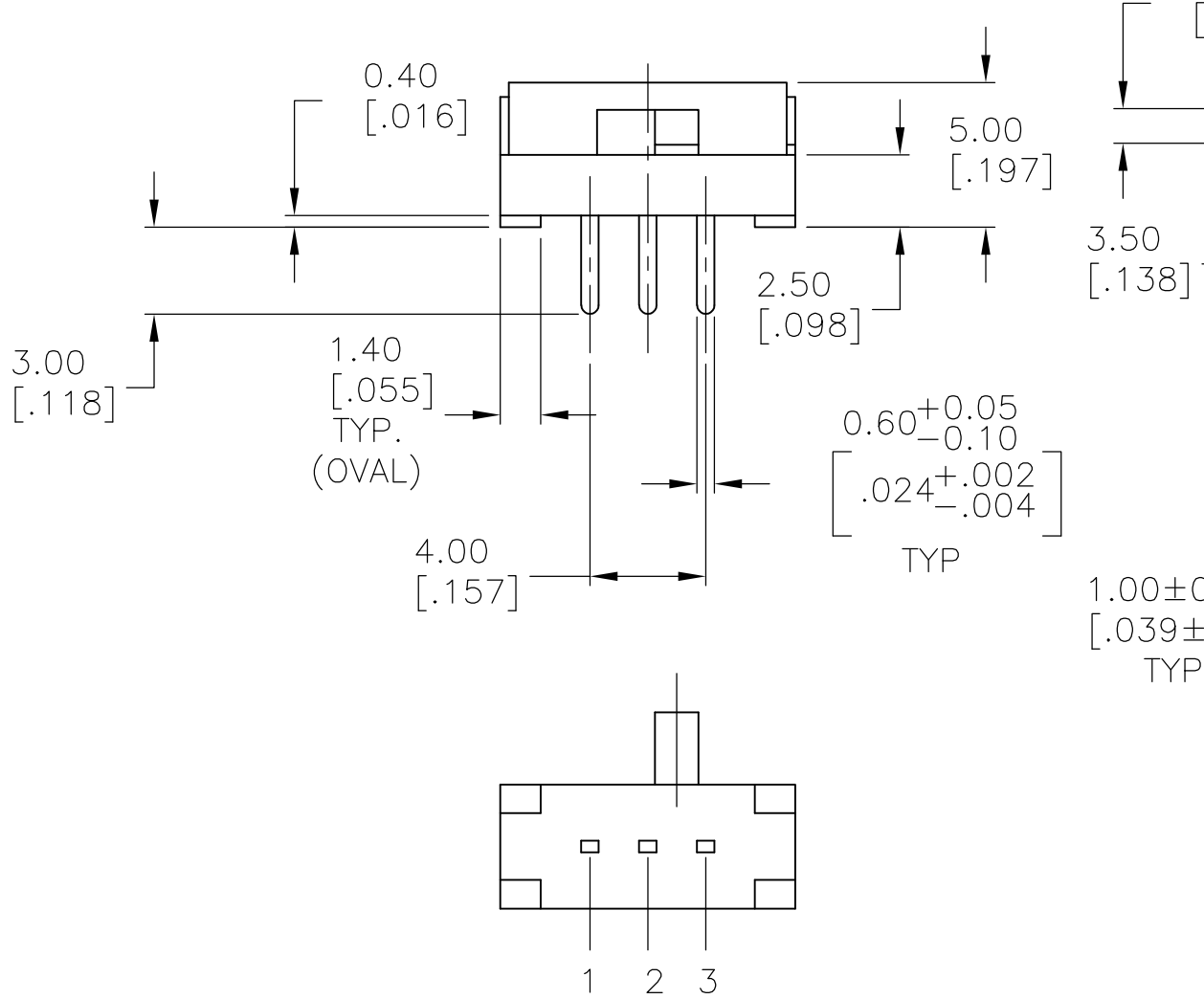


C

B

A



PCB HOLE LAYOUT
TOLERANCE ON P.C. LAYOUT
DIMENSIONS TO BE : ±.002(±.005)