54AC164245

Datasheet

Rad-hard 16-bit transceiver 3.3 V to 5 V bidirectional level shifter

The upper metallic lid can be either floating or internally connected to ground

Product status link
54AC164245

Features

- Fully compatible with the 54ACS164245
- Dual supply bidirectional level shifter
- Extended voltage range from 2.3 V to 5.5 V
- Separated enable pin for 3-state output
- Schmidt-triggered I/Os: 100 mV hysteresis
- Internal 26 Ω limiting resistor on each I/O
- High speed: Tpd = 8 ns maximum
- Fail safe
- Cold spare
- Hermetic package
- 100 krad (Si) at any Mil1019 dose rate
- SEL immune to 110 MeV.cm^2/mg LET ions
- RHA QML-V qualified
- SMD: 5962R98580

Description

The 54AC164245 is a rad-hard advanced high-speed CMOS, Schmitt trigger, 16-bit, bidirectional, multi-purpose transceiver with 3-state outputs and cold sparing.

Designed to be used as an interface between a 5 V bus and a 3.3 V bus in mixed 5 V/3.3 V supply systems, it achieves high-speed operations while the CMOS low-power dissipation is kept.

All pins have cold spare buffers to change them to high impedance when V_{DD} is tied to ground.

This IC is intended for a two-way asynchronous communication between data buses. The direction of the data transmission is determined by the nDIR inputs.

The A port interfaces with the 3.3 V bus can also operate at 2.3 V. The B port operates with the 5 V bus.

The 54AC164245 is packaged in hermetic ceramic Flat 48-lead screened as per MIL-PRF-38535 to comply with the needs of space applications. It is available with the upper metallic lid either floating or internally connected to ground.

1 Functional description

Figure 1. Logic diagram

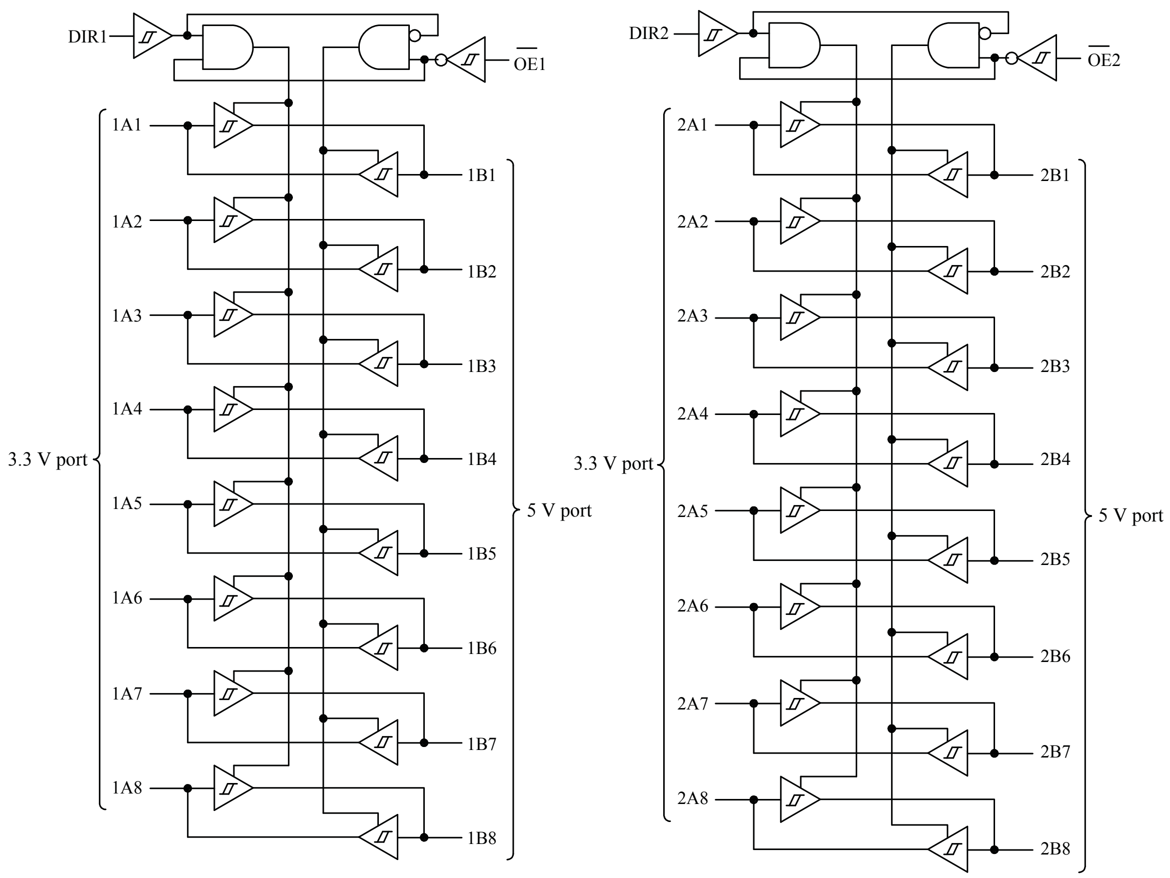


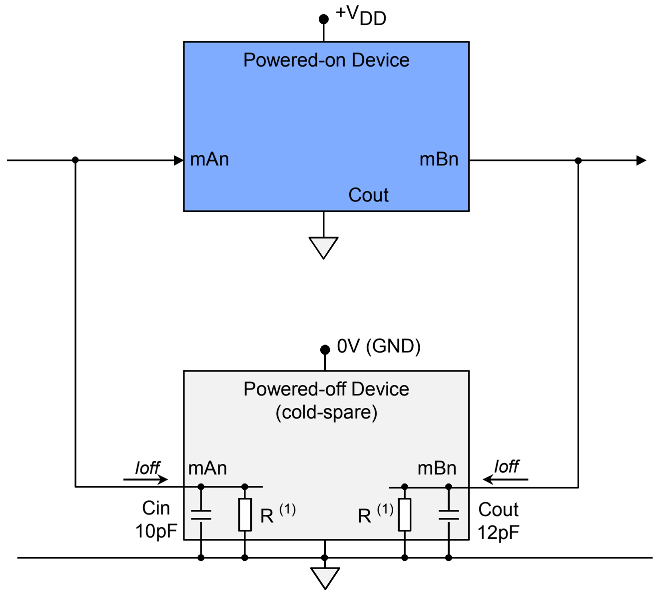
Table 1. Function table

Enable, OEx	Direction, DIRx	Operation
L	L	B data to A bus
	H	A data to B bus
H	X	Isolation

1.1 Cold spare

The 54AC164245 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V ($V_{DD} = V_{SS} = 0$ V, $V_{DD} - V_{SS} = 0$ V) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices that are not powered to be switched on only when required. Power consumption is therefore reduced by switching off the redundant circuit. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between I/Os and V_{DD}. The ESD protection is ensured through a non-conventional dedicated structure. Using cold spare on bus A and bus B separately is not allowed. In cold spare, both V_{DD1} and V_{DD2} must be at 0 V.

Figure 2. Cold spare and cold redundancy



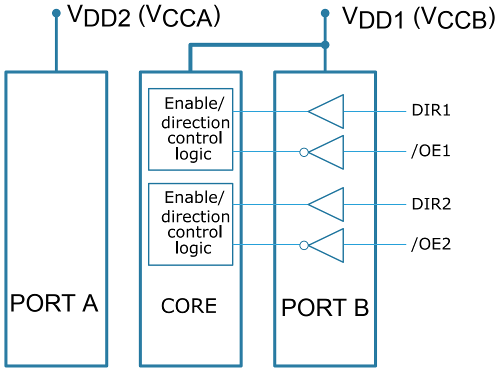
1. $R = Ioff/V_{DD}$

1.2 Power-up

During power-up, all outputs are forced to high impedance. The high impedance state is maintained approximately until V_{DD} is high, thus avoiding any transient and erroneous signals during power-up.

However, the 54AC164245 must be supplied with V_{DD1} (V_{CCB}) higher or equal to V_{DD2} (V_{CCA}).

Figure 3. Power-up



1. In operating mode, V_{DD1} (V_{CCB}) must be higher than or equal to V_{DD2} (V_{CCA}). V_{DD2} higher than V_{DD1} is forbidden.
2. In power-up, V_{DD1} (V_{CCB}) must be powered up before V_{DD2} (V_{CCA}).
3. In power-down, V_{DD2} (V_{CCA}) must be powered down before V_{DD1} (V_{CCB}).
4. Control signals: DIRx and OEx are 5 volt tolerant inputs. Corresponding CMOS logic levels that apply to all control inputs are: V_{ILmax} = 0.3VDD1 and V_{IHmin} = 0.7VDD1. For a proper operation, connect power to all V_{DD} and ground all V_{SS} pins (i.e., no floating VDD or VSS input pins). Tie unused inputs to V_{SS}.

1.3 Pin connections

Figure 4. Pin connections

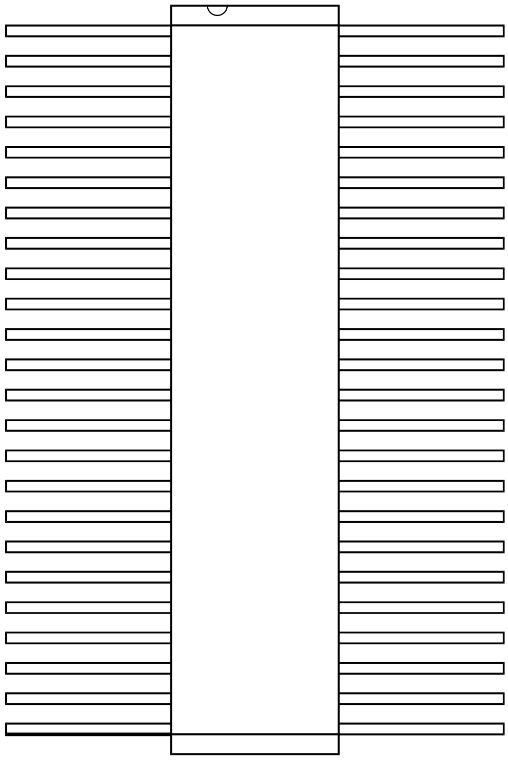


Table 2. Pin descriptions

Pin number	Symbol	Name and function
1	DIR1	Direction control inputs
2, 3, 5, 6, 8, 9, 11, 12	1B1 to 1B8	Side B inputs or 3-state outputs (5 V port)
4,10, 15, 21, 28, 34, 39, 45	V_{SS}	Reference voltage to ground
7, 18	V_{DD1}	Supply voltage (5 V)
13, 14, 16, 17, 19, 20, 22, 23	2B1 to 2B8	Side B inputs or 3-state outputs (5 V port)
24	DIR2	Direction control inputs
25	nG2	Output enable inputs (active low)
31, 42	V_{DD2}	Supply voltage (3.3 V)
47, 46, 44, 43, 41, 40, 38, 37	1A1 to 1A8	Side A inputs or 3-state outputs (3.3 V port)
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Side A inputs or 3-state outputs (3.3 V port)
48	nG1	Output enable inputs (active low)

Note: Concerning the RHRAC164245K01V: the upper metallic lid is floating (not connected to any pins); while concerning the RHRAC164245K03V: the upper metallic lid is connected to ground pins.

2 Absolute maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Unless otherwise noted, all voltages are referenced to V_{SS}.

The limits for the parameters specified in Table 3. Absolute maximum ratings apply over the full specified V_{DD} range and case temperature range of -55 °C to 125 °C.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD1}	5 V supply voltage (1)	-0.3 to 7	V
V_{DD2}	3 V supply voltage		
V_{IA}	DC input voltage range port A	-0.3 to V_{DD1} + 0.3 V	
V_{IB}	DC input voltage range port B		
V_{OA}	DC output voltage range port A		
V_{OB}	DC output voltage range port B		
I_{IA}	DC input currents port A, anyone input	± 10	mA
I_{IB}	DC input currents port B, anyone input		
T_{stg}	Storage temperature range	-65 to 150	°C
T_L	Lead temperature (10 s)	300	
T_J	Junction temperature range	175	
R_{thjc}	Thermal resistance junction to case (2)	8	°C/W
ESD	HBM: human body model (3)	2	kV

1. *V_{DD1} must be higher or equal to V_{DD2} (V_{DD2} higher than V_{DD1} is forbidden).*
2. *Short-circuits can cause excessive heating and destructive dissipation. Values are typical.*
3. *Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.*

In Table 4. Operating conditions, unless otherwise noted, all voltages are referenced to V_{SS}.

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD1}	Supply voltage (1)	4.5 to 5.5 or 2.3 to 3.6	V
V_{DD2}		2.3 to 3.6 or 4.5 to 5.5	
V_I	Input voltage on A port	0 to V_{DD2}	
	Input voltage on B port	0 to V_{DD1}	
	Input voltage control inputs (OE1, OE2, DIR1, DIR2)		
V_O	Output voltage	0 to V_{DD1}	
T_{op}	Operating temperature	-55 to 125	°C
d_t / d_v	Input rise and fall time V_{CC} = 3.0, 4.5 or 5.5 (2)	0 to 8	ns / V

1. *V_{DD1} must be higher or equal to V_{DD2} (V_{DD2} higher than V_{DD1} is forbidden).*
2. *Derates system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.*

3 Electrical characteristics

In the table below, T_{op} = -55 °C to 125 °C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 2.7 V to 3.6 V, unless otherwise specified. Each input/output, as applicable, is tested at the specified temperature, for the specified limits, according to the tests specified in TABLE IA from the SMD 5962-98580 DLA Agency Spec. Non-designated output terminals are high-level logic, low-level logic or open, except for all I_{DD} tests, where the output terminals are open. When performing these tests, the current meter must be placed in the circuit so that all current flows through the meter.

Table 5. **DC specifications**

Symbol	Parameter	Port voltage	Test conditions (V_{DD}) (1)	Limits		Unit
				Min.	Max.	
V_{T+}	Schmitt trigger positive going threshold port A	3.3 V	V_{DD1} = 4.5 and 5.5 V		0.7 V_{DD2}	V
			V_{DD2} = 2.7 and 3.6 V			
		5 V	V_{DD1} = 4.5 and 5.5 V			
			V_{DD2} = 4.5 and 5.5 V			
	Schmitt trigger positive going threshold port B	3.3 V	V_{DD2} = 2.7 and 3.6 V		0.7 V_{DD1}	
			V_{DD1} = 2.7 and 3.6 V			
		5 V	V_{DD1} = 4.5 and 5.5 V			
			V_{DD2} = 2.7 and 3.6 V			
V_{T-}	Schmitt trigger positive going threshold port A	3.3 V	V_{DD1} = 4.5 and 5.5 V		0.3 V_{DD2}	
			V_{DD2} = 2.7 and 3.6 V			
		5 V	V_{DD1} = 4.5 and 5.5 V			
			V_{DD2} = 4.5 and 5.5 V			
	Schmitt trigger positive going threshold port B	3.3 V	V_{DD2} = 2.7 and 3.6 V		0.3 V_{DD1}	
			V_{DD1} = 2.7 and 3.6 V			
		5 V	V_{DD1} = 4.5 and 5.5 V			
			V_{DD2} = 2.7 and 3.6 V			
V_H	Schmitt trigger range of hysteresis port A	3.3 V	V_{DD1} = 4.5 and 5.5 V	0.4		
			V_{DD2} = 2.7 and 3.6 V			
		5 V	V_{DD1} = 4.5 and 5.5 V	0.6		
			V_{DD2} = 4.5 and 5.5 V			
	Schmitt trigger range of hysteresis port B	3.3 V	V_{DD2} = 2.7 and 3.6 V	0.4		
			V_{DD1} = 2.7 and 3.6 V			
		5 V	V_{DD1} = 4.5 and 5.5 V	0.6		
			V_{DD2} = 2.7 and 3.6 V			

Symbol	Parameter	Port voltage	Test conditions (V_{DD}) [(1)]	Limits		Unit
				Min.	Max.	
I_{IH}	Input current high port A (for input under test $V_I = V_{DD2}$ other inputs, $V_I = V_{DD2}$ or V_{SS})	3.3 V	V_{DD1} = 5.5 V		3	µA
			V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V			
			V_{DD2} = 5.5 V			
	Input current high port B (for input under test $V_I = V_{DD1}$ other inputs, $V_I = V_{DD1}$ or V_{SS})	3.3 V	V_{DD1} = 3.6 V			
			V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V			
			V_{DD2} = 3.6 V			
I_{IL}	Input current low port A (for input under test $V_I = V_{SS}$ other inputs, $V_I = V_{DD2}$ or V_{SS})	3.3 V	V_{DD1} = 5.5 V	-1		
			V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V			
			V_{DD2} = 5.5 V			
	Input current low port B (for input under test $V_I = V_{SS}$ other inputs, $V_I = V_{DD1}$ or V_{SS})	3.3 V	V_{DD1} = 3.6 V			
			V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V			
			V_{DD2} = 3.6 V			
I_{CS}	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 5.5 V, $\overline{OEn}$ = 5.5 V		V_{DD1} = 0 V	-1	5	
	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 0V, $\overline{OEn}$ = 5.5 V					
	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 5.5 V, $\overline{OEn}$ = 0 V					
	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 0 V, $\overline{OEn}$ = 0 V					
V_{OL1}	Low level output voltage port A, I_{OL} = 8 mA for all inputs affecting output under test, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 V		0.5	V
			V_{DD2} = 2.7 V			
		5 V	V_{DD1} = 4.5 V		0.4	
			V_{DD2} = 4.5 V			
	Low level output voltage port B, I_{OL} = 8 mA for all inputs affecting output under test, $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 2.7 V		0.5	
			V_{DD2} = 2.7 V			
		5 V	V_{DD1} = 4.5 V		0.4	
			V_{DD2} = 2.7 V			

Symbol	Parameter	Port voltage	Test conditions (V_{DD}) [1]	Limits		Unit
				Min.	Max.	
V_{OL2}	Low level output voltage	3.3 V	V_{DD1} = 4.5 V		0.2	V
			V_{DD2} = 2.7 V			
	Port A, I_{OL} = 100 µA for all inputs affecting output under test, V_I = V_{DD2} or V_{SS}	5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 4.5 V			
	Low level output voltage	3.3 V	V_{DD1} = 2.7 V			
			V_{DD2} = 2.7 V			
	Port B, I_{OL} = 100 µA for all inputs affecting output under test, V_I = V_{DD1} or V_{SS}	5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 2.7 V			
V_{OH1}	High level output voltage port A, I_{OH} = -8 mA for all inputs affecting output under test, V_I = V_{DD2} or V_{SS}	3.3 V	V_{DD1} = 4.5 V	V_{DD2}-0.9		
			V_{DD2} = 2.7 V			
		5 V	V_{DD1} = 4.5 V	V_{DD2}-0.7		
			V_{DD2} = 4.5 V			
	High level output voltage port B, I_{OH} = -8 mA for all inputs affecting output under test, V_I = V_{DD1} or V_{SS}	3.3 V	V_{DD1} = 2.7 V	V_{DD1}-0.9		
			V_{DD2} = 2.7 V			
		5 V	V_{DD1} = 4.5 V	V_{DD1}-0.7		
			V_{DD2} = 2.7 V			
V_{OH2}	High level output voltage port A, I_{OH} = - 100 µA for all inputs affecting output under test, V_I = V_{DD2} or V_{SS}	3.3 V	V_{DD1} = 4.5 V	V_{DD2}-0.2		
			V_{DD2} = 2.7 V			
		5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 4.5 V			
	High level output voltage port B, I_{OH} = - 100 µA for all inputs affecting output under test, V_I = V_{DD1} or V_{SS}	3.3 V	V_{DD1} = 2.7 V	V_{DD1}-0.2		
			V_{DD2} = 2.7 V			
		5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 2.7 V			

Symbol	Parameter	Port voltage	Test conditions (V_{DD}) (1)	Limits		Unit
				Min.	Max.	
I_{OL} (2)	Output current (sink) port A, $V_I = V_{SS}$	3.3 V	V_{DD1} = 4.5 V	8.0		mA
			V_{DD2} = 2.7 V			
			V_{OL} = 0.5 V			
		5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 4.5 V			
			V_{OL} = 0.4 V			
	Output current (sink) port B, $V_I = V_{SS}$	3.3 V	V_{DD1} = 2.7 V			
			V_{DD2} = 2.7 V			
			V_{OL} = 0.5 V			
		5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 2.7 V			
			V_{OL} = 0.4 V			
I_{OH} (3)	Output current (source) port A, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 V	-8.0		
			V_{DD2} = 2.7 V			
			$V_{OH} = V_{DD2}$-0.9 V			
		5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 4.5 V			
			$V_{OH} = V_{DD2}$-0.7 V			
	Output current (source) port B, $V_I = V_{DD2}$ or V_{SS}	3 V	V_{DD1} = 2.7 V			
			V_{DD2} = 2.7 V			
			$V_{OH} = V_{DD2}$-0.9 V			
		5 V	V_{DD1} = 4.5 V			
			V_{DD2} = 2.7 V			
			$V_{OH} = V_{DD2}$-0.7 V			
I_{OZH}	Three-state output leakage current high port A, for input under test, $V_I = V_{DD2}$ other inputs, $V_O = V_{DD2}$ $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 5.5 V		3.0	µA
			V_{DD2} = 3.6 V			
			V_{DD1} = 5.5 V			
			V_{DD2} = 5.5 V			
	Three-state output leakage current high port B, for input under test, $V_I = V_{DD1}$ other inputs, $V_O = V_{DD1}$ $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 3.6 V			
			V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V			
			V_{DD2} = 3.6 V			

Symbol	Parameter	Port voltage	Test conditions (V_{DD}) [1]	Limits Min.	Limits Max.	Unit
I_{OZL}	Three-state output leakage current low port A, for input under test, $V_I = V_{SS}$ other inputs, $V_O = V_{SS}$ $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 5.5 V	-1.0		µA
			V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V			
			V_{DD2} = 5.5 V			
	Three-state output leakage current low port B, for input under test, $V_I = V_{SS}$ other inputs, $V_O = V_{SS}$ $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 3.6 V			
			V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V			
			V_{DD2} = 3.6 V			
I_{OS} [4]	Short-circuit output current port A, $V_O = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 to 5.5 V	-100	100	mA
			V_{DD2} = 2.7 to 3.6 V			
		5 V	V_{DD1} = 4.5 to 5.5 V	-200	200	
			V_{DD2} = 4.5 to 5.5 V			
	Short-circuit output current port B, $V_O = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 2.7 to 3.3 V	-100	100	
			V_{DD2} = 2.7 to 3.6 V			
		5 V	V_{DD1} = 4.5 to 5.5 V	-200	200	
			V_{DD2} = 2.7 to 3.6 V			
P_D [5]	Power dissipation, port A, C_L = 50 pF per switching output	3.3 V	V_{DD1} = 4.5 to 5.5 V		1.5	mW/MHz
			V_{DD2} = 2.7 to 3.6 V			
		5 V	V_{DD1} = 4.5 to 5.5 V		2.0	
			V_{DD2} = 4.5 to 5.5 V			
	Power dissipation, port B, C_L = 50 pF per switching output	3.3 V	V_{DD1} = 2.7 to 3.3 V		1.5	
			V_{DD2} = 2.7 to 3.6 V			
		5 V	V_{DD1} = 4.5 to 5.5 V		2.0	
			V_{DD2} = 2.7 to 3.6 V			
I_{DDQ}	Quiescent supply current port A, $V_I = V_{DD2}$ or V_{SS}	5 V	V_{DD1} = 5.5 V at 25 °C		10	µA
			V_{DD2} = 5.5 V at 25 °C			
			V_{DD1} = 5.5 V at -55 to 125 °C		100	
			V_{DD2} = 5.5 V at -55 to 125 °C			
	Quiescent supply current port B, $V_I = V_{DD1}$ or V_{SS}	5 V	V_{DD1} = 5.5 V at 25 °C		10	
			V_{DD2} = 5.5 V at 25 °C			
			V_{DD1} = 5.5 V at -55 to 125 °C		100	
			V_{DD2} = 5.5 V at -55 to 125 °C			
C_I	Input capacitance		f = 1 MHz $V_{DD1} = V_{DD2}$ = 0 V		15	pF
C_O	Output capacitance		f = 1 MHz $V_{DD1} = V_{DD2}$ = 0 V			
[6]	Functional test $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$		V_{DD1} = 4.5 to 5.5 V	L	H	
			V_{DD2} = 2.7 to 3.6 V			

1. *This device requires both V_{DD1} and V_{DD2} power supplies for operation. The power supply is indicated and followed by the voltage to which the power supply is set to the given test.*
2. *This parameter is supplied as a design limit but not guaranteed or tested.*
3. *Power does not include power contribution of any CMOS output sink current.*
4. *No more than one output should be shorted at a time for a maximum duration of one second.*
5. *Power dissipation specified per switching output.*
6. *Tests must be performed in sequence and include attribute data only. Functional tests should include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table must, at the minimum, test all the functions of each input and output. All possible input to output logic patterns per function should be guaranteed, if not tested, to Table 1. Function table. Functional tests are performed in sequence as approved by the qualifying activity on qualified devices. Functional tests are in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min + 20%, -0%); V_{IL} = V_{IL}(max + 0%, -50%), as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices are guaranteed to V_{IH}(min) and V_{IL}(max).*

In the table below, data are guaranteed by design but, not tested.

Table 6. **AC electrical characteristics**

Symbol	Parameter	Port voltage	Test condition (V_{DD})	Limits		Unit
				Min.	Max.	
t_{PLH}	Propagation delay time, data to bus (active low) C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V	1.0	20	ns
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V			
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		15	
			V_{DD2} = 4.5 to 5.5 V			
t_{PHL}	Propagation delay time, data to bus (active high) C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		20	
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V			
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		15	
			V_{DD2} = 4.5 to 5.5 V			
t_{PZL}	Propagation delay time, output enable, $\overline{OEn}$ to bus (active low), C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		18	
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V		18	
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		12	
			V_{DD2} = 4.5 to 5.5 V			
t_{PZH}	Propagation delay time, output enable, $\overline{OEn}$ to bus (active high), C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		18	
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V			
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		12	
			V_{DD2} = 4.5 to 5.5 V			
t_{PLZ}	Propagation delay time, output disable, $\overline{OEn}$ to bus (low impedance), C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		20	
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V			
			V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		15	
			V_{DD2} = 4.5 to 5.5 V			

Symbol	Parameter	Port voltage	Test condition (V_{DD})	Limits		Unit
				Min.	Max.	
t_{PHZ}	Propagation delay time, output disable, $\overline{OEn}$ to bus (high impedance), C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V	1.0	18	ns
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V			
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		12	
			V_{DD2} = 4.5 to 5.5 V			
t_{PZL}	Propagation delay time, output enable, DIRn to bus (active low), C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		18	
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V			
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		12	
			V_{DD2} = 4.5 to 5.5 V			
t_{PZH}	Propagation delay time, output enable, DIRn to bus (active high), C_L = 50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		18	
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V			
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		12	
			V_{DD2} = 4.5 to 5.5 V			
t_{PLZ}	Propagation delay time, output disable, DIRn to bus (low impedance), C_L =50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		20	
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V			
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		15	
			V_{DD2} = 4.5 to 5.5 V			
t_{PHZ}	Propagation delay time, output disable, DIRn to bus (high impedance), C_L =50 pF	Port A = 3.3 V, Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		20	
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V			
			V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V		15	
			V_{DD2} = 4.5 to 5.5 V			

4 Radiations

Total dose (MIL-STD-883 TM 1019):

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specifications.

The 54AC164245 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specifications, between 50 and 300 rad/s only (full CMOS technology).

All parameters, provided in Table 5. DC specifications and Table 6. AC electrical characteristics, apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID)
- The initial characterization is performed in qualification only on both biased and unbiased parts
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification

Heavy-ions

The behavior of the product when submitted to heavy-ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

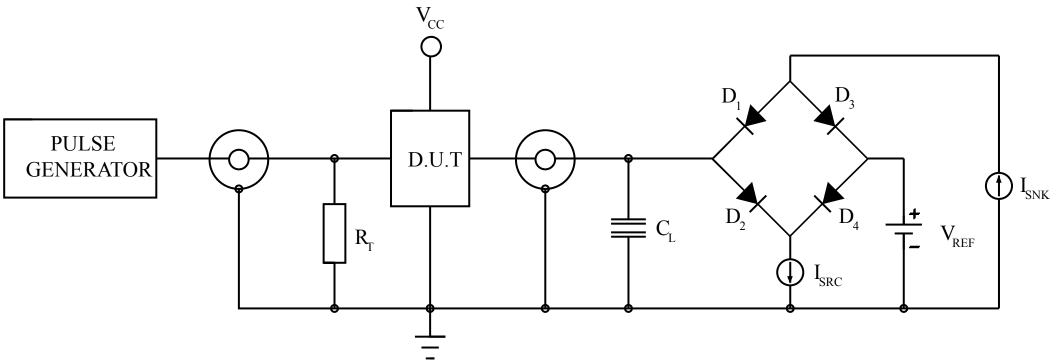
Table 7. Radiation

Type	Characteristics	Value	Unit
TID(1)	Total ionizing dose, high-dose rate (50 - 300 rad/s) up to:	100	krad
Heavy-ions	SEL(2) immune up to: (with a particle angle of 60 ° at 125 °C and a fluence of $1x10^7$n/cm^2)	110	MeV.cm²/mg
	SEL immune up to: (with a particle angle of 0 ° at 125 °C and a fluence of $1x10^7$n/cm^2)	55	
	SET(3) immune up to: (at 25 °C, and a fluence of $1x10^6$ n/cm^2)	64	

1. *A total ionizing dose (TID) of 100 krad(Si) is equivalent to $1x10^3$ Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up.*
3. *SET: single event transient*

5 Test circuit

Figure 5. Test circuit



1. C_L = 50 pF or equivalent (includes jig and probe capacitance), R_T = Z_{OUT} of pulse generator (typically 50 Ω), V_{REF} = 0.5 V_{DD}. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements. Input signal from pulse generator: V_I = 0.0 V to V_{DD}; f = 10 MHz; t_r = 1.0 V/ns "0.3 V/ns; t_f = 1.0 V/ns "0.3 V/ns; t_r and t_f are measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD} respectively.

Figure 6. Waveform 1: propagation delay

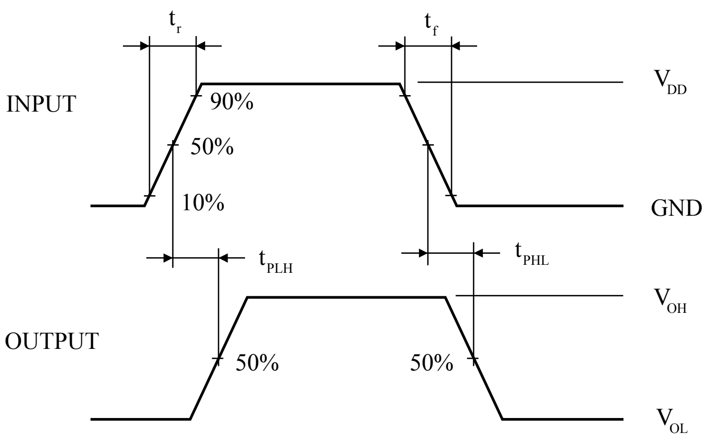


Figure 7. **Waveform 2: enable and disable times (port A = port B, 5 V operation)**

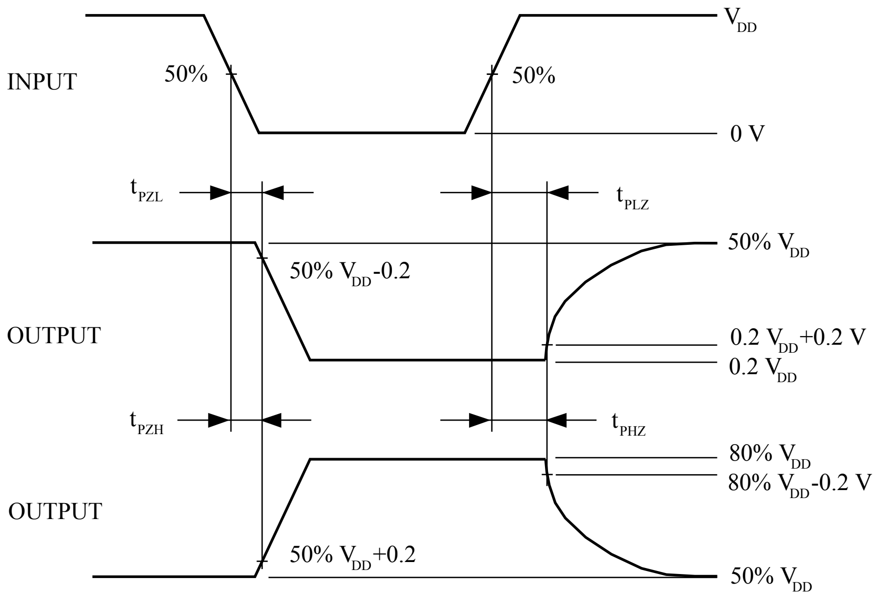


Figure 8. **Waveform 3: enable and disable times (port A = port B, 3.3 V operation)**

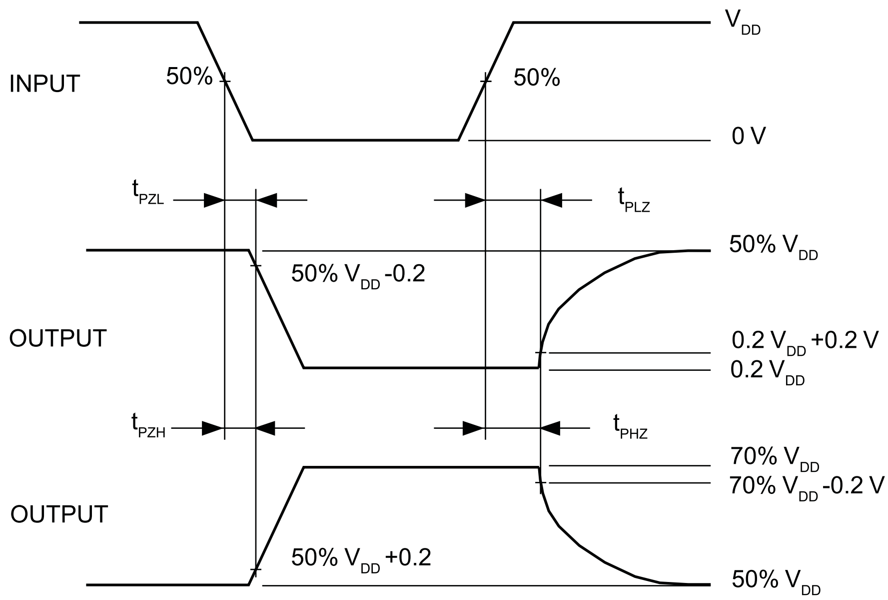
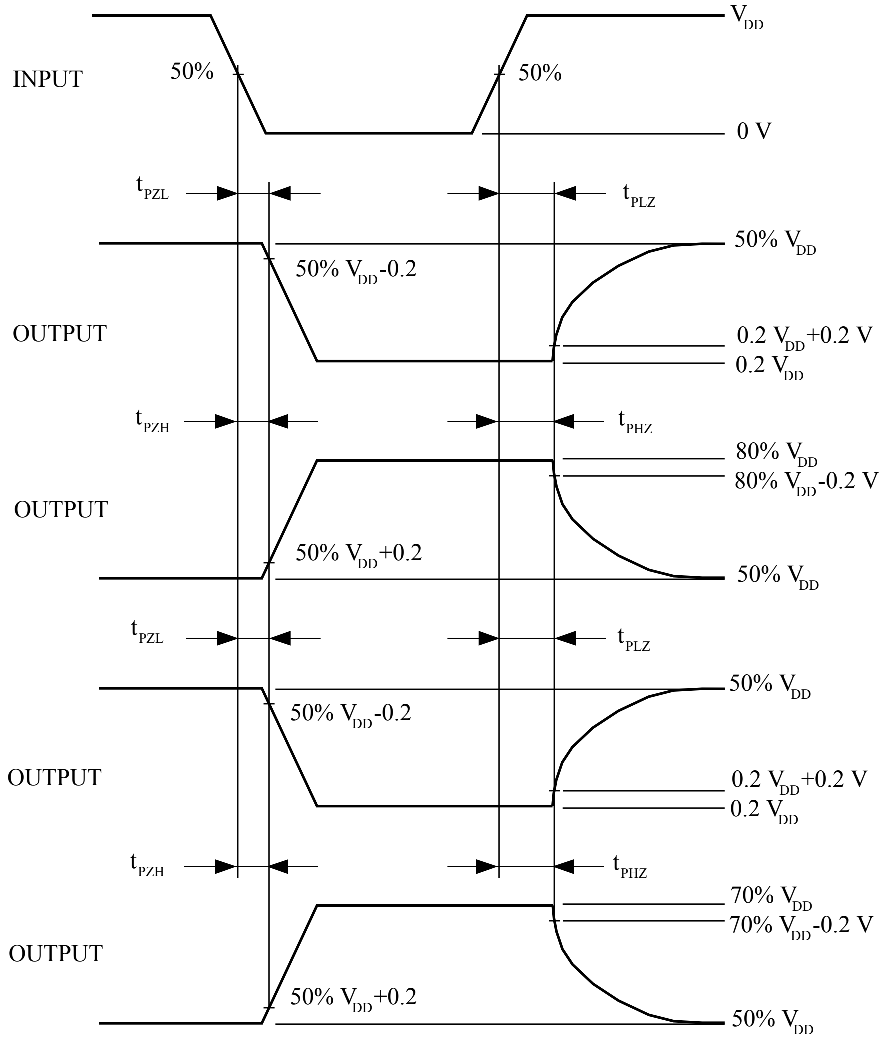


Figure 9. Waveform 4: enable and disable times (port A = 3.3 V, port B = 5 V)



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.1 Ceramic Flat-48 package information

Figure 10. Ceramic Flat-48 package outline

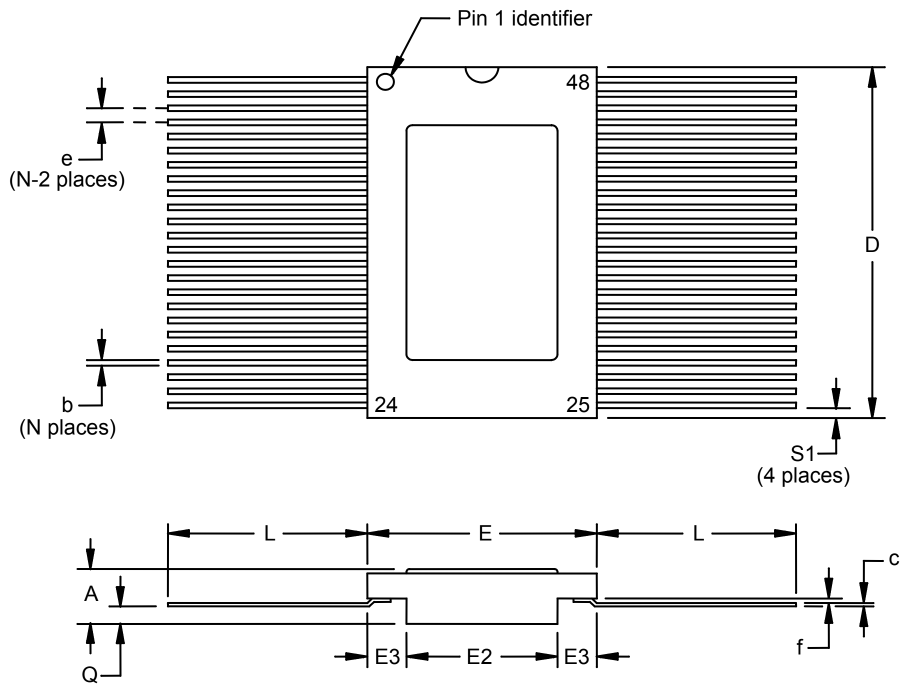


Table 8. **Ceramic Flat-48 mechanical data**

Ref.	Dimensions					
	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	6.85	8.38	9.40	0.270	0.330	0.370
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

7 Ordering information

Table 9. **Order code**

Order code	SMD	Quality level	Lid	Mass	Package	Lead finish	Marking(1)	Packing
RHRAC164245K1	-	Engin. model	-	1.5 g	Flat-48	Gold	RHRAC164245K1	Conductive strip pack
RHRAC164245K01V	5962R9858008VYC	QML-V flight	Floating				5962R9858008VYC	
RHRAC164245K03V	5962R9858008VZC		Internally grounded				5962R9858008VZC	

1. *Specific marking only. Complete marking includes the following:*
    - *ST logo*
    - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
    - *Country of origin (FR = France)*

Note: Contact your ST sales office for information about the specific conditions for products in die form.

8 Other information

Date code:

The date code is structured as engineering model: EM xyywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 10. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID

Quality level	Item
QML-V Flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
23-Sep-2011	1	Initial release.
06-Apr-2012	2	Added Pin 4 description to Table 3: "pin descriptions".
29-Aug-2013	3	Minor changes to layout Features: removed “Bus hold” Table 1: updated order codes, quality level, and EPPL data. Table 10: "Order codes": updated order codes and description data. Added Section 8: "Other information"
28-Apr-2014	4	Table 11: "Documentation provided for ESCC flight": removed documentation for engineering model (there is none). Updated disclaimer
27-Jul-2015	5	Table 4: "Absolute maximum ratings": removed R_{thja} and updated R_{thjc} information respectively.
14-Sep-2016	6	Table 1: updated "RHFAC164245K1" with "RHRAC164245K1" and "RHFAC164245K01V" with "RHRAC164245K01V". Table 10: "Order codes": updated "RHFAC164245K1" with "RHRAC164245K1".
12-Jan-2017	7	Updated Section 1.1: "Cold spare" Updated Section 1.2: "Power-up" Table 4: "Absolute maximum ratings": updated VDD1/VDD2 value and updated footnote 1. Table 5: “Operating conditions”: added footnote 1
16-May-2017	8	Updated Section 1.2: "Power-up" and footnote 1 in Table 5: "Operating conditions".
31-May-2018	9	Updated Section 1.2 Power-up, Section 7 Ordering information. Updated Table 4. Operating conditions.
11-Dec-2018	10	Updated features and description in cover page. Updated Section 1.3 Pin connections, Section 4 Radiations, Table 9. Order code. Added Section 8 Other information.

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