bladeRF 2.0 **USB 3.0 Software Defined Radio**



The bladeRF is an off-the-shelf USB 3.0 Software Defined Radio (SDR) that is easy and affordable for students and RF enthusiasts to explore wireless communications, yet provides a powerful waveform development platform expected by industry professionals.

Support is available for Linux, macOS, and Windows. The bladeRF libraries, utilities, firmware, and platform HDL are released and under open source licenses, schematics are available online. The FPGA and USB 3.0 peripheral controller are programmable using vendor-supplied tools and SDKs that are available online, free of charge.



FEATURES

Analog Devices RF Transceiver

- 47 MHz to 6 GHz frequency range
- 2x2 MIMO, 61.44 MHz sampling rate
- 56 MHz filtered bandwidth (IBW)
- Automatic gain control (AGC)
- Real-time custom gain control tables controlled via SPI and discrete external input pins
- Automatic IQ and DC offset correction
- 128-tap digital FIR filtering

USB 3.0 SuperSpeed Support

- Cypress FX3 peripheral controller with integrated 200 MHz ARM926EJ-S processor
- Fully bus-powered over USB 3.0
- External power option via 5 V DC barrel jack with automatic switchover

Altera Cyclone V FPGA

49 kLE and 301 kLE variants available for custom signal processing and hardware accelerators

Factory-calibrated SiTime MEMS VCTCXO

- Calibrated within 1 Hz of 38.4 MHz
- Taming supported via 12-bit DAC or ADF4002 PLL
- MEMS oscillators provide superior reliability, aging, power supply noise rejection, and vibe/shock performance compared to guartz oscillators

Fully Customizable

- Expansion port with 32 I/O pins (LVDS available)
 - JTAG connectors
- Triggered multi-device sampling synchronization
- Onboard bias tee optionally provides 5 V to active antennas and accessories

SOFTWARE SUPPORT & APPLICATIONS

Supported by popular third-party software¹

- GNU Radio via gr-osmosdr
- Pothos via SoapvSDR
- SDRangel _
- SDR Console
- SDR# via sdrsharp-bladeRF
- YateBTS _
- OpenAirInterface
- srsUE & srsLTE _
- MathWorks MATLAB[®] & Simulink[®] support
- Python bindings

Applications

- Custom modem and waveform development
- Wireless video (e.g., ATSC, DVB-T, DVB-S)
- GPS reception and simulation
- Whitespace exploration
- GSM and LTE
- ADS-B reception and simulation

Operating Systems

- Linux
- Windows
- macOS

¹ Third-party software is copyrighted by the respective owners and/or contributors.

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USB 3.0 Software Defined Radio



MinTypMaxRF Specifications ADC/DAC Sample Rate 0.521^2 61.44 ADC/DAC Resolution 12 $VCTCXO$ Calibrated Accuracy ³ 26 VCTCXO Calibrated Accuracy ³ 26 6000 RF Tuning Range (RX) 70 6000 RF Tuning Range (TX) 47 6000 RF Bandwidth Filter <0.2 56 CW Output Power $+8$ FPGA Specifications U Logic Elements 49 301 Memory $3,383$ $13,917$ Variable-precision DSP Blocks 66 342 Embedded 18x18 Multipliers 132 684 Physical Specifications $6.3 \times 11.7 \times 1.8$		SPECIFICATIONS				
RF SpecificationsIADC/DAC Sample Rate 0.521^2 61.44 ADC/DAC Resolution12VCTCXO Calibrated Accuracy ³ 26RF Tuning Range (RX)70 6000 RF Tuning Range (TX)47 6000 RF Bandwidth Filter<0.256CW Output Power+8FPGA SpecificationsLogic Elements49 301 Memory $3,383$ $13,917$ Variable-precision DSP Blocks 66 342 Embedded 18x18 Multipliers 132 684 Physical Specifications $6.3 \times 11.7 \times 1.8$	Unit	Мах				
ADC/DAC Resolution12VCTCXO Calibrated Accuracy326RF Tuning Range (RX)70RF Tuning Range (TX)47RF Bandwidth Filter<0.2					RF Specifications	
VCTCXO Calibrated Accuracy ³ 26 RF Tuning Range (RX) 70 6000 RF Tuning Range (TX) 47 6000 RF Bandwidth Filter <0.2	MSPS	61.44		0.521 ²	ADC/DAC Sample Rate	
RF Tuning Range (RX) 70 6000 RF Tuning Range (TX) 47 6000 RF Bandwidth Filter <0.2	bits		12		ADC/DAC Resolution	
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RF Bandwidth Filter <0.2	MHz	6000		70	RF Tuning Range (RX)	
CW Output Power +8 FPGA Specifications	MHz	6000		47	RF Tuning Range (TX)	
FPGA Specifications Logic Elements 49 301 Memory 3,383 13,917 Variable-precision DSP Blocks 66 342 Embedded 18x18 Multipliers 132 684 Physical Specifications 6.3 x 11.7 x 1.8	MHz	56		<0.2	RF Bandwidth Filter	
Logic Elements 49 301 Memory 3,383 13,917 Variable-precision DSP Blocks 66 342 Embedded 18x18 Multipliers 132 684 Physical Specifications 6.3 x 11.7 x 1.8	dBm		+8		CW Output Power	
Memory 3,383 13,917 Variable-precision DSP Blocks 66 342 Embedded 18x18 Multipliers 132 684 Physical Specifications 6.3 x 11.7 x 1.8					FPGA Specifications	
Variable-precision DSP Blocks66342Embedded 18x18 Multipliers132684Physical Specifications6.3 x 11.7 x 1.8	kLE	301		49	Logic Elements	
Embedded 18x18 Multipliers 132 684 Physical Specifications 6.3 x 11.7 x 1.8	kbits	13,917		3,383	Memory	
Physical Specifications 6.3 x 11.7 x 1.8		342		66	Variable-precision DSP Blocks	
Dimensions 6.3 x 11.7 x 1.8		684		132	Embedded 18x18 Multipliers	
Dimensions					Physical Specifications	
	cm				Dimensions	
	inch		2.5 x 4.6 x 0.70			
Weight 56 (0.12)	g (lb.)		56 (0.12)		Weight	
Operating Temperature (A4/A9) 0 70	°C	70		0	Operating Temperature (A4/A9)	
Operating Temperature (A9 Thermal) -40 85	°C	85		-40	Operating Temperature (A9 Thermal)	

ACCESSORIES

CaseClear polyceBT-100WidebandBT-200Wideband

Clear polycarbonate case Wideband bias-tee powered Power Amplifier

Wideband bias-tee powered Low Noise Amplifier

² The minimum ADC sampling rate is 25 MSPS. 521 KSPS is achieved using the maximum decimation of 12 and an additional FIR decimation of 4. ³ VCTCXO is factory-calibrated to 1 Hz at 38.4 MHz. Temperature stability, aging, and other factors will affect accuracy after leaving the factory. All specifications are subject to change without notice.