

## Si5041 EVALUATION BOARD

### Description

The Si5041-EVB provides a platform for evaluating Silicon Laboratories' Si5041 XFP Signal Conditioning Transceiver. The Si5041 is a complete, low-power, high-performance XFP transceiver suitable for use in all XFP module types, from short-reach datacom to long-reach telecom applications. The Si5041 is unique in that it integrates a rate-agile, jitter-attenuating transmit CMU and receive CMU. The device supports referenceless operation or may use a reference clock for LOL detection. The device can be completely configured through a serial microcontroller interface. The Si5041 Transceiver provides full-duplex operation at serial data rates from 9.95 to 11.35 Gbps (continuous).

The Si5041-EVB also contains an MCU (C8051F320) and a crystal oscillator (Si534), both from Silicon Labs. The 8051F320 provides status and control communication between the Si5041 and the Si5041-EVB Software. The Si534 is a multi-rate crystal oscillator that, when enabled, supplies one of four selectable reference clocks to the Si5041 while providing that clock at SMA connectors for external monitoring/use.

The Silicon Laboratories MCU (C8051F320) has a USB port that is used to communicate to a PC that is running the Si5041 EVB software. The MCU also has a serial port that connects to the serial control port of the Si5041 to read and write to its registers. In addition, the MCU drives all but one of the LEDs on the EVB and can make a very accurate reading of the three voltages that power the EVB.

### Features

The Si5041-EVB includes the following:

- Evaluation of Silicon Laboratories' Si5041 XFP Signal Conditioning Transceiver
- Separate supply connections for the following:
  - $V_{DD}$  (1.8 V) powers the internal circuitry of the Si5041.
  - $V_{DD\_3p3}$  (3.3 V) powers the MCU and XTAL oscillator.
  - $V_{DDIO}$  (1.8 or 3.3 V) powers the LVTTTL IOs of the Si5041.
- Four selectable on-chip reference frequencies.
- LEDs for visual monitoring of key chip and board parameters.
- Si5041 EVB software allows for quick and easy access to all registers in the Si5041.
- A dual-row header allows the Si5041 to be easily connected to another MCU for serial control and status communications.
- Synchronous output clock at 1/64 the recovered clock rate.

### Si5041-EVB Quick Start

To set up the Si5041-EVB, perform the following steps:

1. Install the Si504x EVB Software. (Assumes that Microsoft .NET Framework 1.1 is already installed.)
2. Allow the software installer to also install the Si504x EVB Driver. (This must be installed before the EVB is connected to the PC via the USB cable.)
3. Connect the power supplies to the EVB.
4. Turn on the power supplies.
5. Connect a USB cable from the EVB to the PC where the software was installed. Launch the software by clicking on **Start→Programs→Silicon Laboratories→Si504x EVB Software** and selecting one of the programs to run.
6. If prompted, pick a serial number corresponding to the desired EVB to control.

7. The device should now be functioning with the CMUs in referenceless mode. That is, the RX and TX CMUs clean up the recovered clock from the CDR without the aid of any external reference clock or crystal. In addition, the device will automatically detect an external reference clock for CDR acquisition. If an external reference clock is not provided, the CDR acquisition will be in referenceless mode as well.
8. Next, open System Programmer. Under System Programmer, there is a block diagram of the device, and under the "Alarms and Interrupts" tab, are all the alarms you need for the evaluation.

## 1. Functional Description

The Si5041-EVB and software allow for a complete and simple evaluation of the functions, features, and performance of the Si5041 transceiver.

### 1.1. Input Power

This evaluation board requires three power inputs, +1.8 V, +3.3 V, and  $V_{DDIO}$  (1.8 V or 3.3 V), as well as a ground connection. J8 and J9 are used for connecting power to the EVB (see Figure 1).

### 1.2. LEDs

Three LEDs indicate that power has been properly applied to the EVB. These are +3.3 V,  $V_{DDIO}$ , and +1.8 V. Since these LEDs are driven by the MCU (not the power itself), the  $V_{DDIO}$  and +1.8 V LEDs will not function unless +3.3 V is first applied to the EVB (see Figure 1).

The 3.3 V LED will be on solid when the 3.3 V input is within the 2.97 to 3.63 V range. The 1.8 V LED will be on solid when the 1.8 V at the Si5041  $V_{DD}$  pins is within the 1.62 to 1.89 V range.

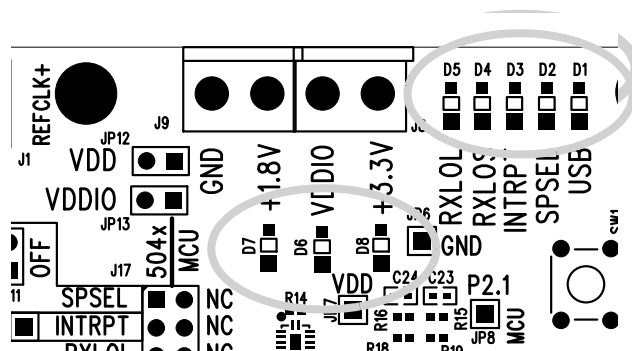
The  $V_{DDIO}$  LED will be on solid when this input voltage is between 1.89 and 3.63 V. The  $V_{DDIO}$  LED will flash on and off when this voltage is between 1.62 and 1.89 V.

The REF ON LED indicates that the Si534 clock reference chip is powered up and applying a clock signal to the Si5041. JP16 must be set to the ON position in order to power up the Si534.

**Table 1. LED Status and Description**

LED	Status	Description
3.3 V	ON	When 3.3 V supply is between 2.97 and 3.63 V.
1.8 V	ON	When Si5041 $V_{DD}$ pins are between 1.62 and 1.89 V.
$V_{DDIO}$	ON	When Si5041 $V_{DDIO}$ pin is between 1.89 and 3.63 V.
	FLASHING	When Si5041 $V_{DDIO}$ pin is between 1.62 and 1.89 V.
REF ON	ON	When the Reference clock source Si534 is powered up.
USB	ON	Flashes when USB Access is occurring.
SPSEL	ON	When the Si5041 SPSEL pin is high.
INTRPT	ON	When the Si5041 INTRPT pin is high.
RXLOS	ON	When the Si5041 RXLOS pin is high.
RXL0L	ON	When the Si5041 RXL0L pin is high.

Since the 1.8 V LED indicates the voltage at the Si5041  $V_{DD}$  pins, the jumper, JP12, must be in place for this LED to function and for the Si5041 to receive its core supply voltage. However, the  $V_{DDIO}$  LED will function without the jumper on JP13.

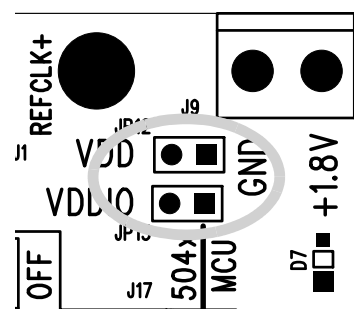


**Figure 1. LEDs**

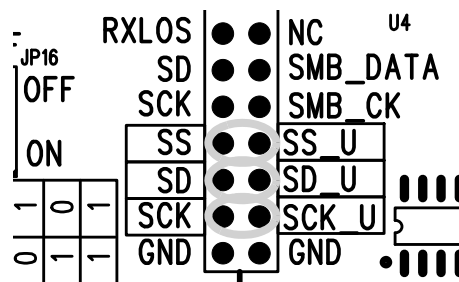
### 1.3. Jumpers and Headers

**For the EVB to function, there are five jumpers that must be installed.**

There must be jumpers on JP12 and JP13 because they apply power to the Si5041 (see Figure 2). The next three required jumpers are three positions on J17, labeled SS, SD, and SCK on one side and SS\_U, SD\_U, and SCK\_U on the other side (see Figure 3). Connecting jumpers between SS to SS\_U, SD to SD\_U, and SCK to SCK\_U enables the onboard MCU to communicate with the Si5041 using the 3-wire serial interface.



**Figure 2. JP12 and JP13**



**Figure 3. J17**

## 1.3.1. MCU to Si5041 Serial Communications (Status and Control)

The microcode within the MCU is designed to communicate with the Si5041 when SPSEL pin 9 is high (JP11 no jumper). In this mode, the serial data transfer from the MCU to the Si5041 is very similar to the SPI protocol but with a single bidirectional data line rather than two unidirectional data lines. However, one could write new microcode for the MCU that uses the SMBus (I<sup>2</sup>C compatible) to communicate with the Si5041. To enable SMBus communication between the Si5041 and the MCU, you must install a jumper on JP11 and on J17 between SD/SMB\_DAT, SCK/SMB\_CK and SS/SS\_U. See Figure 4. Note that INTRPT on JP17 should be labeled as INTRPTB because the interrupt from the Si5041 is an active low signal.

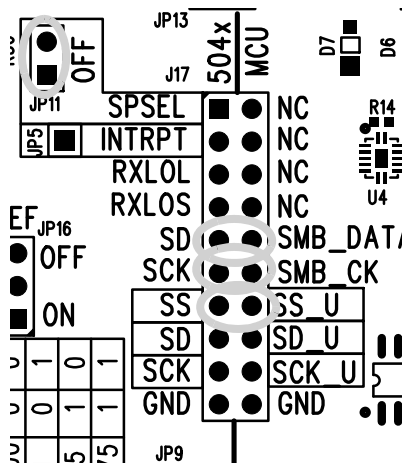


Figure 4. SMBus Protocol

## 1.3.2. External MCU Control

To use an external MCU, make sure that all jumpers are removed from J17 and that JP11 does not have a jumper (see Figure 5). Now, the following pins of J17 are available for connection to an external MCU.

- SCK
- SD
- SS
- RXLOS
- RXLOL
- INTRPT
- SPSEL
- GND

The Silicon Labs MCU that is well-suited for use within XFP Modules is the C8051F330.

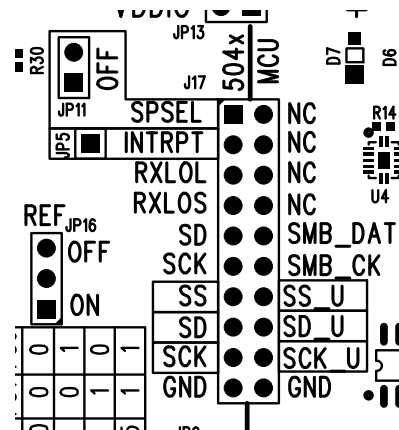


Figure 5. External MCU

## 1.3.3. Reference Clock

To use the on-chip reference clock (Si534), JP16 must be set to the ON position. When this is done, the REF ON LED will light, indicating that power is applied to the Si534. The output frequency of the Si534 is controlled by jumpers JP17 and JP18 (see Figure 6).

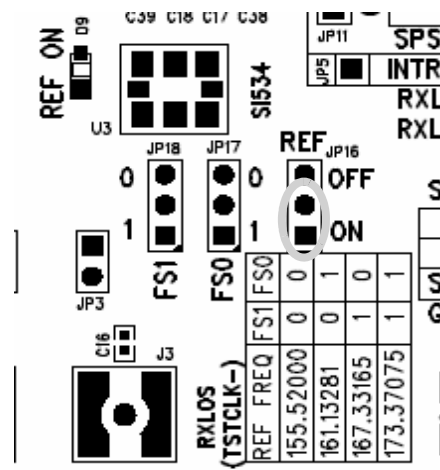
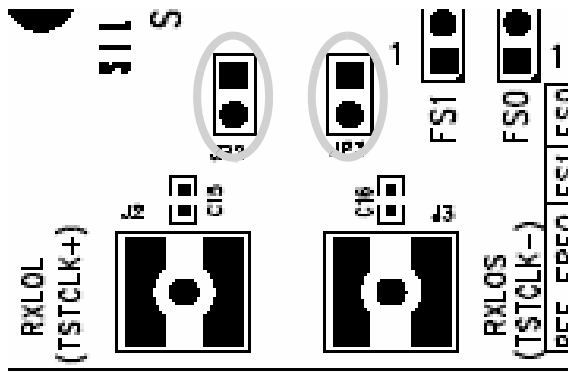


Figure 6. Reference Clock

## 1.3.4. Synchronous Test Clock

By setting Register 57 to 9Ch, the Tx CMU clock divided by 64 will be output at J2 and J3. The EVB must have jumpers on JP2 and JP3 to enable the /64 clock output (see Figure 7). By setting Register 57 to 1Ch, the Rx CMU clock divided by 64 will be output at J2 and J3. When jumpers are placed on JP2 and JP3, the functionality of RXLOS and RXLOL is lost, and the state of the LEDs for these two signals becomes invalid. To return the RXLOL and RXLOS signals to their normal modes, set Register 57 to 00h, and remove the jumpers on JP2 and JP3. Register 57 cannot be changed with the System Programmer GUI, you must use the Register Programmer GUI (see page 8).



**Figure 7. Synchronous Test Clock**

## 1.4. Reference Clock Details

The Si5041 can function without a reference clock and meet all system jitter generation and jitter tolerance specifications. However, the presence of a reference clock provides the following capabilities:

- Ability to measure the frequency error of the input data and generate a Loss-of-Lock indication if the frequency error exceeds 1000 ppm with respect to the reference clock.
- Only acquire lock if the input data is within 200 ppm.

A reference clock to the Si5041 can be input from an external source, or it can be generated from the onboard Si534. Since the clock from the Si534 is linearly summed with the external reference clock input, care must be taken to ensure that both clock sources are not active at the same time. When the Si534 is enabled (JP16 on), its output will be present at SMAs J1 and J5 for monitoring and/or system usage. When the Si534 is OFF, a differential clock applied at J1 and J5 will be attenuated by 2.7 dB before it reaches the REFCLK± inputs of the Si5041.

While an Si534 has the capability of generating any four frequencies between 10 MHz and 1400 MHz, this Si534 has been programmed to generate four specific frequencies. Jumpers JP17 and JP18 control the FS[1:0] inputs to the Si534 (see Figure 6). The four frequencies are as follows:

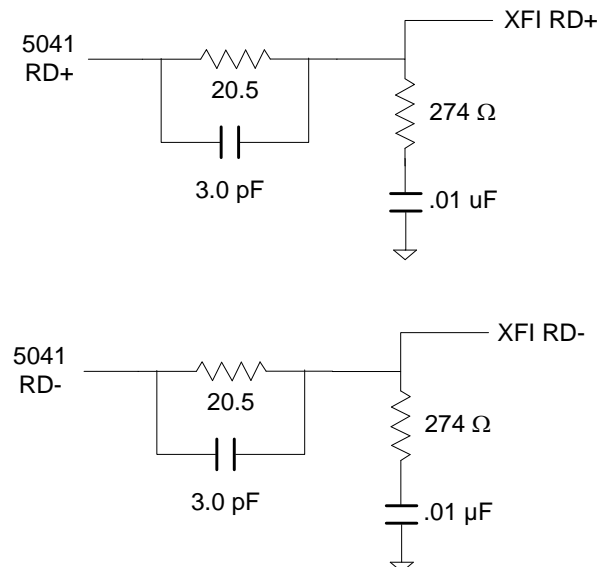
- 155.52000 MHz Set FS[1:0] = 00  
This is 1/64 of the SONET OC-192 rate of 9.95328e9 bps
- 161.13281 MHz Set FS[1:0] = 01  
This is 1/64 of the 10 GIGE LAN PHY rate of 10.3125e9 bps

- 167.33165 MHz Set FS[1:0] = 10  
This is 1/64 of the SONET OC-192 rate with 255/237 FEC overhead (10.709225e9 bps)
- 173.37075 MHz Set FS[1:0] = 11  
This is 1/64 of the 10 GIGE LAN Phy rate with 255/237 FEC overhead (11.095727e9 bps)

While the Si534 output is clean enough to meet the XFP requirements for the "optional clean reference clock", the Si5040 does not support this function. Please look at the Si5041 if you desire this function.

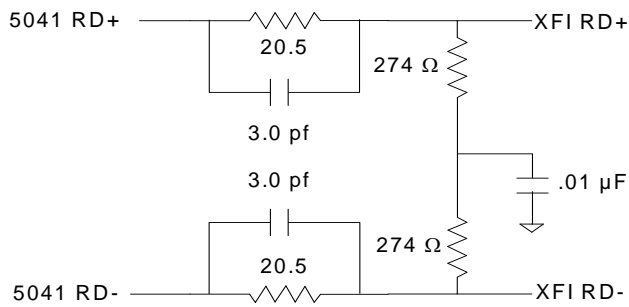
## 1.5. RD De-Emphasis

Even though the output data at the Si5041 RD pins has very fast transitions, we have found that some customers prefer some signal shaping of the RD output signal at the XFI. Therefore, the Si5041 EVB has a de-emphasis circuit added to the RD± outputs that is not shown in the schematic of Figure 10. This circuit is composed of a few resistors and capacitors, all of which can be generic, low-cost units. Because it is a passive circuit, it slightly attenuates the RD signal, which requires that the RD signal level from the Si5041 be slightly increased. Please use the Si5041 Register 56 to increase the RD drive signal from its default value of 600 mV to 800 mV. See the Si5041 data sheet for more information. The circuit that is implemented on the EVB is shown below:



**Figure 8. EVB De-Emphasis Circuit**

Within an XFP module, the pre-emphasis circuit should be located as close to the Si5041 RD± pins as is practical. In an XFP module, the pre-emphasis circuit above can be modified to remove one component yet still behave the same electrically. The following circuit shows this simplification.



**Figure 9. Recommended XFP Pre-Emphasis Circuit**

Should you not like the eye pattern at the RD± pins, this circuit can be easily optimized for your application. If you wish assistance in this matter, please contact Silicon Laboratories.

## 1.6. Start Up Script(s)

Upon selecting the EVB or doing a reset, the Si504X EVB System Programmer will automatically load a script that:

1. Increases the RD output to 800 mV to compensate for the loss of the RD de-emphasis network described in the previous section.
2. Holds the PLL in lock with higher jitter on the input signal. See AN345D section 4.
3. Sets the Interrupt output pin to CMOS mode.

The 504X Register Programmer will not automatically load scripts.

## 2. EVB Software Installation

The following sections describe how to install the EVB software.

### 2.1. PC System Requirements

- Microsoft Windows 2000, XP, or Vista
- USB 2.0
- 2 MB of hard drive space
- 1024x768 screen resolution or greater
- Microsoft .NET Framework 1.1
- Si504x EVB Driver (based on USBXpress 3.1.1)

**Note:** The Si504x EVB Driver is provided with the software installation files.

### 2.2. Microsoft .NET Framework Installation

The Microsoft .NET Framework is required before installing and running the Si504x EVB Software. Details and installation information about the .NET Framework are available via a shortcut in the NETFramework directory or at the following web site:

<http://www.microsoft.com/downloads/details.aspx?FamilyId=262D25E3-F589-4842-8157-034D1E7CF3A3&displaylang=en>

Contact your system administrator for more details.

### 2.3. Si5041 EVB Software Installation

To install:

1. Navigate to the install directory.
2. Double-click the install .exe file.
3. Follow the steps in the wizard to install the program.
4. After the installation is complete, click on Start > Programs > Silicon Laboratories > Si504x EVB Software. Select one of the programs to control the EVB.

5. See the online help available in one of the programs via the Help menu option.

To uninstall:

**Note:** Close all the Si504x EVB Software before running the uninstaller to ensure complete removal of the software.

The driver software must be uninstalled separately. See the next section for details.

To uninstall the software, use the Add and Remove Programs utility in the Control Panel. Select Si504x EVB Software from the list, or double-click on the Uninstal.exe file in the Si504x EVB Software directory, where the software is installed originally.

### 2.4. Si504x EVB Driver

**Note:** The Si504x EVB Driver must be installed on computers that were running the driver from the Si5041 EVB Software version 2.3 or older. This newer driver is required to run with the software version 4.0 and newer.

The driver is installed after the EVB software is installed. If this option is cancelled then the EVB will not run with the computer via USB.

The installer will copy the necessary driver files and update the operating system. However, for every different EVB connected to the same computer, the hardware installation wizard will run to associate this driver with the new EVB. Let the wizard run with its default settings.

The Si504x EVB driver may be removed via the Add and Remove Programs utility in the Control Panel. Locate the entry called Silicon Laboratories Si504x EVB Driver. Click the button and it should show the version and location of what it will remove.

The driver installation files are located with the installed Si504x EVB Software files. The driver files for the EVB may be re-installed from this location or by running the

## 2.5. Si504x EVB Software Description

There are three programs to control the Si5041. Each provides a different kind of access to the device. Refer to the online help in each program by clicking **Help→Help** in the menu for more information on how to use the software.

Program	Description
Register Viewer	The Register Viewer displays the current data in a table format sorted by register address of the Si5041 register map to provide a quick view of the Si5041's state. This program can save and print the register map.
Register Programmer	The Register Programmer provides low-level register control of the Si5041. Single and batch operations are provided to read from and write to the device. Register map files can be saved and opened in the batch mode.
System Programmer	The System Programmer provides high-level control of the Si5041. There are multiple settings for this chip; so, this program will make it easier to configure these settings. (The settings this program can control are documented in the Si5041 data sheet.) The software can also save and open the register data in a text file format.



### 3. Typical Application Schematics

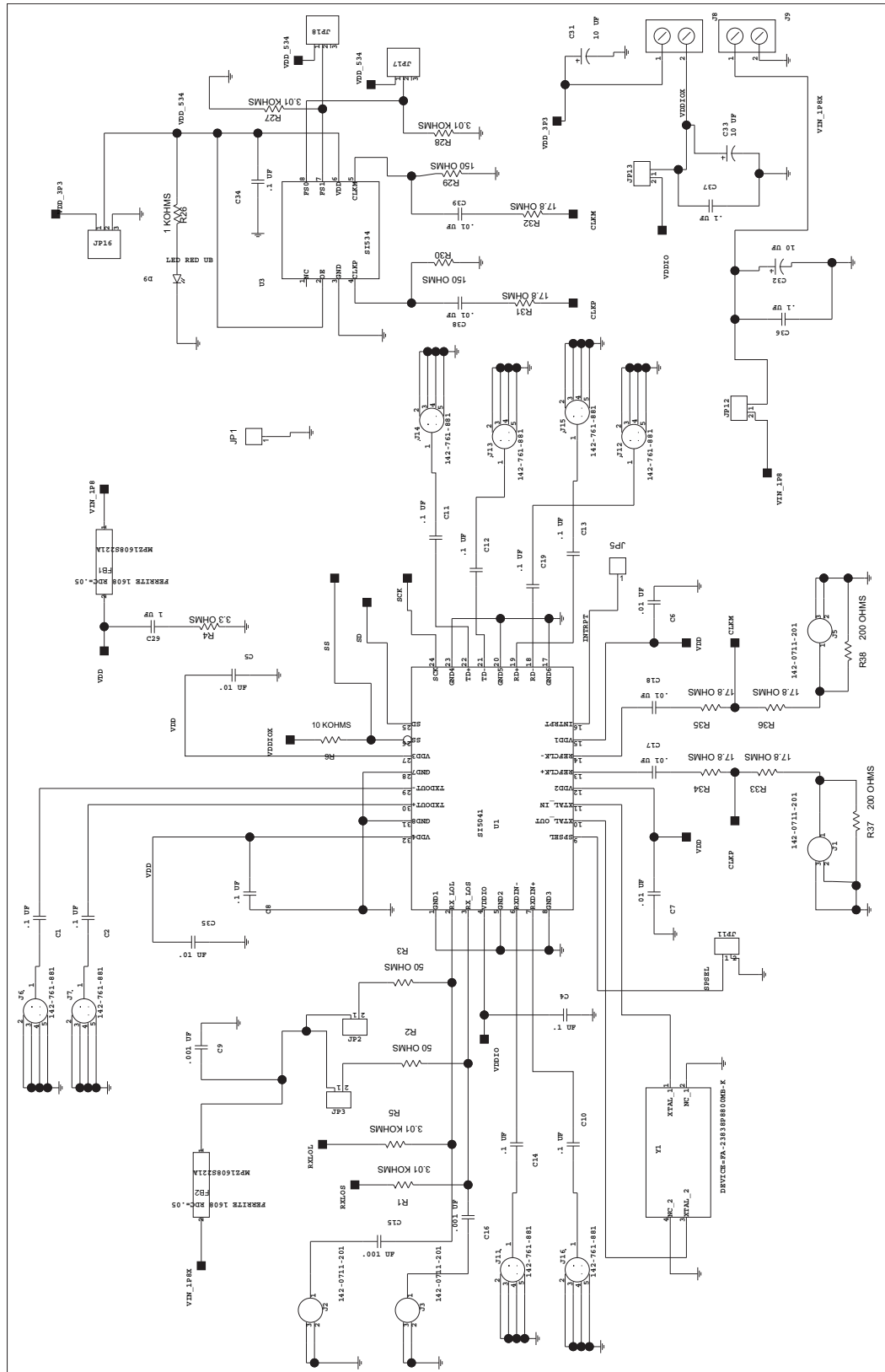


Figure 10. Application Schematic (Page 1)

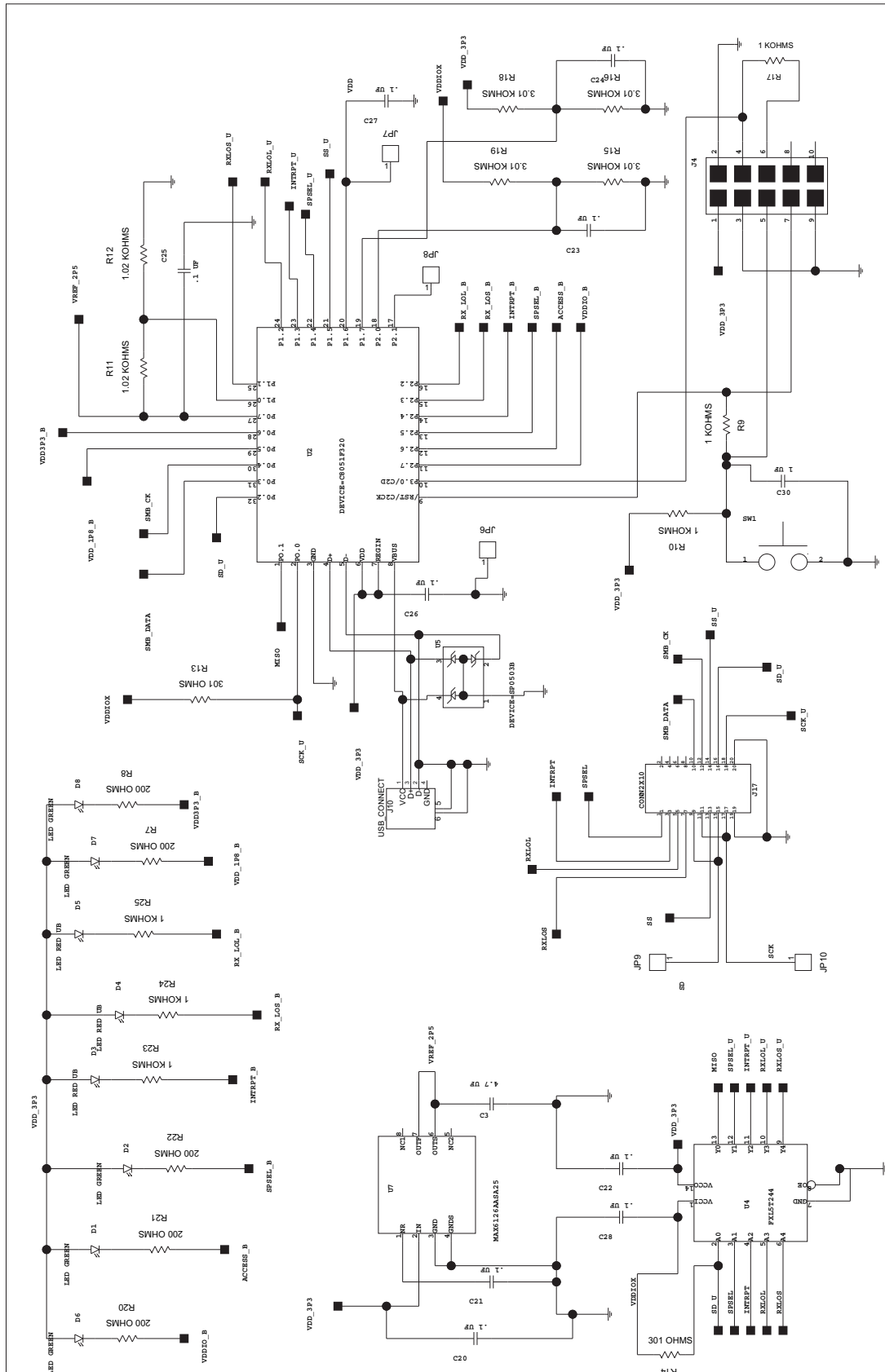


Figure 11. Application Schematic (Page 2)

#### 4. Bill of Materials

**Table 2. Si5041-EVB Bill of Materials**

Item	Qty	Reference	Description	Manufacturer Number	Manufacturer
1	8	C1,C2,C10, C11,C12	CAP, SM, 0.1 $\mu$ F, 10 V, 10%, X7R,0402	540L105KW10820T	ATC
		C13,C14,C19			
2	14	C4,C8,C20, C21,C22,C23, C24,C25,C26, C27,C28,C34, C36,C37,	CAP, SM, 0.1 $\mu$ F, 16 V, 10%, X7R,0402	C0402X7R160-104KNE	Venkel
3	7	C5,C6,C7, C17,C18, C38,C39	CAP, SM, 0.01 $\mu$ F, 25 V, X7R,0402	C0402X7R250-103KNE	Venkel
4	1	C3	CAP, SM, 4.7 $\mu$ F, 6.3 V, X7R,0805	CEJMK212BJ475KG-T	Taiyo Yuden
5	3	C9,C15,C16	CAP, SM, 1000 pF, 50 V, 5%, C0G,0402	C0402C0G500-102JNE	Venkel
6	2	C29,C30	CAP, SM, 1 $\mu$ F, 6.3 V, X7R, 0603	C0603X7R6R3-105KNE	Venkel
7	3	C31,C32,C33	CAP, SM, 10 $\mu$ F, 10 V, X7R, 1206	C1206X7R100-106KNE	Venkel
8	5	D1,D2,D6, D7,D8	LED, SM, LN1371G, GREEN	LN1371G	Panasonic
9	4	D3,D4,D5,D9	LED, SM, LN1271, BRIGHT RED	LN1271RAL-TR	Panasonic
10	2	FB1,FB2	FERRITE, SM, 165 $\Omega$ , 2000 mA	MPZ1608S221A	TDK
11	4	J1,J2,J3,J5	CONN, SMA, SM, VERT	142-0711-201	Johnson Components
12	1	J4	CONN, HEADER, 5x2	103309-1	AMP
13	8	J6,J7,J11,J12, J13,J14,J15, J16	CONN, SMA, COPLANAR	142-0761-801	Johnson Components
14	2	J8,J9	CONN, POWER, 2 POSITION	1729018	Phoenix Contact
15	1	J10	CONN, USB, B, RECEPT	897-30-004-90-000000	MILL-MAX
16	1	J17	CONN, HEADER, 10X2	2340-6111TN or 2380-6121TN	3M
17	7	JP1,JP5,JP6, JP7,JP8,JP9, JP10	CONN, HEADER, 1X1	2340-6111TN or 2380-6121TN	3M
18	5	JP2,JP3,JP11, JP12,JP13	CONN, HEADER, 2x1	2340-6111TN or 2380-6121TN	3M
19	3	JP16,JP17, JP18	CONN, HEADER, 3x1	2340-6111TN or 2380-6121TN	3M
20	8	R1,R5,R15, R16,R18,R19, R27,R28	RES, SM, 3.01 k $\Omega$ , 1%, 0402	CR0402-16W-3011FT	Venkel

# Si5041-EVB

**Table 2. Si5041-EVB Bill of Materials (Continued)**

Item	Qty	Reference	Description	Manufacturer Number	Manufacturer
21	2	R2,R3	RES, SM, 49.9 $\Omega$ , 1%, 0402	CR0402-16W-49R9FT	Venkel
22	1	R4	RES, SM, 3.3 $\Omega$ , 5%, 0402	CR0402-16W-3R3JT	Venkel
23	1	R6	RES, SM, 10 k $\Omega$ , 1%, 0402	CR0402-16W-1002FT	Venkel
24	7	R7,R8,R20, R21,R22,R37, R38	RES, SM, 200 $\Omega$ , 1%, 0402	CR0402-16W-2000FT	Venkel
25	7	R9,R10,R17, R23,R24,	RES, SM, 1 k $\Omega$ , 1%, 0402	CR0402-16W-1001FT	Venkel
		R25,R26			
26	2	R11,R12	RES, SM, 1.02 k $\Omega$ , 0.1%, 0402	TFCR0402-16W-E-1021BT	Venkel
27	2	R13,R14	RES, SM, 301, 1%, 0402	CR0402-16W-3010FT	Venkel
28	2	R29,R30	RES, SM, 150, 1%, 0402	CR0402-16W-1500FT	Venkel
29	6	R31,R32,R33, R34,R35,R36	RES, SM, 17.8, 1%, 0402	CR0402-16W-17R8FT	Venkel
30	1	SW1	SWITCH, PUSH BUTTON, MINIATURE	EVQPAD04M	Panasonic
31	1	U1	IC, SM, Si5041	Si5041	Silicon Laboratories
32	1	U2	IC, SM, MCU, 32 POS, QFN	C8051F320	Silicon Laboratories
33	1	U3	IC, Si534	534AB000129BG	Silicon Laboratories
34	1	U4	IC, SM, VOLTAGE-SUPPLY TRANSLATOR, 14 PIN DQFN	FXL5T244BQX	Fairchild
35	1	U5	IC, SM, DIODE ARRAY, 6 POS, SOT143	SP0503BAHT	Littlefuse
36	1	U7	IC, SM, VOLTAGE REFERENCE, 8-PIN SOIC	MAX6126AASA25	Maxim
37	1	Y1	CRYSTAL, SM, 114.285 MHz	7BA, 114.285 MHZ	TXC
<b>No Load</b>					
38	1	C35	CAP, SM, 0.01 $\mu$ F, 25 V, X7R, 0402	C0402X7R250-103KNE	Venkel

## 5. Layers

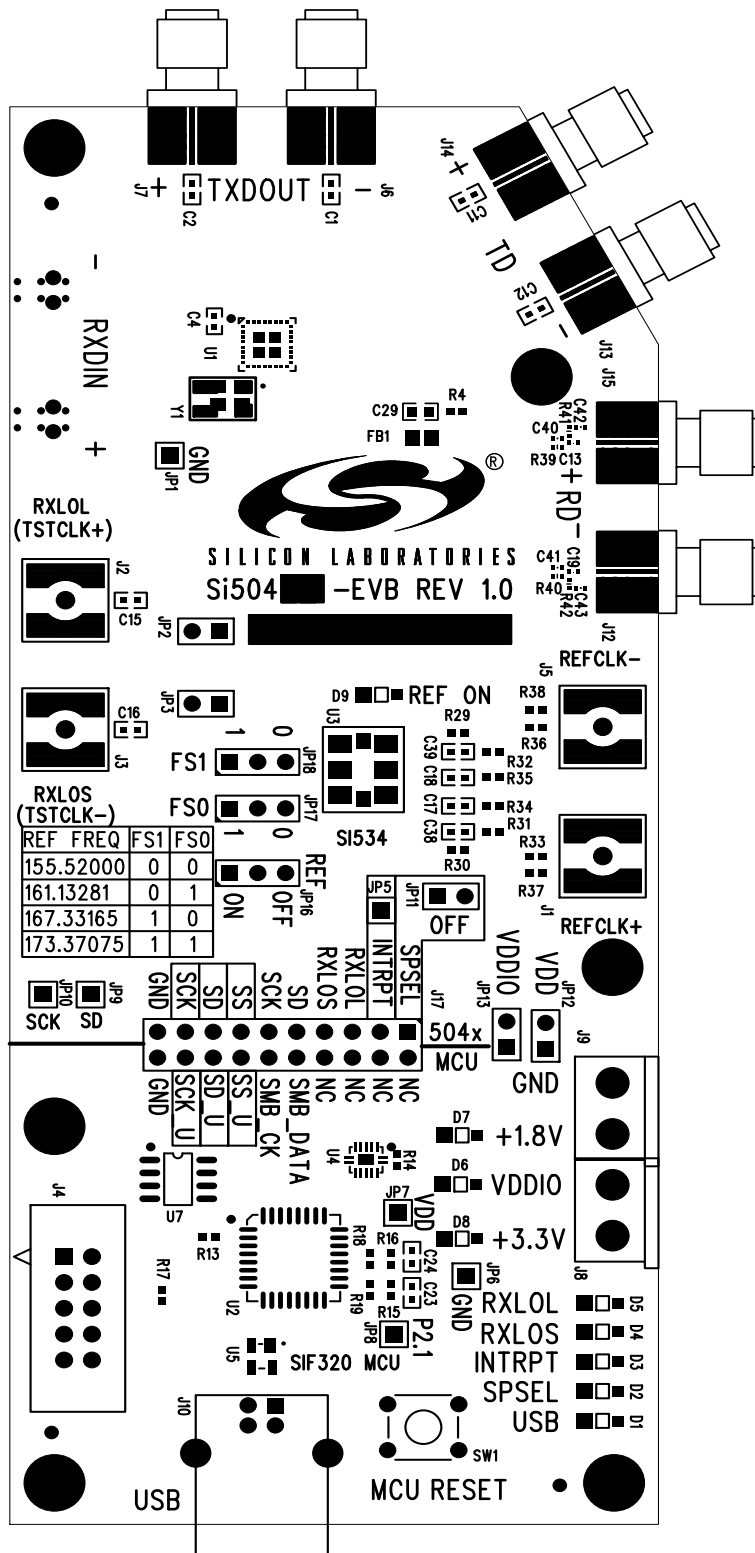


Figure 12. Si5041-EVB Top Silkscreen

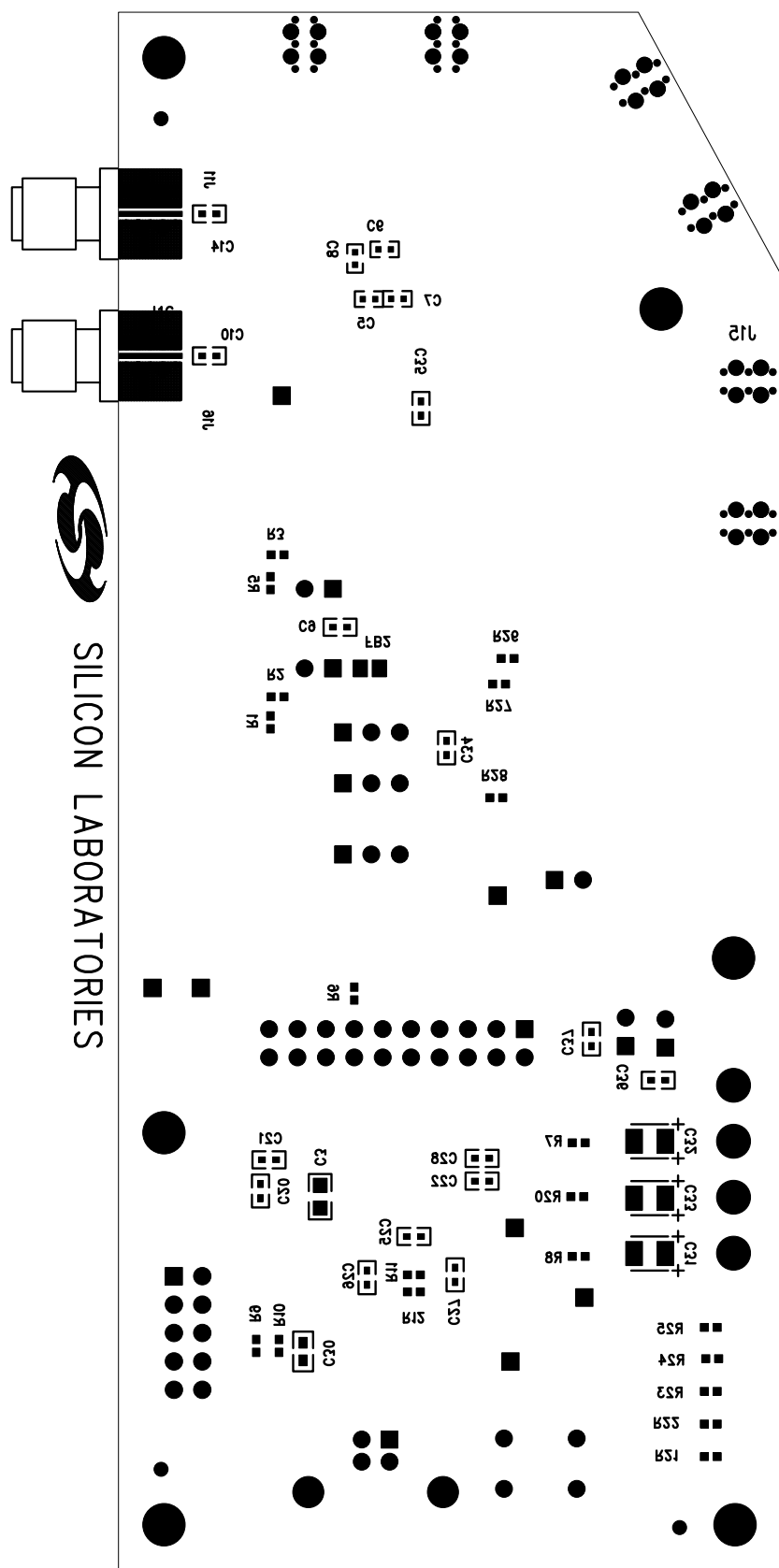


Figure 13. Si5041-EVB Bottom Silkscreen

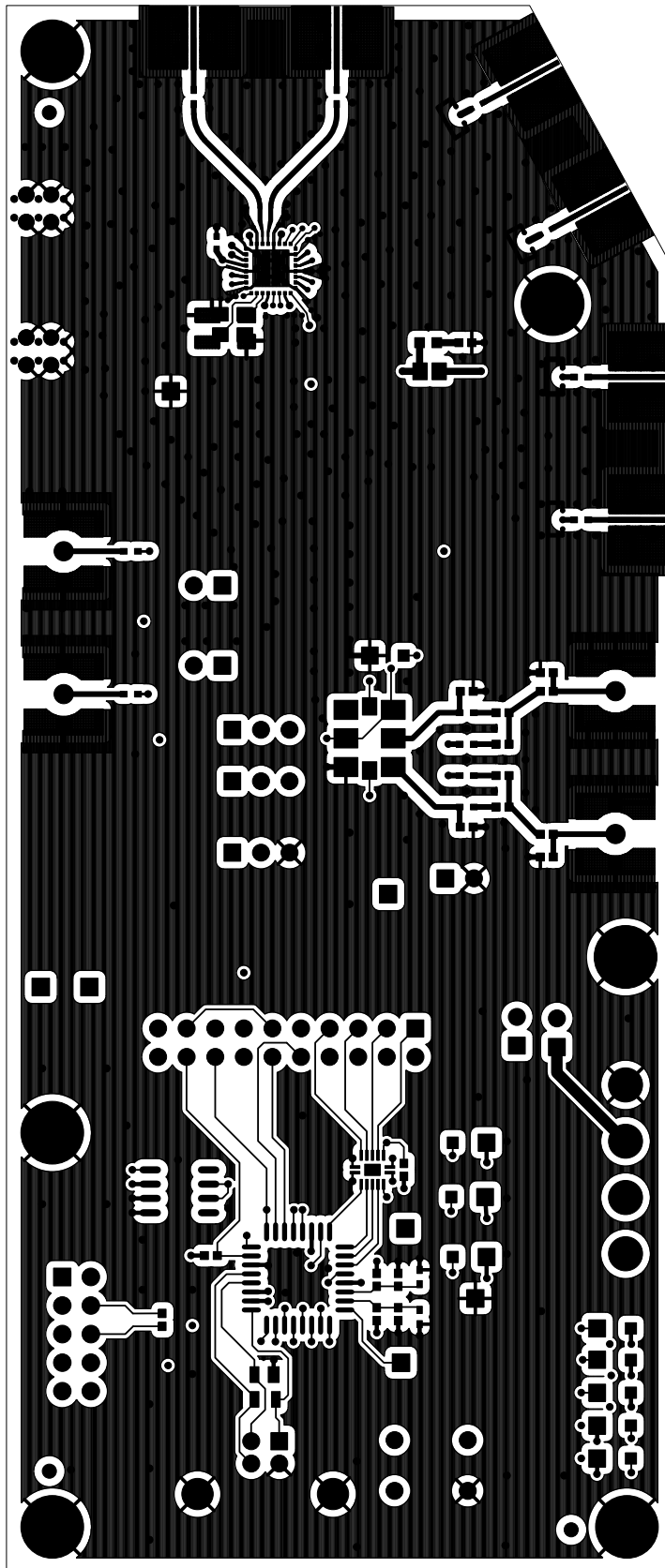


Figure 14. Primary Component Side

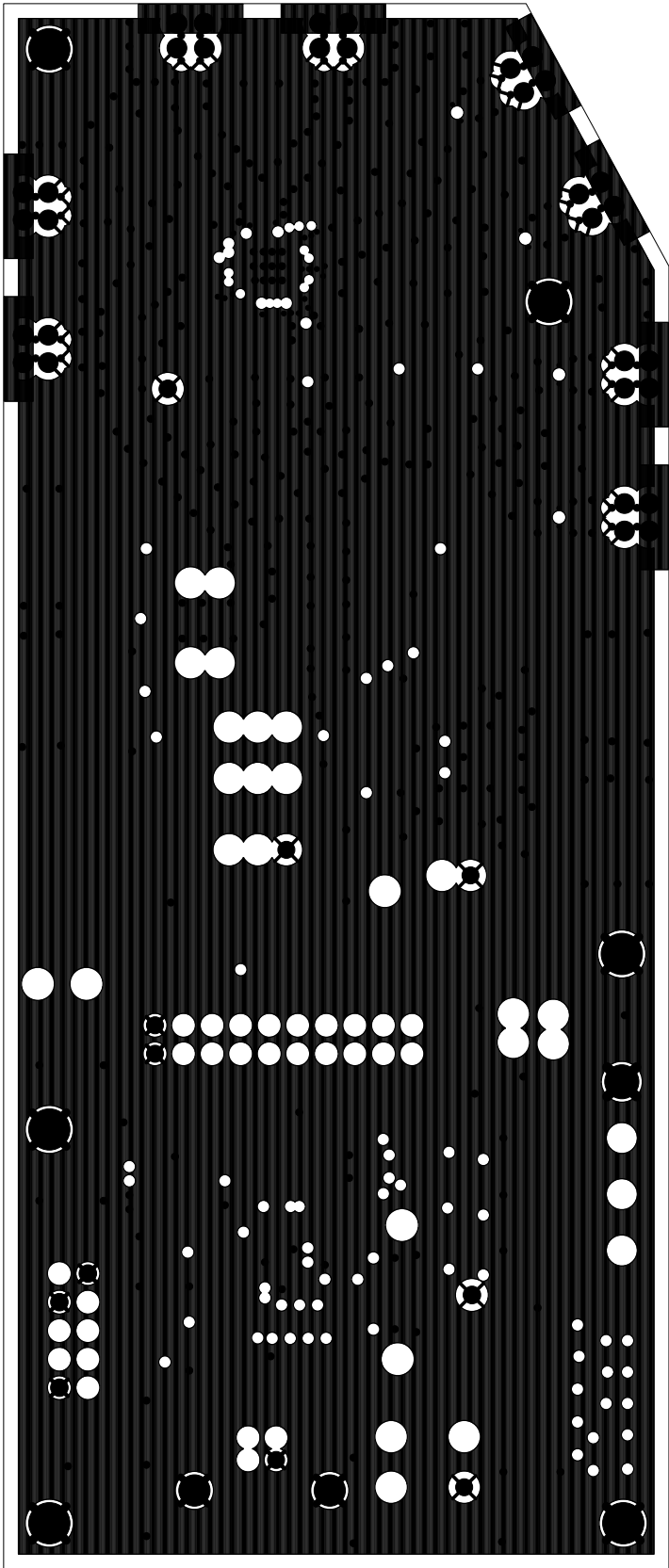


Figure 15. Plane 1 (GND)



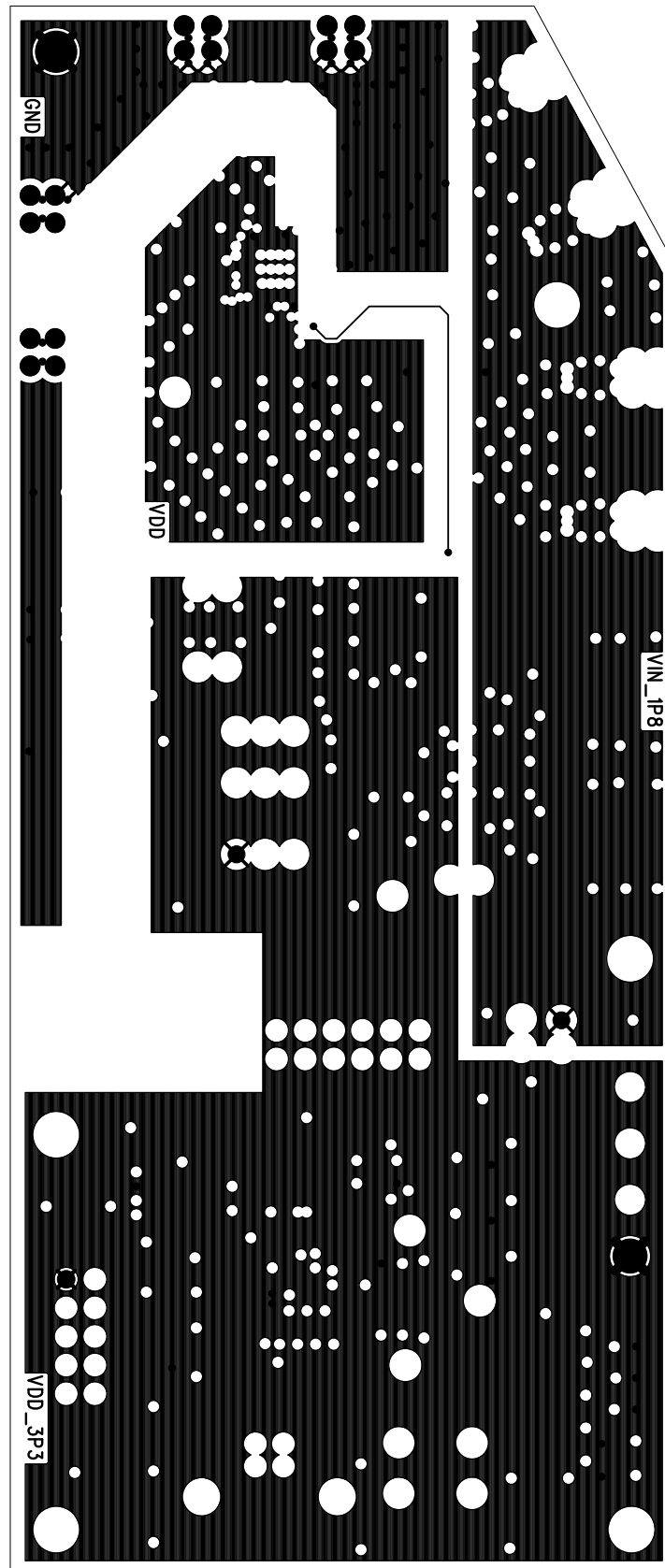


Figure 16. Plane 2 (PWR)

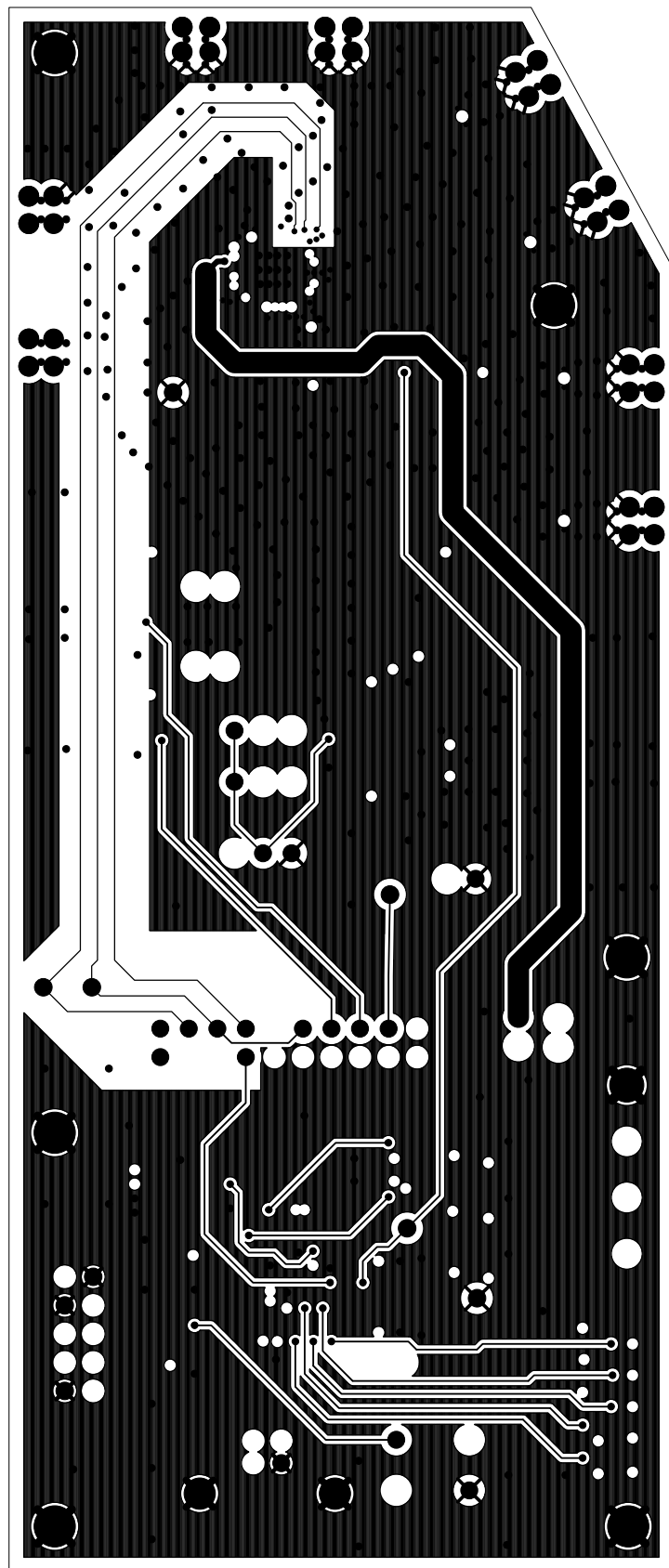


Figure 17. Signal 1

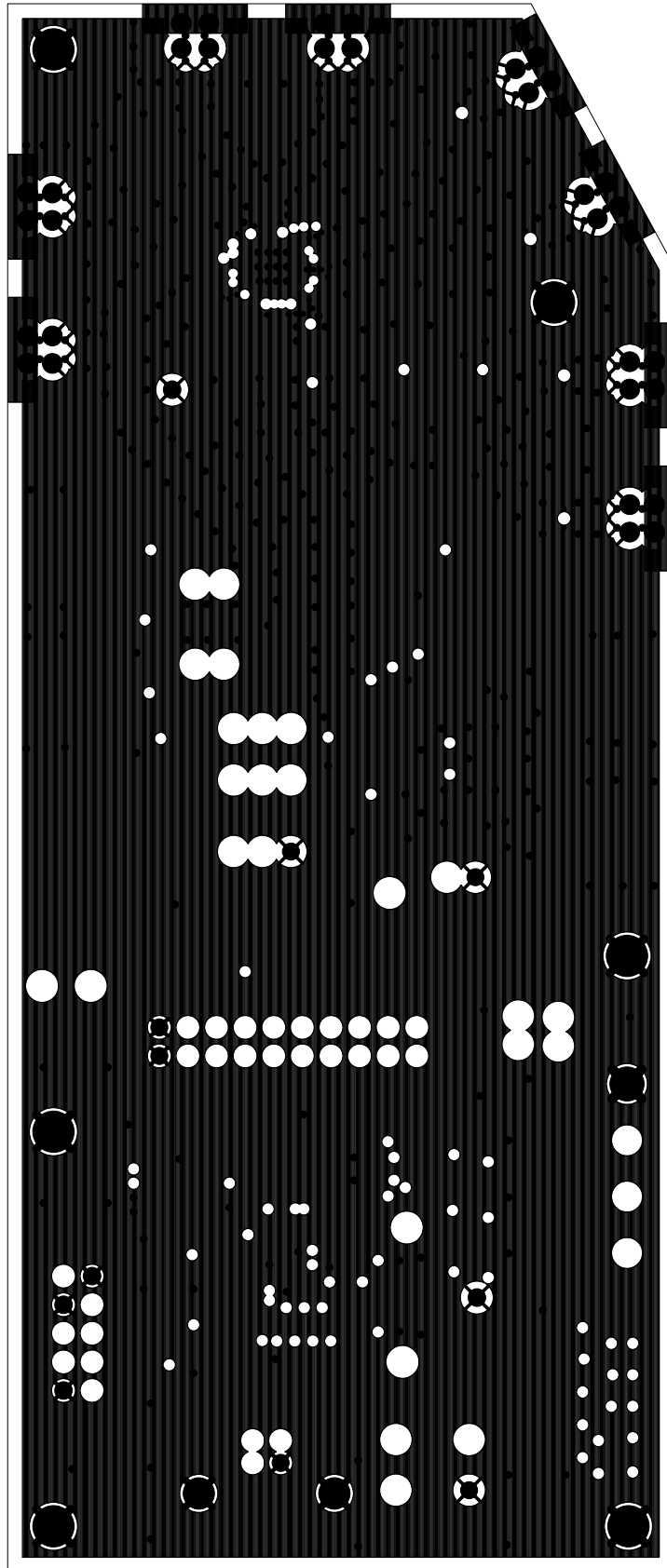


Figure 18. Plane 3 (GND)

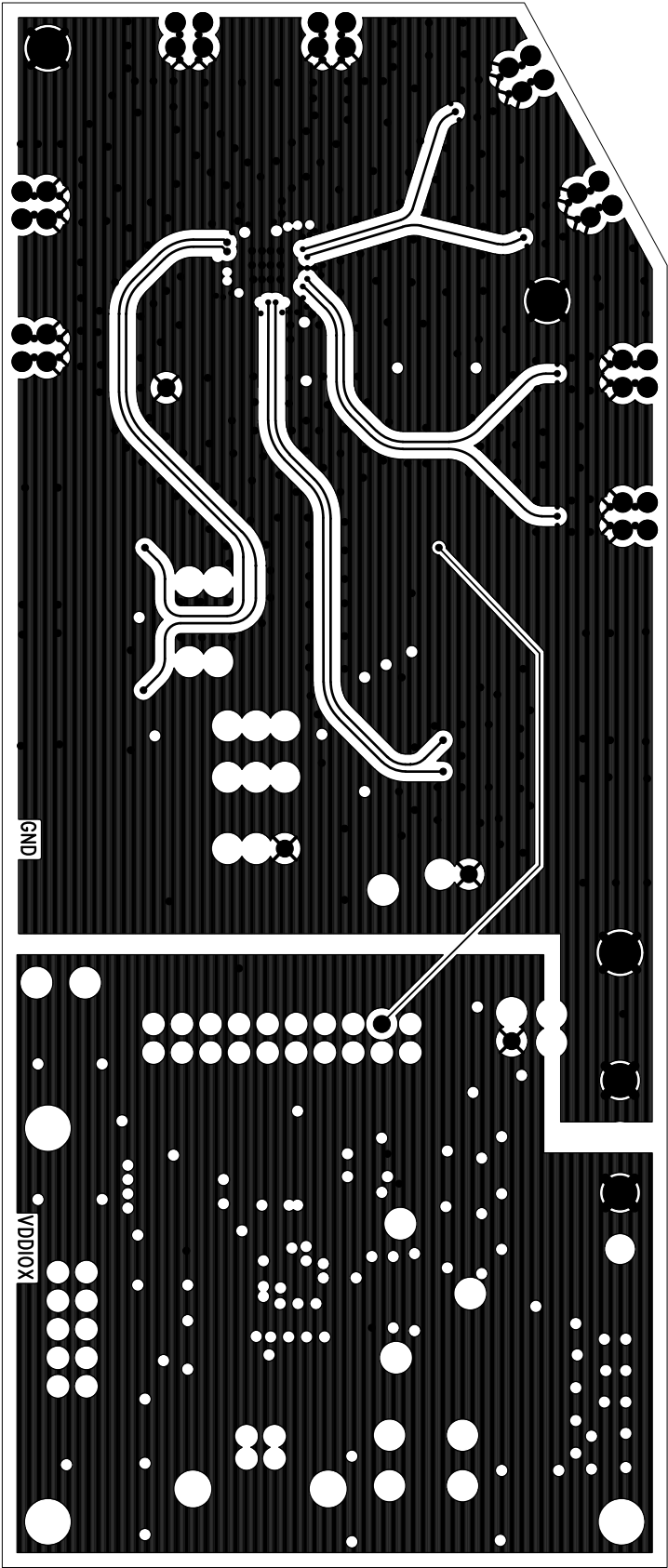


Figure 19. Signal 2

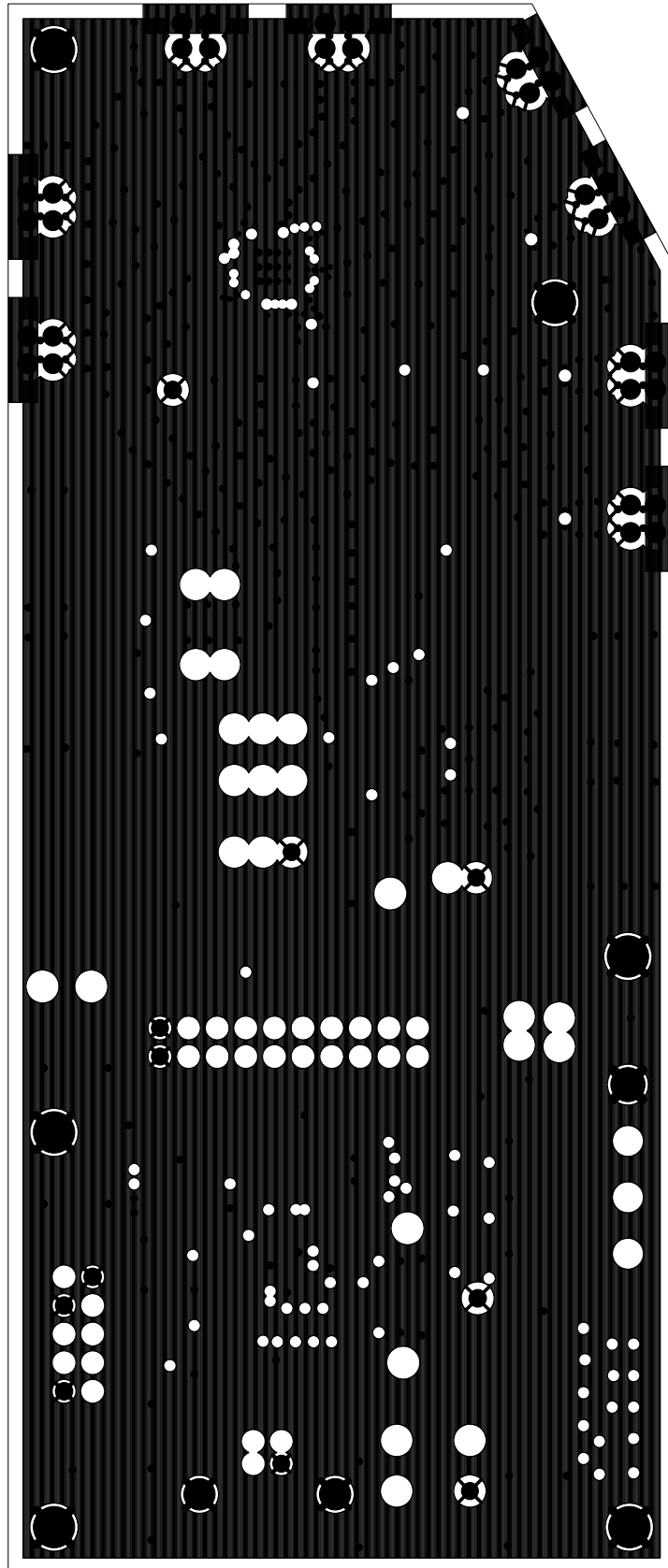


Figure 20. Plane 4 (GND)

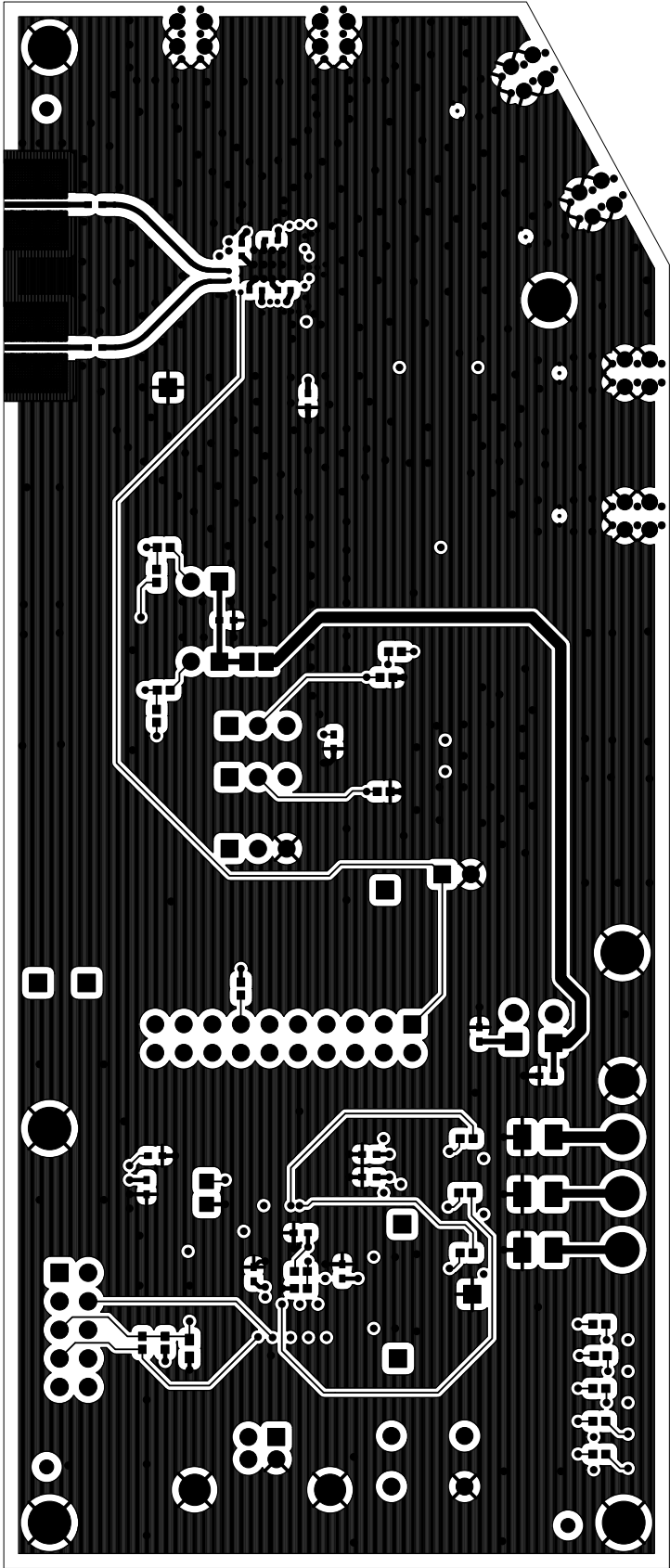


Figure 21. Secondary Side

## NOTES:

## CONTACT INFORMATION

Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
Tel: 1+(512) 416-8500  
Fax: 1+(512) 416-9669  
Toll Free: 1+(877) 444-3032

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<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>  
and register to submit a technical support request.

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