GENNUM

GS9076 HD-LINX® III
SD-SDI Automatic Reclocker with Dual Differential Outputs

GS9076 Data Sheet

Features

- SMPTE 259M-C compliant
- Automatic lock to SDI and DVB-ASI at 270Mb/s
- 4:1 input multiplexer patented technology
- Choice of dual reclocked data outputs or one data output and one recovered clock output
- Loss of Signal (LOS) Output
- Lock Detect Output
- On-chip Input and Output Termination
- Differential 50Ω inputs and outputs
- Mute, Bypass and Autobypass functions
- Footprint and drop-in compatible with existing GS2975A designs
- Pb-free and RoHS Compliant
- Single 3.3V power supply
- Operating temperature range: 0°C to 70°C

Applications

- SMPTE 259M-C Serial Digital Interfaces

Description

The GS9076 is an SD-SDI Serial Digital Reclocker designed to automatically recover the embedded clock from a digital video signal and re-time the incoming video data. The device automatically detects and locks to incoming SMPTE 259M-C SDI and DVB-ASI signals at 270Mb/s.

The GS9076 removes the high frequency jitter components from the bit-serial stream. Input termination is on-chip for seamless matching to 50Ω transmission lines. The device requires only one external crystal to set the VCO frequency when not locked and provides adjustment free operation.

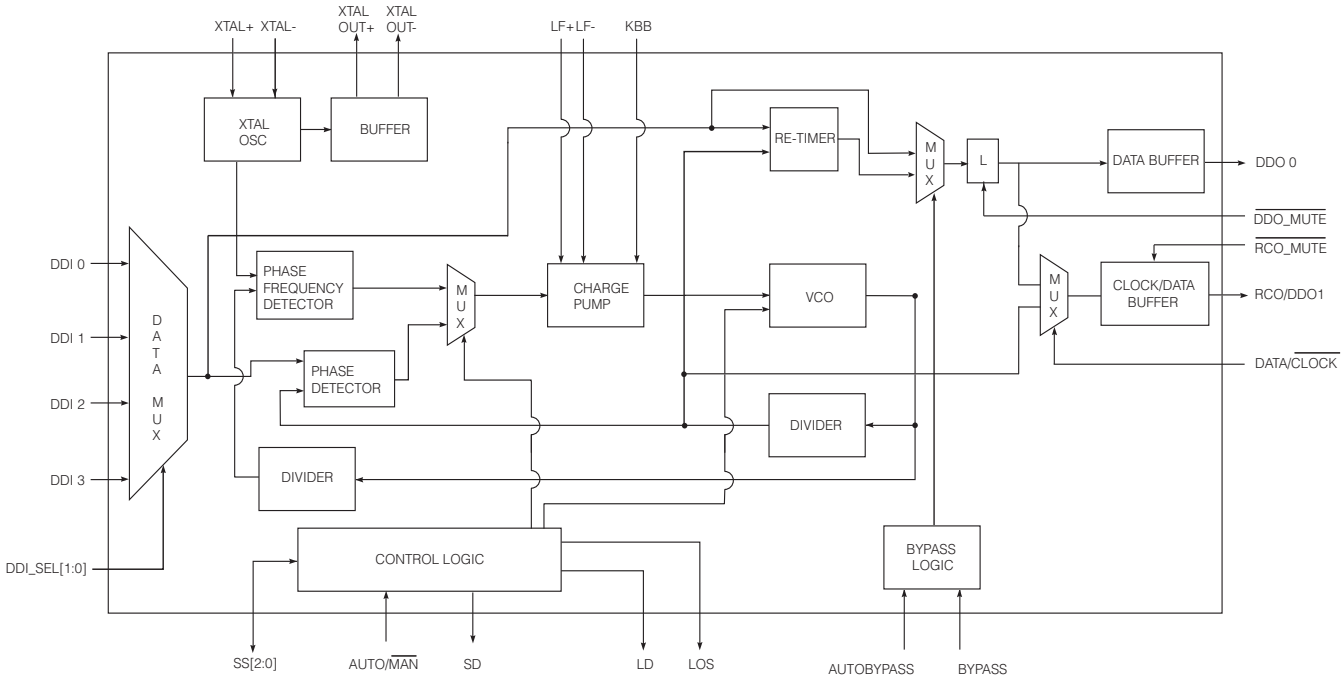
In systems which require passing of non-SMPTE data rates, the GS9076 can be configured to either automatically or manually enter a bypass mode in order to pass the signal without reclocking.

The GS9076 offers a choice of dual reclocked data outputs or one data output and one recovered clock output. The device is footprint and drop-in compatible with existing GS2975A designs, with no additional application changes required.

The GS9076 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous sub-components are RoHS compliant.

Functional Block Diagram



GS9076 Functional Block Diagram

Contents

1. Pin Out

1.1 GS9076 Pin Assignment

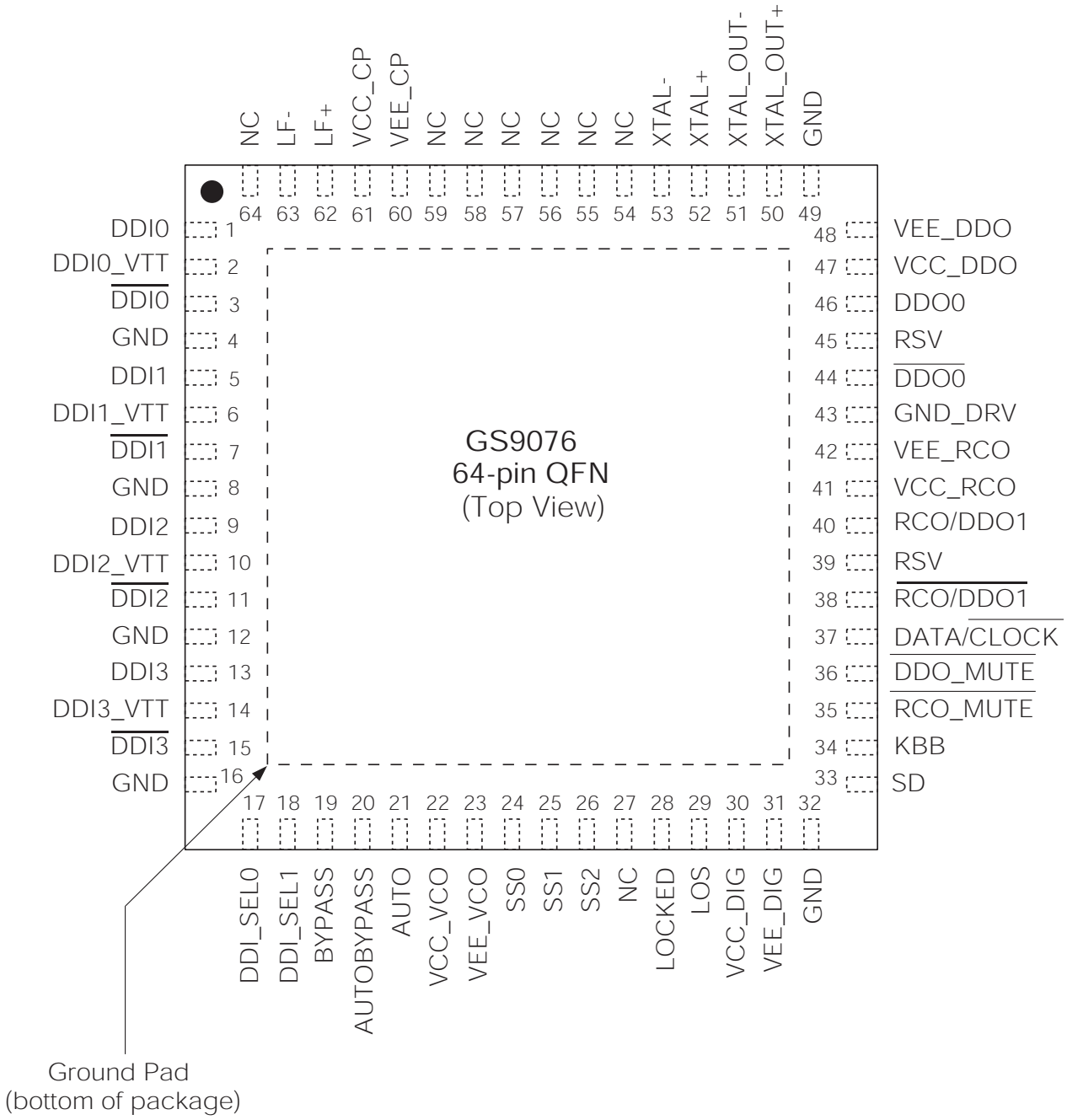


Figure 1-1: 64-Pin QFN

1.2 GS9076 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1, 3	DDI0, $\overline{\text{DDI0}}$	Input	Serial digital differential input 0.
2	DDI0_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI0 and $\overline{\text{DDI0}}$.
4, 8, 12,16, 32, 43, 49	GND	Passive	Recommended connect to GND.
5, 7	DDI1,$\overline{\text{DDI1}}$	Input	Serial digital differential input 1.
6	DDI1_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI1 and $\overline{\text{DDI1}}$.
9, 11	DDI2, $\overline{\text{DDI2}}$	Input	Serial digital differential input 2.
10	DDI2_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI2 and $\overline{\text{DDI2}}$.
13, 15	DDI3, $\overline{\text{DDI3}}$	Input	Serial digital differential input 3.
14	DDI3_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI3 and $\overline{\text{DDI3}}$.
17, 18	DDI_SEL[1:0]	Logic Input	Serial digital input select.
19	BYPASS	Logic Input	Bypass the reclocker stage. When BYPASS is HIGH, it overwrites the AUTOBYPASS setting.
20	AUTOBYPASS	Logic Input	Automatically bypasses the reclocker stage when the PLL is not locked This pin is ignored when BYPASS is HIGH.
21	AUTO	Logic Input	Auto select. This pin should be set HIGH for automatic SD-SDI and DVB-ASI standard detection.
22	VCC_VCO	Power	Most positive power supply connection for the internal VCO section. Connect to 3.3V.
23	VEE_VCO	Power	Most negative power supply connection for the internal VCO section. Connect to GND.
24, 25, 26	SS[2:0]	Bi-directional	The SS[2:0] pins will display 010 when the internal PLL has locked to a 270Mb/s input data rate.
27	NC	No Connect	Not connected internally.
28	LOCKED	Output	Lock Detect. This pin is set HIGH by the device when the PLL is locked.

DDI_SEL1	DDI_SEL0	INPUT SELECTED
0	0	DDI0
0	1	DDI1
1	0	DDI2
1	1	DDI3

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
29	LOS	Output	Loss of Signal. Set HIGH when there are no transitions on the active DDI[3:0] input.
30	VCC_DIG	Power	Most positive power supply connection for the internal glue logic. Connect to 3.3V.
31	VEE_DIG	Power	Most negative power supply connection for the internal glue logic. Connect to GND.
33	SD	Output	This signal will be set HIGH when the reclocker has locked to 270Mbps or LOW when a non-SMPTE standard is applied. (i.e. the device is not locked).
34	KBB	Analog Input	Controls the loop bandwidth of the PLL.
35	$\overline{\text{RCO\_MUTE}}$	Power	Serial clock or secondary data output mute. Assert LOW for reduced power consumption, see Section 2.2 DC Electrical Characteristics. When $\overline{\text{RCO\_MUTE}}$ = LOW, the RCO/DDO1 output is powered down. When $\overline{\text{RCO\_MUTE}}$ = HIGH, the RCO/DDO1 output is active. NOTE: This is not a logic input pin.
36	$\overline{\text{DDO\_MUTE}}$	Logic Input	Mutes the DDO0 and/or RCO/DDO1 outputs.

$\overline{\text{DDO\_MUTE}}$	$\overline{\text{RCO\_MUTE}}$	DATA/$\overline{\text{CLOCK}}$	DDO0	RCO/DDO1
1	1	0	DATA	CLOCK
1	1	1	DATA	DATA
0	1	0	MUTE	CLOCK
0	1	1	MUTE	MUTE
1	0	X	DATA	Power down
0	0	X	MUTE	Power down

NOTE:
MUTE = Outputs latched at previous data bit.
Power down = Outputs pulled to V_{cc} through 50Ω resistor.

37	DATA/$\overline{\text{CLOCK}}$	Logic Input	Data/$\overline{\text{Clock}}$ select. When set HIGH, the RCO/DDO1 pin will output a copy of the serial digital ouput (DDO0). When set LOW, the RCO/DDO1 pin will output a re-timed clock (RCO).
38, 40	$\overline{\text{RCO/DDO1}}$ / RCO/DDO1	Output	Serial clock or secondary data output. When $\overline{\text{RCO\_MUTE}}$ is connected to VCC, the serial digital differential clock or secondary data output will be presented.
39, 45	RSV	Reserved	Do not connect.
41	VCC_RCO	Power	Most positive power supply connection for the RCO/DDO1 and $\overline{\text{RCO/DDO1}}$ output driver. Connect to 3.3V.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
42	VEE_RCO	Power	Most negative power supply connection for theRCO/DDO1 and $\overline{\text{RCO/DDO1}}$ output driver. Connect to GND.
43	GND_DRV	Passive	Recommended connect to GND.
44, 46	$\overline{\text{DDO0}}$, DDO0	Output	Differential Serial Digital Outputs.
47	VCC_DDO	Power	Most positive power supply connection for the DDO0/$\overline{\text{DDO0}}$ output driver. Connect to 3.3V.
48	VEE_DDO	Power	Most negative power supply connection for the DDO0/$\overline{\text{DDO0}}$ output driver. Connect to GND.
50, 51	XTAL_OUT+, XTAL_OUT-	Output	Differential outputs of the reference oscillator used for monitoring or test purposes.
52, 53	XTAL+, XTAL-	Input	Reference crystal input. Connect to the GO1535 as shown in the Typical Application Circuit on page 21.
54 - 59	NC	No Connect	Not connected internally.
60	VEE_CP	Power	Most negative power supply connection for the internal charge pump. Connect to GND.
61	VCC_CP	Power	Most positive power supply connection for the internal charge pump. Connect to 3.3V.
62, 63	LF+, LF-	Passive	Loop filter capacitor connection. Connect as shown in the Typical Application Circuit on page 21.
64	NC	No Connect	Not connected internally. Recommended connect to GND.
–	Center Pad	–	Ground pad on bottom of package. Solder to main ground plane following recommendations under Recommended PCB Footprint on page 23

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage Range	-0.5V to +3.6 V_{DC}
Input Voltage Range	V_{ee} - 0.5V to V_{cc} + 0.5V
Operating Temperature Range	-20°C to 85°C
Storage Temperature Range	-50°C < T_s < 125°C
Input ESD Voltage	4kV HBM, 100V MM
Solder Reflow Temperature	260°C

NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown. Typical values: V_{CC} = 3.3V and T_A =25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	Operating Range	3.135	3.3	3.465	V
Supply Current	I_{CC}	RCO/DD01 enabled	–	142	170	mA
	I_{CC}	RCO/DDO1 disabled	–	123	152	mA
Power Consumption	–	RCO/DD01 enabled	–	468	590	mW
	–	RCO/DD01 disabled	–	404	528	mW
Logic Inputs DDI_SEL[1:0], BYPASS, AUTOBYPASS, AUTO, $\overline{\text{DDO\_MUTE}}$	V_{IH}	High	2.0	–	–	V
	V_{IL}	Low	–	–	0.8	V
Logic Outputs SD, LOCKED, LOS	V_{OH}	I_{OH} = -2mA	2.4	–	–	V
	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
Bi-Directional Pins (Auto Mode) SS[2:0], AUTO = 1	V_{OH}	I_{OH} = -2mA	2.4	–	–	V
	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
XTAL_OUT+, XTAL_OUT-	V_{OH}	High	–	V_{CC} - 0.075	–	V
	V_{OL}	Low	–	V_{CC} - 0.300	–	V

Table 2-1: DC Electrical Characteristics (Continued)

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown. Typical values: V_{CC} = 3.3V and T_A =25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RCO_MUTE	–	I = -1.5mA	V_{CC} - 0.165	V_{CC}	V_{CC} + 0.165	V
Serial Input Voltage	–	Common Mode	1.65 + (V_{SID}/2)	–	V_{CC} - (V_{SID}/2)	V
Serial Output Voltage DDO0/$\overline{\text{DDO0}}$, RCO/DDO1 / $\overline{\text{RCO/DDO1}}$	–	Common Mode	–	V_{CC} - (V_{OD}/2)	–	V

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown. Typical values: V_{CC} = 3.3V and T_A =25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	–	–	–	270	–	Mb/s	–
Serial Input Jitter Tolerance	–	Worst case modulation (e.g. square wave modulation)	0.8	–	–	UI	–
PLL Lock Time - Asynchronous	t_{ALOCK}	–	–	0.5	2.0	ms	–
PLL Lock Time - Synchronous	t_{SLOCK}	KBB = Float, CLF=47nF, 270Mb/s	–	5	20	us	–
Serial Output Rise/Fall Time SDO0 and RCO/DDO1 (20% - 80%)	t_{rSDO},t_{rRCO}	50Ω load (on chip)	–	110	–	ps	–
	t_{fSDO},t_{fRCO}	50Ω load (on chip)	–	110	–	ps	–
Serial Digital Input Signal Swing	V_{SID}	Differential with internal 100Ω input termination See Figure 2-1	100	–	800	mV_{p-p}	–
Serial Digital Output Signal Swing DDO0 and RCO/DDO1	VOD	100Ω load differential See Figure 2-2	300	450	600	mV_{p-p}	–
DDO0 to DDO1 skew	DD_{skew}	270Mb/s	–	156	–	ps	1
DDO0 to RCO skew	DR_{skew}	270 Mb/s	–	37	–	ps	2
Serial Output Jitter on DDO0 and DDO1	t_{OJ}	270 Mb/s	–	0.02	0.07	UI	3
Additive Jitter	t_{AJ}	Bypass mode, 270 Mb/s	–	15	–	ps	–

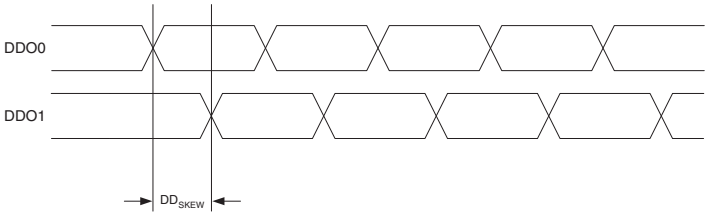
Table 2-2: AC Electrical Characteristics (Continued)

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown. Typical values: V_{CC} = 3.3V and T_A =25°C

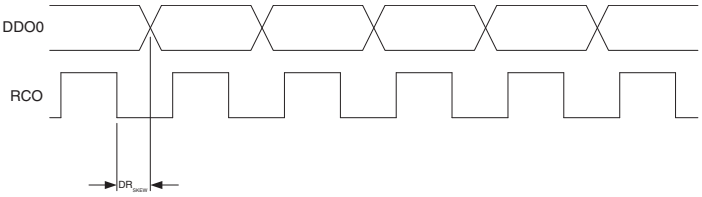
Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Loop Bandwidth	BW_{LOOP}	270 Mb/s, KBB = VCC	–	0.16	–	MHz	–
		270 Mb/s, KBB = FLOAT	–	0.32	–	MHz	–
		270 Mb/s, KBB = GND, <0.1dB Peaking	–	0.64	–	MHz	–

NOTES:

1. DDO0 to DDO1 skew allignment as defined here:



2. DDO0 to RCO skew allignment as defined here:



3. KBB = Float, PRN = 2^{23}-1, input jitter = $40ps_{p-p}$

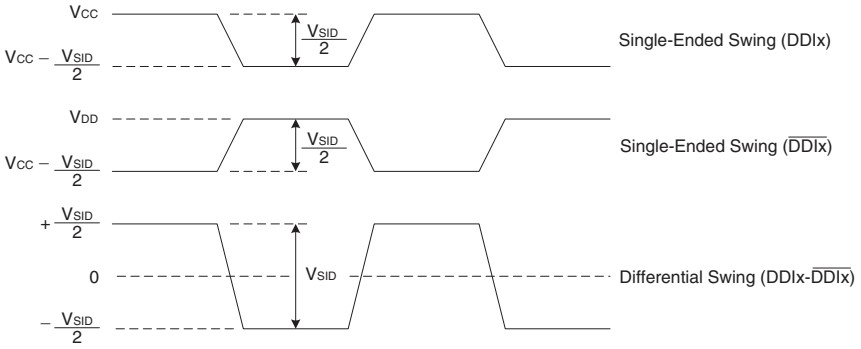


Figure 2-1: Serial Digital Input Signal Swing

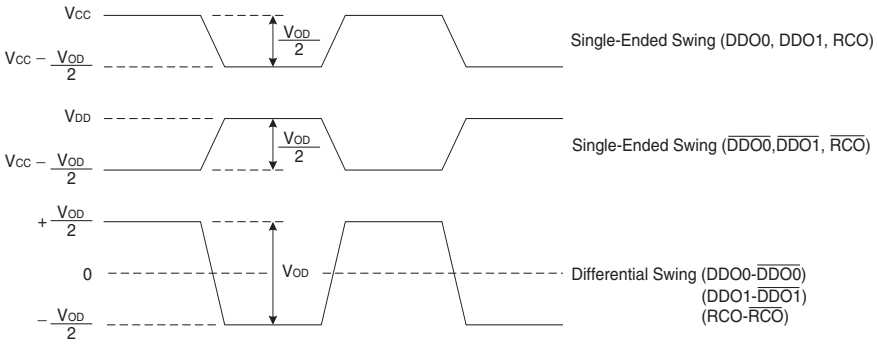


Figure 2-2: Serial Digital Output Signal Swing

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-3. The recommended standard Pb reflow profile is shown in Figure 2-4.

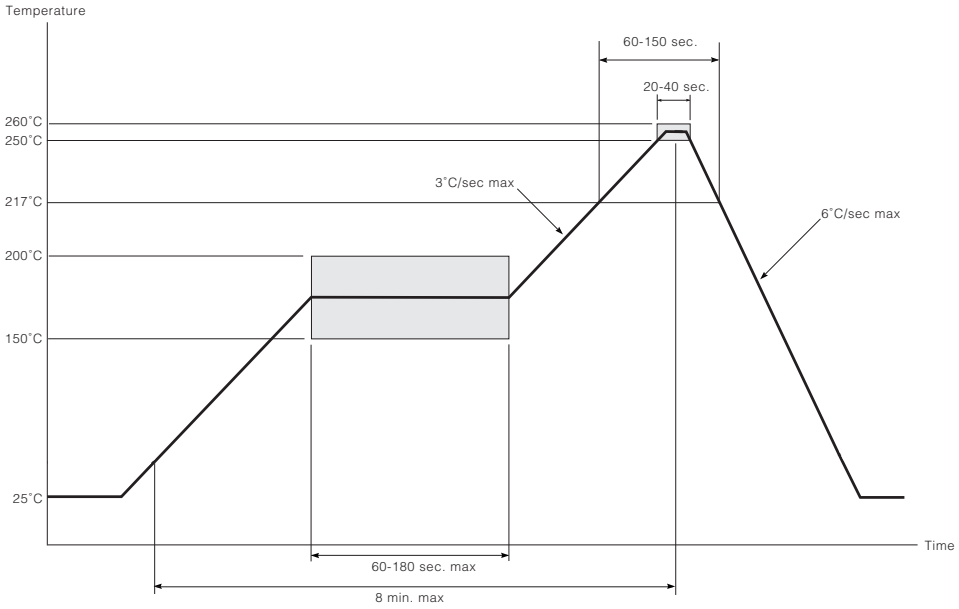


Figure 2-3: Maximum Pb-free Solder Reflow Profile (Preferred)

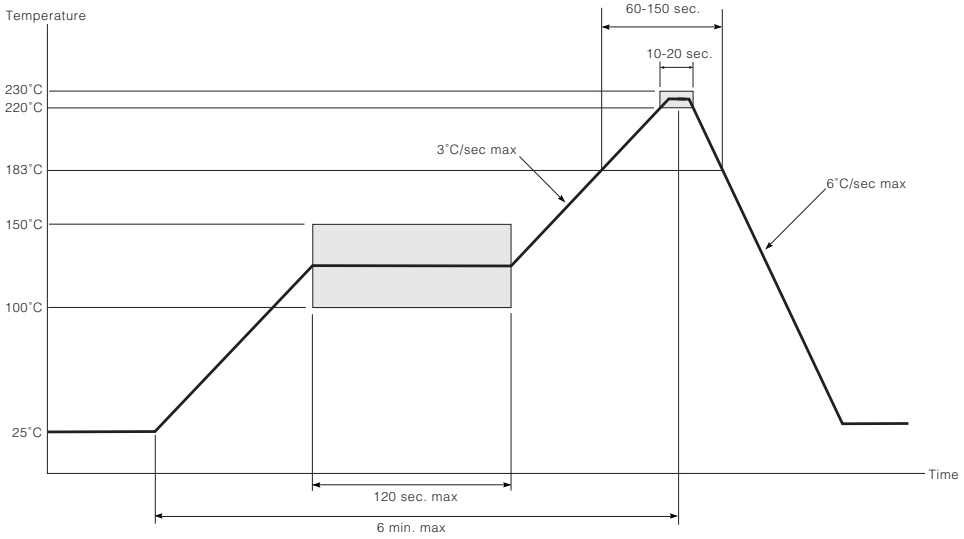


Figure 2-4: Standard Pb Solder Reflow Profile

3. Input / Output Circuits

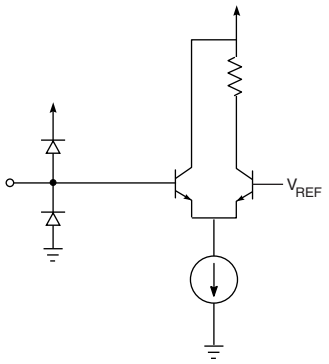


Figure 3-1: TTL Inputs

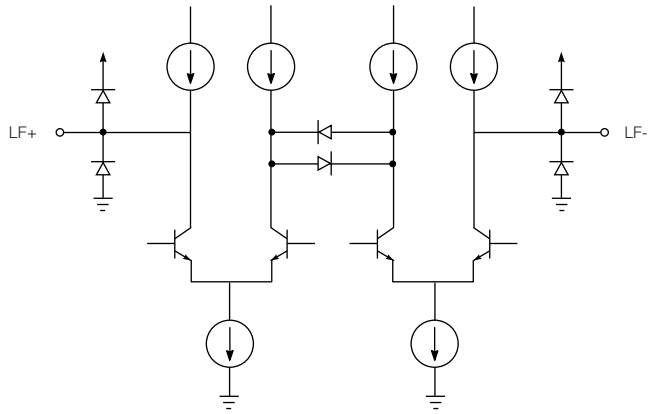


Figure 3-2: Loop Filter

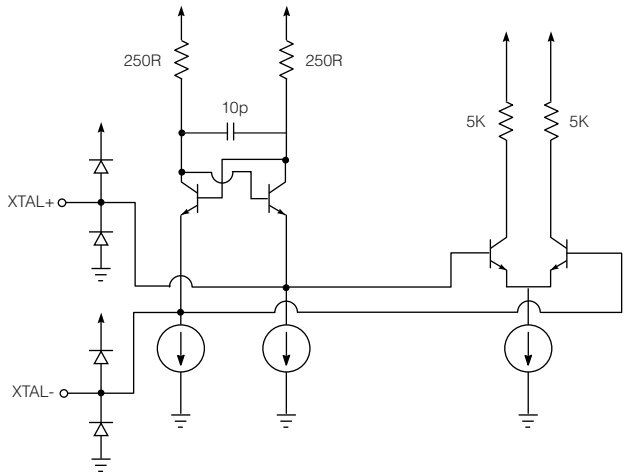


Figure 3-3: Crystal Input

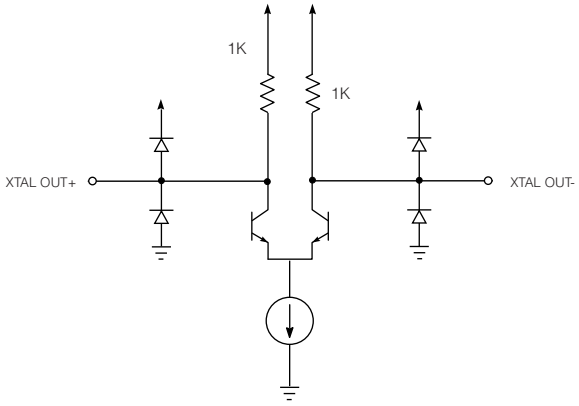


Figure 3-4: Crystal Output Buffer

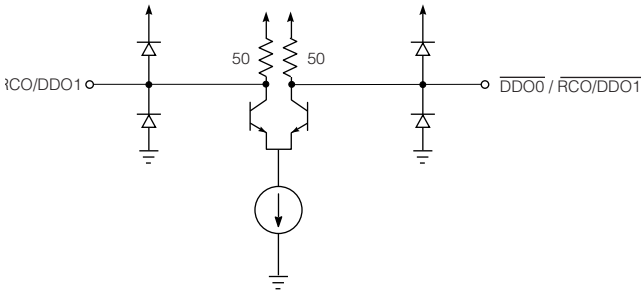


Figure 3-5: Serial Data Outputs, Serial Clock Outputs

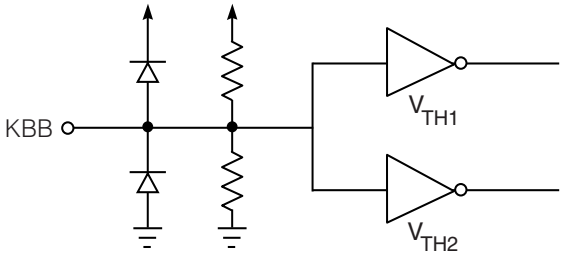


Figure 3-6: KBB

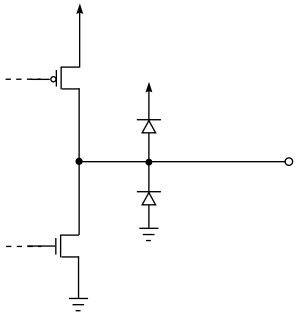


Figure 3-7: Indicator Outputs: SD, LOCKED, LOS

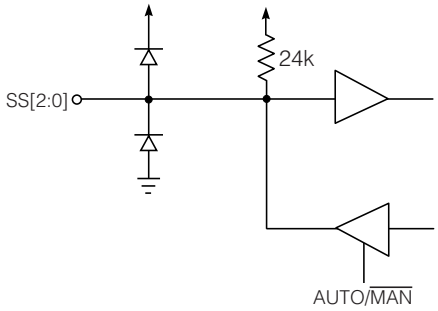


Figure 3-8: Standard Select/Indication Bi-directional Pins

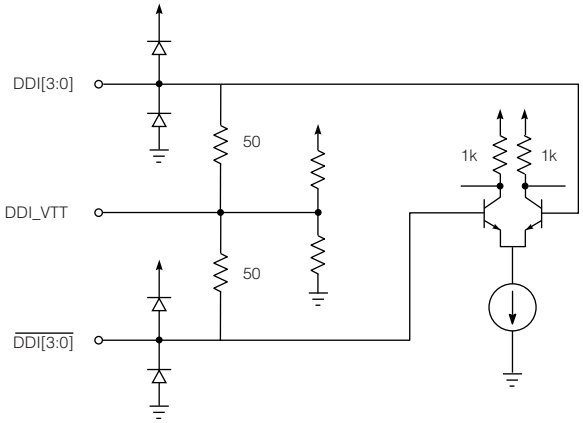


Figure 3-9: Serial Data Inputs

4. Detailed Description

The GS9076 is a SD-SDI Serial Digital Reclocker designed to automatically recover the embedded clock from a digital video signal and re-time the incoming video data.

The GS9076 will recover the embedded clock signal and re-time the data from a SMPTE 259M-C compliant digital video signal.

Using the functional block diagram (page 2) as a guide, Slew Rate Phase Lock Loop (S-PLL) on page 16 to Lock and LOS on page 20 describes each aspect of the GS9076 in detail.

4.1 Slew Rate Phase Lock Loop (S-PLL)

The term “slew” refers to the output phase of the PLL in response to a step change at the input. Linear PLLs have an output phase response characterized by an exponential response whereas an S-PLL’s output is a ramp response (see Figure 4-1). Because of this non-linear response characteristic, traditional small signal analysis is not possible with an S-PLL.

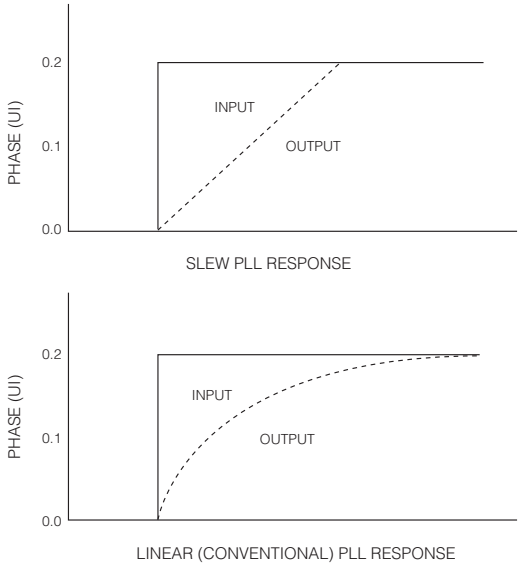


Figure 4-1: PLL Characteristics

The S-PLL offers several advantages over the linear PLL. The Loop Bandwidth of an S-PLL is independent of the transition density of the input data. Pseudo-random data has a transition density of 0.5 verses a pathological signal which has a transition density of 0.05. The loop bandwidth of a linear PLL will change proportionally with this change in transition density. With an S-PLL, the loop bandwidth is defined by the jitter at the data input. This translates to infinite loop bandwidth with a zero jitter input signal. This allows the loop to correct for small variations in the input jitter quickly, resulting in very low output jitter. The loop bandwidth of the GS9076's PLL is defined at 0.2UI of input jitter.

The PLL consists of two acquisition loops. First is the Frequency Acquisition (FA) loop. This loop is active when the device is not locked and is used to achieve lock to the supported data rates. Second is the phase acquisition (PA) loop. Once locked, the PA loop tracks the incoming data and makes phased corrections to produce a re-clocked output.

4.2 VCO

The internal VCO of the GS9076 is an LC oscillator. It is trimmed at the time of manufacture to capture all data rates over temperature and operation voltage ranges.

Integrated into the VCO is a series of programmable dividers used to achieve all serial data rates, as well as additional dividers for the frequency acquisition loop.

4.3 Charge Pump

During frequency acquisition, the charge pump has two states, "pump-up" and "pump-down," which is produced by a leading or lagging phase difference between the input and the VCO frequency.

During phase acquisition, there are two levels of "pump-up" and two levels of "pump down" produced for leading and lagging phase difference between the input and VCO frequency. This is to allow for greater precision of VCO control.

The charge pump produces these signals by holding the integrated frequency information on the external loop-filter capacitor, C_{LF}. The instantaneous frequency information is the result of the current flowing through an internal resistor connected to the loop-filter capacitor.

4.4 Frequency Acquisition Loop — The Phase-Frequency Detector

An external crystal of 14.140 MHz is used as a reference to keep the VCO centered at the last known data rate. This allows the device to achieve a fast synchronous lock, especially in cases where a known data rate is interrupted. The crystal reference is also used to clock internal timers and counters. To keep the optimal performance of the reclocker over all operating conditions, the crystal frequency must be 14.140 MHz, +/-50ppm. The GO1535 meets this specification and is available from GENNUM.

The VCO is divided by a selected ratio which is dependant on the input data rate. The resultant is then compared to the crystal frequency. If the divided VCO frequency and the crystal frequency are within 1% of each other, the PLL is considered to be locked to the input data rate.

4.5 Phase Acquisition Loop — The Phase Detector

The phase detector is a digital quadrature phase detector. It indicates whether the input data is leading or lagging with respect to a clock that is in phase with the VCO (I-clk) and a quadrature clock (Q-clk). When the phase acquisition loop (PA loop) is locked, the input data transition is aligned to the falling edge of I-clk and the output data is re-timed on the rising edge of I-clk. During high input jitter conditions (>0.25UI), Q-clk will sample a different value than I-clk. In this condition, two extra phase correction signals will be generated which instructs the charge pump to create larger frequency corrections for the VCO.

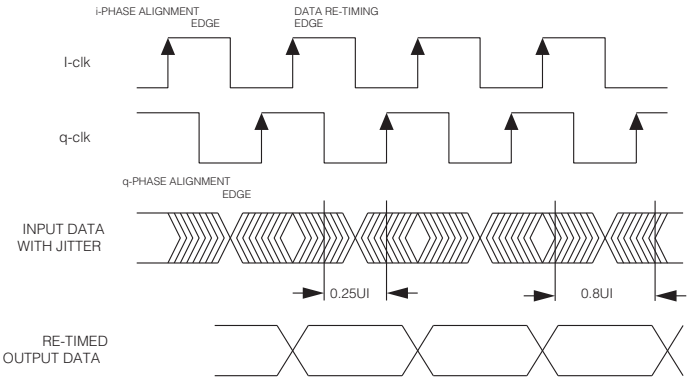


Figure 4-2: Phase Detector Characteristics

When the PA loop is active, the crystal frequency and the incoming data rate are compared. If the resultant is more that 2%, the PLL is considered to be unlocked and the system jumps to the FA loop.

4.6 4:1 Input Mux

The 4:1 input mux allows the connection of four independent streams of video/data. There are four differential inputs (DDI[3:0] and $\overline{\text{DDI}}$[3:0]). The active channel can be selected via the DDI_SEL[1:0] pins. Table 4-1 shows the input selected for a given state at DDI_SEL[1:0].

Table 4-1: Bit Pattern for Input Select

DDI_SEL[1:0]	Selected Input
00	DDI0
01	DDI1
10	DDI2
11	DDI3

The DDI inputs are designed to be DC interfaced with the output of the GS9074A Cable Equalizer. There are on chip 50Ω termination resistors which come to a common point at the DDI_VT pins. Connect a 10nF capacitor to this pin and connect the other end of the capacitor to ground. This terminates the transmission line at the inputs for optimum performance.

If only one input pair is used, connect the unused positive inputs to +3.3V and leave the unused negative inputs floating. This helps to eliminate crosstalk from potential noise that would couple to the unused input pair.

4.7 Automatic and Manual Data Rate Selection

The GS9076 can be configured to manually lock to a specific data rate or automatically search for and lock to the incoming data rate. The AUTO/$\overline{\text{MAN}}$ pin selects automatic data rate detection mode (Auto mode) when HIGH and manual data rate selection mode (Manual mode) when LOW.

In Auto mode, the SS[2:0] bi-directional pins become outputs and the bit pattern indicates the data rate that the PLL is locked to (or previously locked to).

In Manual mode, the data rate can be programmed and the SS[2:0] pins become inputs. In this mode, the PLL will only lock to the data rate selected.

Table 4-2 shows the SS[2:0] pin settings for either the data rate selected (in Manual mode) or the data rate that the PLL has locked to (in Auto mode).

Table 4-2: Data Rate Indication/Selection Bit Pattern

SS[2:0]	Data Rate (Mb/s)
010	270

4.8 Bypass Mode

In Bypass mode, the GS9076 passes the data at the inputs directly to the outputs. There are two pins that control the bypass function: BYPASS and AUTOBYPASS.

When BYPASS is set HIGH, the GS9076 will be in Bypass mode.

When AUTOBYPASS is set HIGH, the GS9076 will be configured to enter Bypass mode only when the PLL has not locked to a data rate. When BYPASS is set HIGH, AUTOBYPASS will be ignored.

When the PLL is not locked, and both BYPASS and AUTOBYPASS are set LOW, the serial digital output DDO0/$\overline{\text{DDO0}}$ or DDO1/$\overline{\text{DDO1}}$ will produce invalid data.

4.9 Lock and LOS

The LOCKED signal is an active high output which indicates when the PLL is locked.

The internal lock logic of the GS9076 includes a system which monitors the Frequency Acquisition Loop and the Phase Acquisition Loop as well as a monitor to detect harmonic lock.

The LOS (Loss of Signal) output is an active HIGH output which indicates the absence of data transitions at the DDIx input. In order for this output to be asserted, transitions must not be present for a period of t_{LA} = 5 - 10 us. After this output has been asserted, LOS will deassert within t_{LD} = 0 - 5 us after the appearance of a transition at the DDIx input.

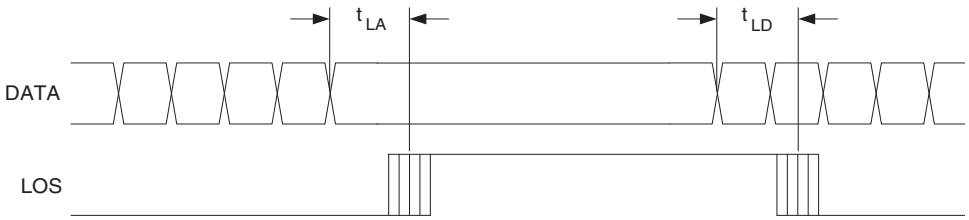
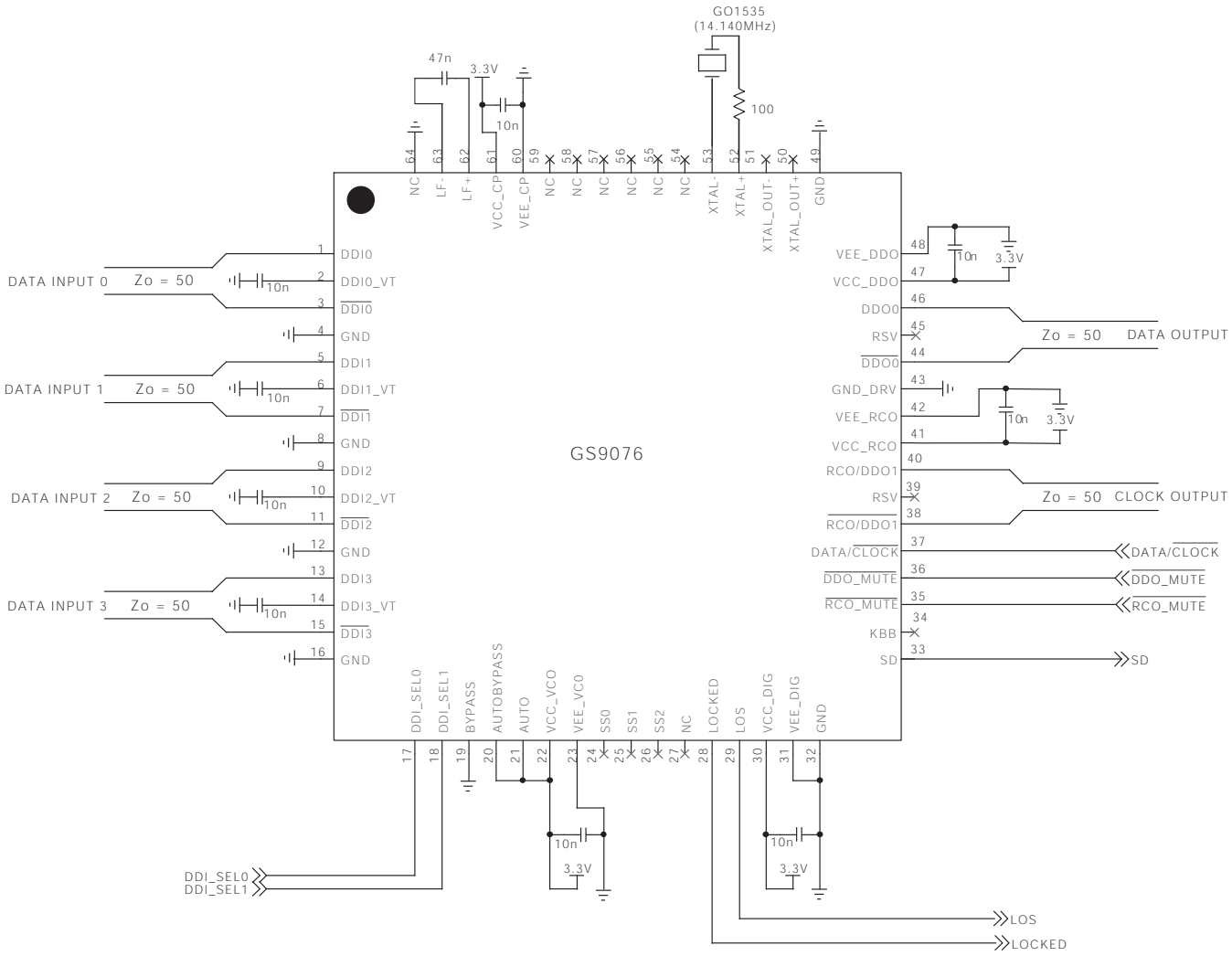


Figure 4-3: LOS signal timing

NOTE: LOS is sensitive to transitions appearing at the input, and does not distinguish between transitions caused by input data, and transitions due to noise.

5. Typical Application Circuit

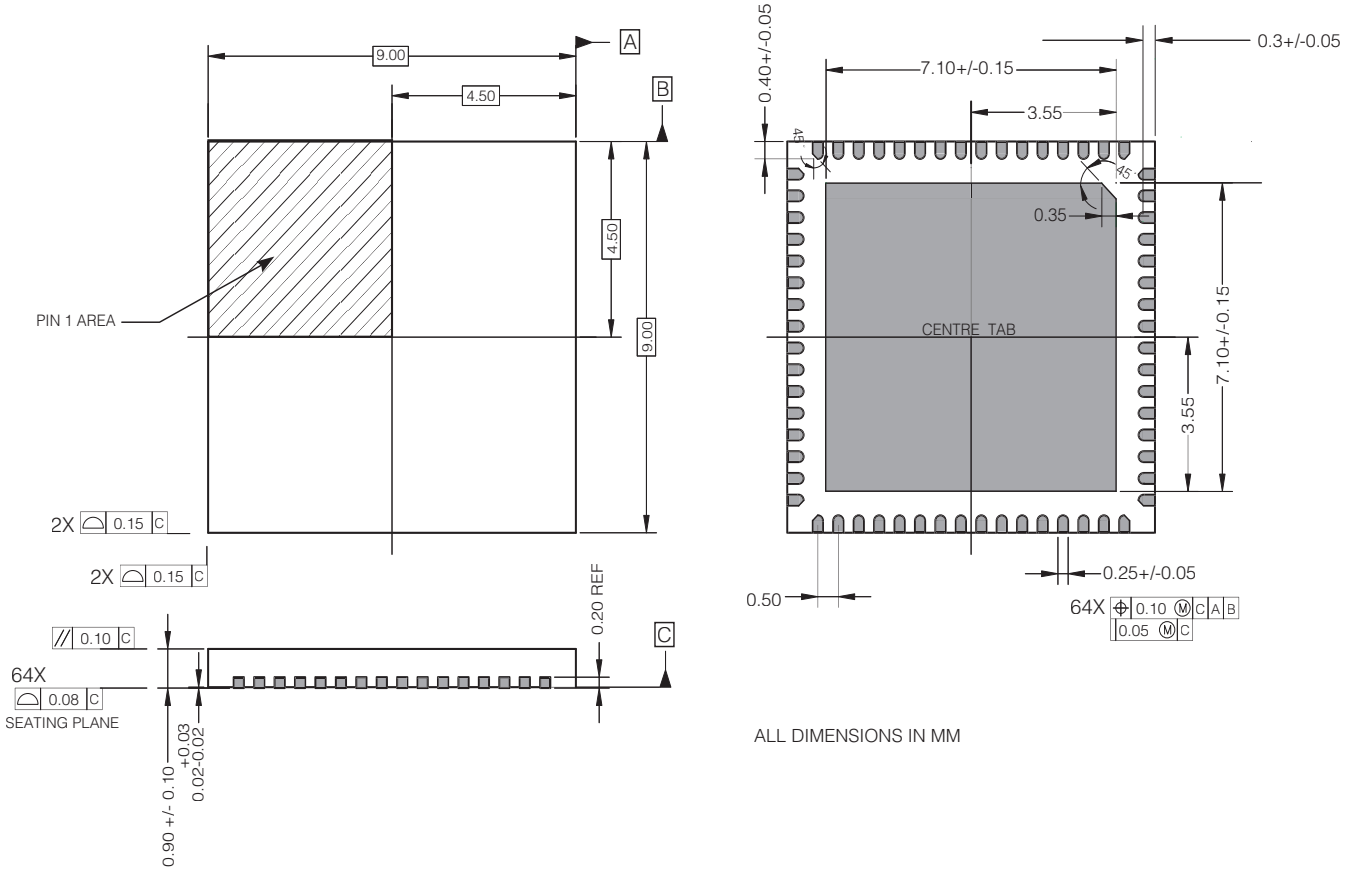


Note: All resistors in ohms and all capacitors in Farads.

Figure 5-1: GS9076 Typical Application Circuit

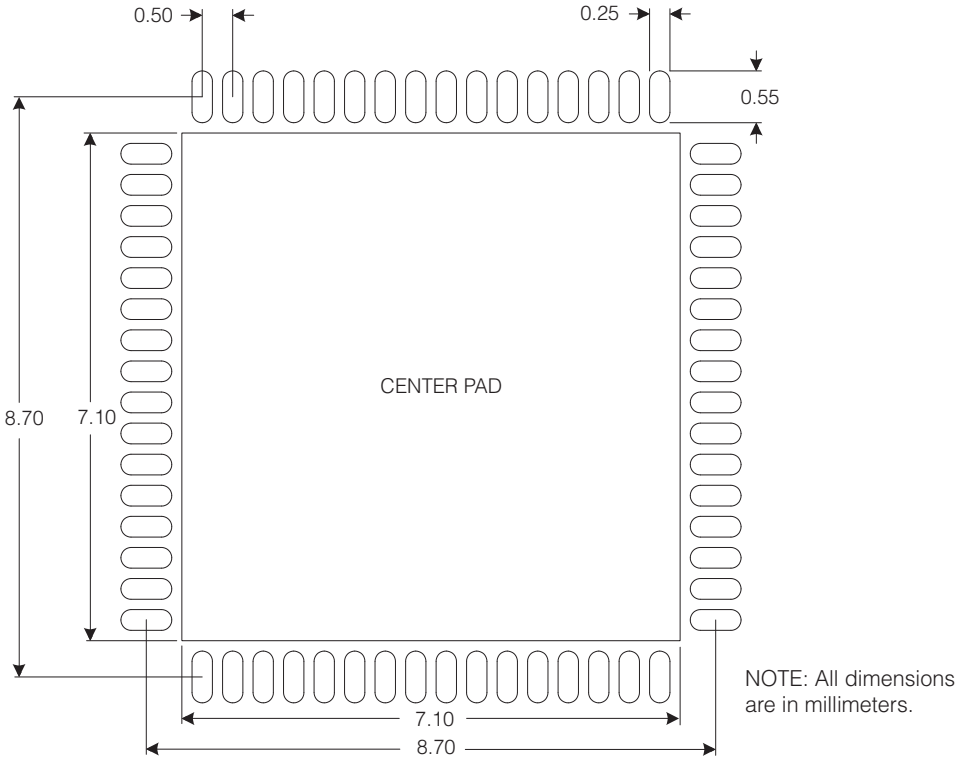
6. Package & Ordering Information

6.1 Package Dimensions



ALL DIMENSIONS IN MM

6.2 Recommended PCB Footprint



The center pad of the PCB footprint should be connected to the ground plane by a minimum of 36 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	9mm x 9mm 64-pin QFN
Moisture Sensitivity Level (per JEDEC J-STD-020C)	3
Junction to Case Thermal Resistance, $\theta_{j\text{-}c}$	9.1°C/W
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at zero airflow)	21.5°C/W
Junction to Board Thermal Resistance, $\theta_{j\text{-}b}$	5.6°C/W
Psi, Ψ	0.2°C/W
Pb-free and RoHS Compliant	Yes

6.4 Marking Diagram

6.5 Ordering Information

	Part Number	Package	Temperature Range
GS9076	GS9076-CNE3	Pb-free 64-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
1	149009	–	January 2008	Changes to Functional Block Diagram, Figure 3-7 and Ordering Information. Addition of section 4.7 Automatic and Manual Data Rate Selection.
0	144926	–	May 2007	New Document.

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