Dec. 2013

DDR4 SDRAM Memory

Product Guide

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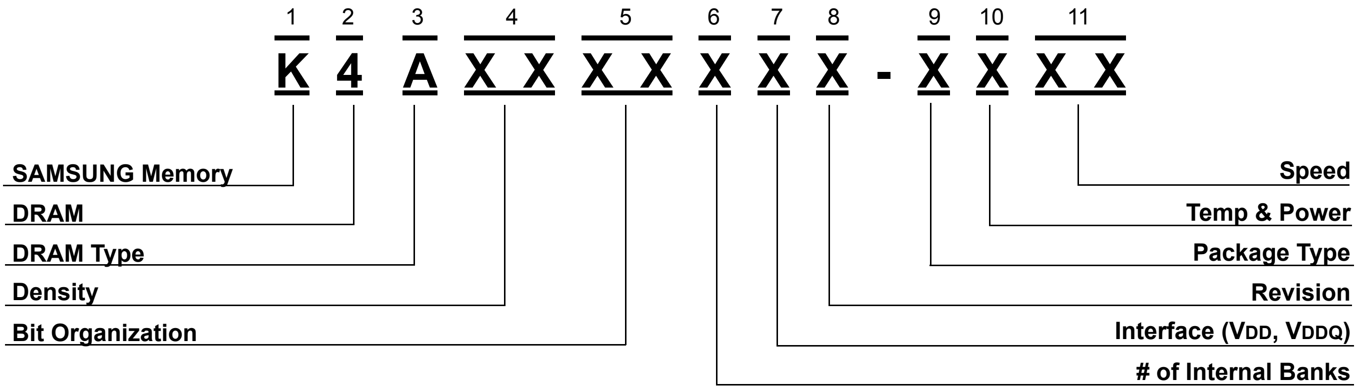
1. DDR4 SDRAM MEMORY ORDERING INFORMATION



1. SAMSUNG Memory : K

2. DRAM : 4

3. DRAM Type

A : DDR4 SDRAM

4. Density

4G : 4Gb
8G : 8Gb

5. Bit Organization

04 : x 4
08 : x 8

6. # of Internal Banks

5 : 16 Banks

7. Interface (VDD, VDDQ)

W : POD (1.2V, 1.2V)

8. Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
G : 8th Gen.
H : 9th Gen.

9. Package Type

B : FBGA (Halogen-free & Lead-free, Flip Chip)
M : FBGA (Halogen-free & Lead-free, DDP)

10. Temp & Power

C : Commercial Temp.(0°C ~ 85°C) & Normal Power

11. Speed

PB : DDR4-2133 (1066MHz @ CL=15, tRCD=15, tRP=15)
RC : DDR4-2400 (1200MHz @ CL=17, tRCD=17, tRP=17)

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2. DDR4 SDRAM Component Product Guide

Density	Banks	Part Number	Package & Power, Temp. & Speed	Org.	VDD Voltage	PKG	Avail.	NOTE
4Gb D-die	16Banks (4Bank Groups)	K4A4G045WD	BCPB/RC$^{1)}$	1G x 4	1.2V	78 ball FBGA	Now	
		K4A4G085WD	BCPB/RC$^{1)}$	512M x 8				

NOTE :

1) Need to Contact SAMSUNG for RC(2400Mbps) availability.

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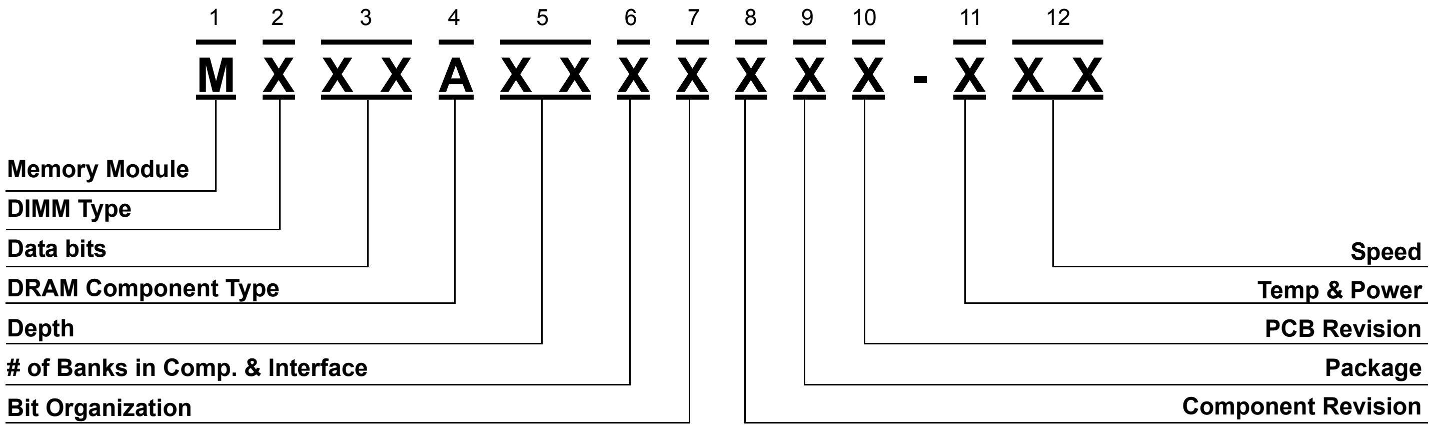
3. DDR4 SDRAM Module Ordering Information



1. Memory Module : M

2. DIMM Type

3 : R/LRDIMM
4 : SODIMM

3. Data Bits

93 : x72 288pin Registered DIMM
86 : x72 288pin Load Reduced DIMM
74 : x72 260pin SODIMM

4. DRAM Component Type

A : DDR4 SDRAM (1.2V VDD)

5. Depth

1G : 1G
2G : 2G
4G : 4G
8G : 8G
1K : 1G (for 8Gb)
2K : 2G (for 8Gb)

6. # of Banks in comp. & Interface

4 : 16Banks & POD-1.2V

7. Bit Organization

0 : x 4
3 : x 8

8. Component Revision

M : 1stGen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
G : 8th Gen.

9. Package

B : FBGA (Halogen-free & Lead-free, Flip Chip)
M : FBGA (Halogen-free & Lead-free, DDP)

10. PCB Revision

0 : None
1 : 1st Rev.
2 : 2nd Rev.
3 : 3rd Rev.
4 : 4th Rev.

11. Temp & Power

C : Commercial Temp.(0°C ~ 85°C) & Normal Power

12. Speed

PB : DDR4-2133 (1066MHz @ CL=15, tRCD=15, tRP=15)
RC : DDR4-2400 (1200MHz @ CL=17, tRCD=17, tRP=17)

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4. DDR4 SDRAM Module Product Guide

4.1 288Pin DDR4 Registered DIMM

288Pin DDR4 Registered DIMM

Org.	Density	Part Number	Speed	Raw Card	Composition	Comp. Version		Internal Banks	Rank	PKG	Height	Avail.	NOTE
1G x72	8GB	M393A1G40DB0	CPB/RC1)	C(1Rx4)	1G x4 * 18pcs	4Gb	D-die	16	1	78ball FBGA	31.25mm	Now	
2G x72	16GB	M393A2G40DB0	CPB/RC1)	A(2Rx4)	1G x4 * 36pcs	4Gb	D-die	16	2	78ball FBGA	31.25mm	Now	

NOTE :
1) Need to Contact SAMSUNG for RC(2400Mbps) availability.

4.2 288Pin DDR4 Load Reduced DIMM

288Pin DDR4 Load Reduced DIMM

Org.	Density	Part Number	Speed	Raw Card	Composition	Comp. Version		Internal Banks	Rank	PKG	Height	Avail.	NOTE
4G x72	32GB	M386A4G40DM0	CPB/RC1)	D(4Rx4)	DDP 2G x4 * 36pcs	4Gb	D-die	16	4	78ball FBGA	31.25mm	Now	

NOTE :
1) Need to Contact SAMSUNG for RC(2400Mbps) availability.

4.3 260Pin DDR4 ECC SODIMM

260Pin DDR4 ECC SODIMM

Org.	Density	Part Number	Speed	Raw Card	Composition	Comp. Version		Internal Banks	Rank	PKG	Height	Avail.	NOTE
1G x72	8GB	M474A1G43DB0	CPB/RC1)	G(2Rx8)	4G x8 * 18pcs	4Gb	D-die	16	2	78ball FBGA	30mm	1Q’14	

NOTE :
1) Need to Contact SAMSUNG for RC(2400Mbps) availability.

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5. LRDIMM Memory Buffer Information

5.1 Label Example

5.2 JEDEC Description Information

① Module total capacity, in gigabytes, for primary bus (ECC not counted)

② Number of package ranks of memory installed and number of logical ranks per package rank

③ Device organization (data bit width) of SDRAMs used on this assembly

④ SDRAM and support component supply voltage (VDD)
blank = 1.2 V operable
L = TBD V operable, TBD V endurant

⑤ Module speed in Mb/s/data pin

⑥ SDRAM speed grade

⑦ Module Type
E = Unbuffered DIMM ("UDIMM"), x64 primary + 8 bit ECC module data bus
L = Load Reduced DIMM (“LRDIMM”), x64 primary + 8 bit ECC module data bus
R = Registered DIMM ("RDIMM"), x64 primary + 8 bit ECC module data bus
S = Small Outline DIMM ("SO-DIMM"), no ECC (x64 bit module data bus)
U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
T = Unbuffered 72-bit small outline DIMM ("72b-SO-DIMM"), x64 primary + 8bit ECC module data bus

⑧ Reference design file used for this design (if applicable)
A = Reference design for raw card ’A’ is used for this assembly
B = Reference design for raw card ’B’ is used for this assembly
AC = Reference design for raw card ’AC’ is used for this assembly (example only)
ZZ = None of the JEDEC standard reference designs were used for this assembly

⑨ Revision number of the reference design used
0 = Initial release
1 = First revision
2 = Second revision
P = Pre-release or Engineering sample
Z = To be used when reference raw card = ZZ

⑩ JEDEC SPD Revision Encoding and Additions level used on this DIMM

5.3 RCD (& Data Buffer) Information

(These codes are only used SAMSUNG, Not JEDEC)

⑪ RCD, Data Buffer Vendor used on this DIMM
TBD

⑫ RCD, Data Buffer Revision used on this DIMM

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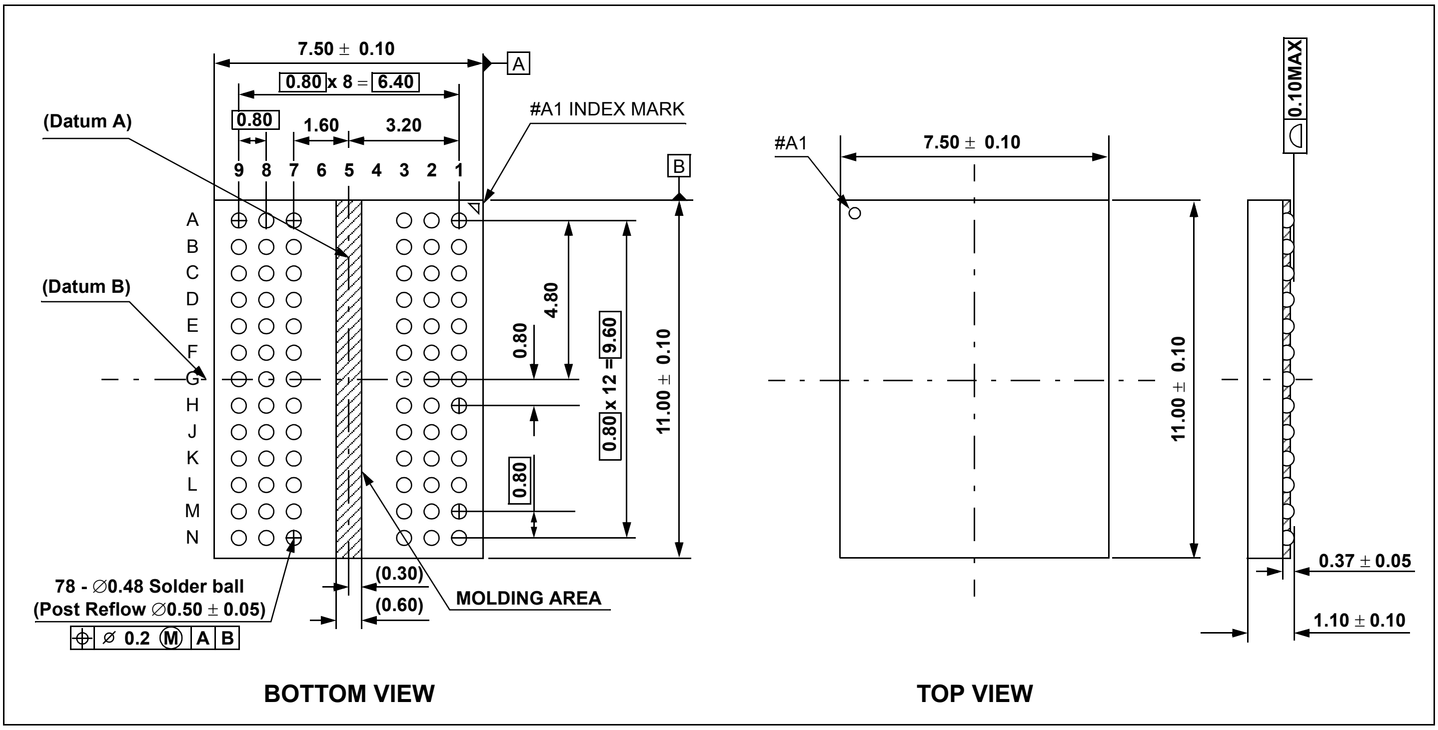
6. Package Dimension

4Gb D-die (x4/x8)



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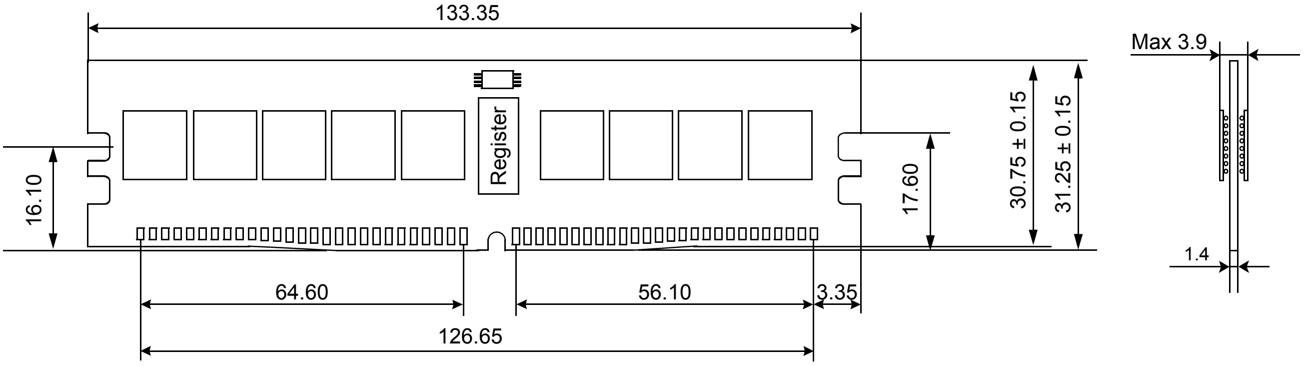
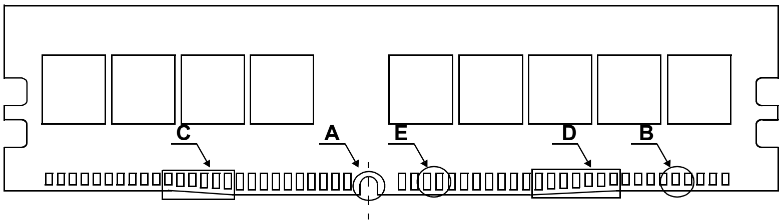
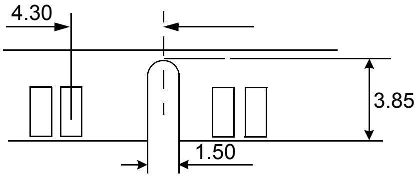
7. Module Dimension

x72 288pin DDR4 SDRAM RDIMM

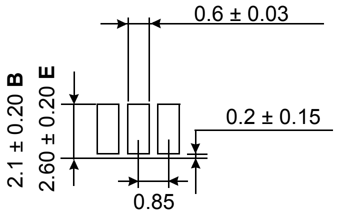
Units : Millimeters



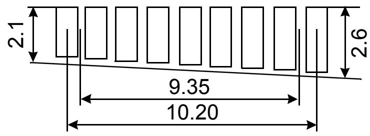




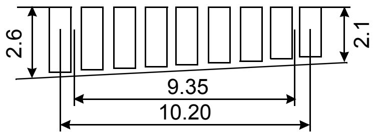
Detail A



Detail B,E



Detail C



Detail D

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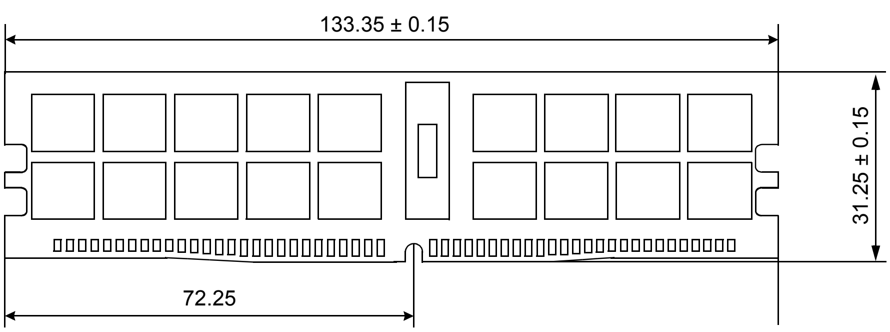
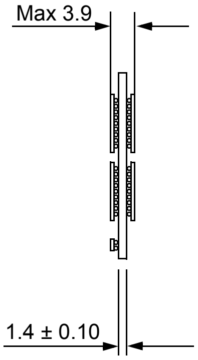
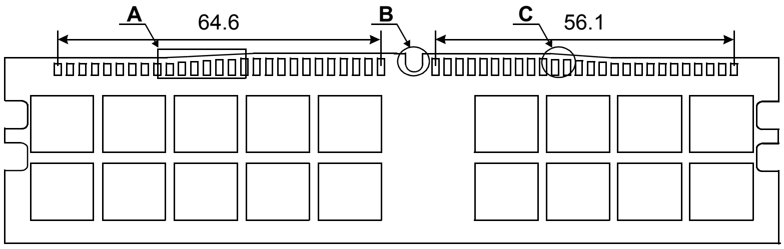
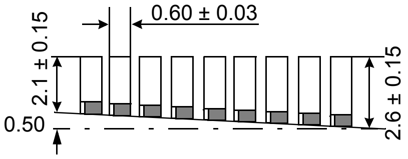
x72 288pin DDR4 SDRAM LRDIMM

Units : Millimeters

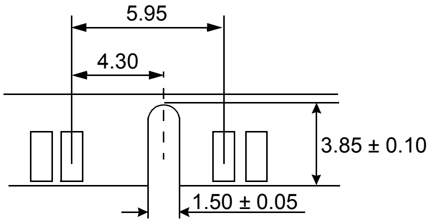




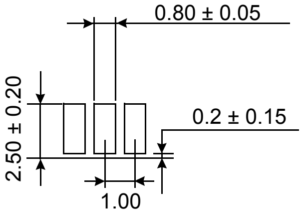




Detail A



Detail B



Detail C

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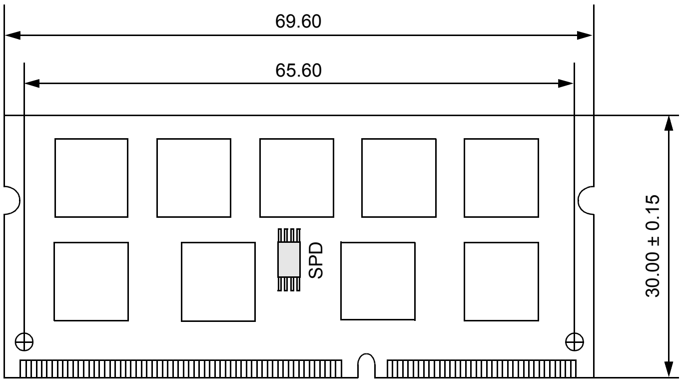
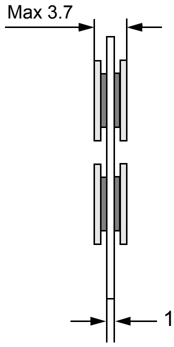
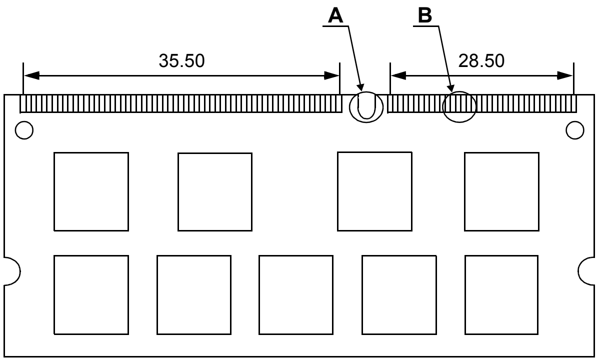
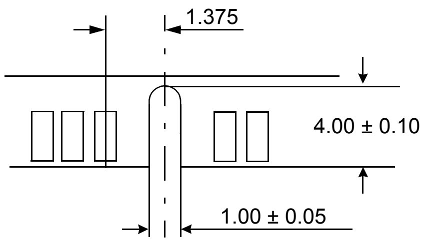
x72 260pin DDR4 SDRAM ECC SODIMM

Units : Millimeters

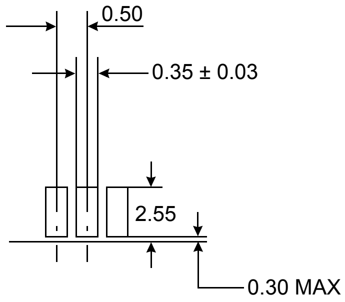








Detail A



Detail B

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