

STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT Voltage Detector IC built in Delay Circuit

TYPE BD45XXXG Series

FEATURES • Detection voltage line up : 2.3~4.8V

•High precision detection voltage: ±1.0%

OABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Par	ameter	Symbol	Limit	Unit
Sup	oly Voltage ※1	VDD-GND	-0.3 to +10	٧
Output Voltage ※1	Nch Open Drain Output	Vout	GND-0.3 to +10	V
Input Vo	oltage of ER	VER	GND-0.3 to VDD+0.3	V
Power	Dissipation	Pd	540	mW
Operating	Temperature %1	Topr	-40 to +105	°C
Storage Tem	perature Range	Tstg	-55 to +125	°C
Junction	Temperature	Tjmax	125	°C

^{※1} Do not exceed Pd.

NOTE: This product is not designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

^{※2} Mounted on 70mm × 70mm × 1.6mm Glass Epoxy PCB, Pd derated at 5.4mW/°C for tempearture above Ta=25°C NOTE: The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.



OELECTRICAL CHARACTERISTICS (Unless Otherwise Specified Ta=-40 to 105°C)

		ol Condition		Limit			Unit	
Parameter	Symbol			Min.	Тур.	Max.	Offic	
Detection Voltage	VDET	VDD=H→L, RL=470kΩ		VDET(T) × 0.99	VDET(T)	VDET(T) × 1.01	V	
Detection Voltage Temperature coefficient	VDET/	-40°C∼+105°C			±100	±360	ppm ∕°C	
Hysteresis Voltage	ΔVDET	VDD=L→H→L, RL=470kΩ			VDET(T) × 0.05	VDET(T) × 0.08	٧	
'High' Output Delay time	1	CL=100pF, RL=100k Ω BD45XX5G BD45XX1G	BD45XX5G	45	50	55	msec	
	tPLH		BD45XX1G	90	100	110		
		**Z, **3	BD45XX2G	180	200	220		
		VDD=VDET-0.2V, VER=0V VD	DET=2.3V~3.1V *2		0.70	2.10		
		VDD=VDET-0.2V, VER=0V VD	DET=2.3V~3.1V	-	0.70	2.85]	
Circuit Current	Inn1	VDD=VDET-0.2V, VER=0V VD	-	0.75	2.25	μΑ		
when ON	IDD1	VDD=VDET-0.2V, VER=0V VD		0.75	3.00			
		VDD=VDET-0.2V, VER=0V VD	DET=4.3V~4.8V %2	•	0.80	2.40]	
		/DD=VDET-0.2V, VER=0V		-	0.80	3.15		
	IDD2	VDD=VDET+0.2V, VER=0V V	DET=2.3V~3.1V ※2	-	0.75	2.25		
		VDD=VDET+0.2V, VER=0V V		0.75	4.28	μΑ		
Circuit Current		VDD=VDET+0.2V, VER=0V V	-	0.80	2.40			
when OFF		VDD=VDET+0.2V, VER=0V VDET=3.2V~4.2V		-	0.80		4.50	
		VDD=VDET+0.2V, VER=0V VDET=4.3V~4.8V %2		-	0.85		2.55	
		VDD=VDET+0.2V, VER=0V VDET=4.3V~4.8V		-	0.85		4.73	
Operating Voltage	VOPL	VoL≦0.4V, RL=470kΩ, Ta=-25~-105°C		0.95	-	<u> </u>	V	
Range	VOFL	VoL≦0.4V, RL=470kΩ, Ta=-40~-25°C		1.20	-	-		
'Low' Output Current	loL	VDS=0.5V, VDD=1.2V		0.4	1.2	-	mA	
(Nch)	IOL	VDS=0.5V, VDD=2.4V		2.0	5.0	-		
Leak Current when OFF	lleak	VDD=VDS=10V ※2			-	0.1	μΑ	
ER Pin 'H' Voltage	VEH	*2			-	-	٧	
ER Pin 'L' Voltage	VEL	*2			-	0.8	V	
ER Pin Input Current	IEL			-	1	10	μА	

VDET(T) : Standard Detection Voltage (2.3V to 4.8V, 0.1V step)

RL: Pull-up resistor to be connected between VouT and power supply.

CL: Capacitor to be connected between VouT and GND.

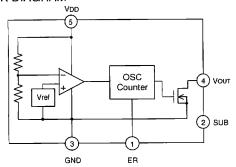
※2 Guarantee is Ta=25°C.

3 tplh:VDD=(VDET(T)-0.5V) \rightarrow (VDET(T)+0.5V)

Attention: Please connect the GND when you don't use 'ER'



OBLOCK DIAGRAM



OPIN NO. , PIN NAME

Pin No.	Pin Name	
1	ER	
2	SUB	
3	GND	
4	Vout	
5	VDD	

NOTE: Substrate Pin should be connected with GND

 $\ensuremath{\,\times\,}$ Please refer to technical note concerning application circuit, and etc.

OSTANDARD DETECTION VOLTAGE AND MARKING

BD45XXXG Series

	BD45XX5G		BD45XX1G		BD45XX	2G
VDET	Product	Marking	Product	Marking	Product	Marking
4.8V	BD45485G	ТО	BD45481G	TS	BD45482G	UJ
4.7V	BD45475G	T1	BD45471G	TT	BD45472G	UK
4.6V	BD45465G	T2	BD45461G	TU	BD45462G	UL
4.5v	BD45455G	Т3	BD45451G	TV	BD45452G	UM
4.4V	BD45445G	T4	BD45441G	TW	BD45442G	UN
4.3V	BD45435G	T5	BD45431G	TX	BD45432G	UP
4.2V	BD45425G	Т6	BD45421G	TY	BD45422G	UQ
4.1V	BD45415G	T7	BD45411G	TZ	BD45412G	UR
4.0V	BD45405G	T8	BD45401G	U0	BD45402G	US
3.9V	BD45395G	T9	BD45391G	U1	BD45392G	UT
3.8V	BD45385G	TA	BD45381G	U2	BD45382G	UU
3.7V	BD45375G	ТВ	BD45371G	U3	BD45372G	UV
3.6V	BD45365G	TC	BD45361G	U4	BD45362G	υw
3.5V	BD45355G	TD	BD45351G	U5	BD45352G	UX
3.4V	BD45345G	TE	BD45341G	U6	BD45342G	UY
3.3V	BD45335G	TF	BD45331G	U7	BD45332G	UZ
3.2V	BD45325G	TG	BD45321G	U8	BD45322G	VO
3.1V	BD45315G	TH	BD45311G	U9	BD45312G	V1
3.0V	BD45305G	TJ	BD45301G	UA	BD45302G	V2
2.9V	BD45295G	TK	BD45291G	UB	BD45292G	V3
2.8V	BD45285G	TL	BD45281G	UC	BD45282G	V4
2.7V	BD45275G	TM	BD45271G	UD	BD45272G	V5
2.6V	BD45265G	TN	BD45261G	UE	BD45262G	V6
2.5V	BD45255G	TP	BD45251G	UF	BD45252G	V7
2.4V	BD45245G	TQ	BD45241G	UG	BD45242G	V8
2.3V	BD45235G	TR	BD45231G	UH	BD45232G	V9



ONOTES FOR USE

1. Absolute maximum range

Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2. GND potential

GND terminal should be a lowest voltage potential every state.

Please make sure all pins which are over ground even if include transient feature.

3. Electrical Characteristics

Be sure to check the electrical characteristics, that is one the tentative specification will be changed by temperature, supply voltage, and external circuit.

4. Bypass Capacitor for Noise Rejection

Please put into the to reject noise between VDD pin and GND. If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point.

5. Short Circuit between Terminal and Soldering

Don't short-circuit between Output pin and VDD pin, Output pin and GND pin, or VDD pin and GND pin. When soldering the IC on circuit board, please be unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

6. Electromagnetic Field

Mal-function may happen when the device is used in the strong electromagnetic field.

- 7. The VDD line inpedance might cause oscillation because of the detection current.
- 8 . A VDD -GND capacitor (as close connection as possible) should be used in high VDD line impedance condition.
- 9. Lower than the minimum input voltage makes the VouT high impedance, and it must be Voo in pull up (Voo) condition.
- 10. BD45XXXG has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If 1MΩ leakage is assumed between the ER terminal and the GND terminal, 100kΩ connection between the ER terminal and the VDD terminal would be recommended. Also, if the leakage is assumed between the VOUT terminal and the GND terminal, the pull up resistor should be less than 1/10 of the assumed leak resistance.

11. External parameters

The recommended parameter range for RL is $50k\Omega \sim 1M\Omega$. When attempting to operate beyond these parameters, be sure to verify the actual operation before continuing use.

12. Power on reset operation

Please note that the power on reset output varies with the Vcc rise up time.

Please verify the actual operation.

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