from Texas Instruments

Unitrode Products

SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

- D Integrated 0.075-Ω Power MOSFET
- D 3 V to 6 V Operation
- D External Analog Control of Fault Current from 0 A to 4 A
- D Independent Analog Control of Current Limit Up to 5 A
- D Fast Overload Protection
- D Unidirectional Switch
- D Minimal External Components
- $D \quad 1\mbox{-}\mu\mbox{A I}_{CC}$ When Disabled
- D Programmable On Time
- D Programmable Start Delay
- D Fixed 3% Duty Cycle

description

The UCC3918 low on-resistance hot swap power manager provides complete power management, hot swap capability, and circuit breaker functions. The only components needed to operate the device, other than supply bypassing, are a timing capacitor, and two programming resistors. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 3% duty cycle ratio limits the average output power. The IFAULT pin allows linear programming of the fault level current from 0 A to 4 A.

Fast overload protection is accomplished by an additional overload comparator. Its threshold is internally set above the maximum sourcing current limit setting. In the event of a short circuit or extreme current condition, this comparator is tripped, shutting down the output. This function is needed since the maximum sourcing current limit loop has a finite bandwidth.



Pin 5 serves as the lowest impedance to the electrical ground. Pins 4, 12, and 13, serve as heat sink/ground. These pins should be connected to large etch PCB areas to help dissipate heat. For N package, pins 4, 12, and 13, are NC.



Pin 9 serves as the lowest impedance to the electrical ground. Pins 5, 6, 7, 8, 16, 17, 18, 19, and 20 serve as heat sink/ground.

When the output current is below the fault level, the output MOSFET is switched on with a nominal resistance of 0.075 Ω . When the output current exceeds the fault level or the maximum sourcing level, the output remains on, but the fault timer starts charging a capacitor connected to the CT pin (C_T). Once C_T charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

The UCC3918 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI terminitation power (Termpwr). The UCC3918 can also be put into the sleep mode, drawing only 1 μ A of supply current.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

description (continued)

Other features include an open-drain fault output indicator, thermal shutdown, undervoltage lockout, 3 V to 6 V operation, and a low thermal resistance small-outline power package.

functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)^{†}}

Input Voltage	8 V
SOIC Power dissipation	2.5 W
Fault output sink current	50 mA
Fault output voltage	VIN
Output Current (dc)	. Internally Limited
Input Voltage SHTDWN, IFAULT, IMAX	0.3 V to VIN
Storage temperature range T _{stg}	65_C to 150_C
Operating virtual junction temperature Tj	55_C to 150_C
Lead temperature (soldering, 10 seconds)	300_C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500 µs. Consult *Packaging Section* of Databook for thermal limitations and considerations of package.



SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Section						
Voltage input range, VIN		3	5	6	V	
VDD supply current	No load		1	2	mA	
Sleep mode current	SHTDWN = 0.2 V		0.5	5	μΑ	
Output Section	·					
R _{DS(on)}	$I_{OUT} = 1 \text{ A to 4 A}, \text{VIN} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$		0.075	0.095	Ω	
	$I_{OUT} = 1 \text{ A to } 4 \text{ A}, \text{VIN} = 3 \text{ V}, T_{A} = 25^{\circ}\text{C}$		0.09	0.116	Ω	
	$I_{OUT} = 1 \text{ A to } 4 \text{ A}, \qquad \text{VIN} = 5 \text{ V}$		0.075	0.125	Ω	
	$I_{OUT} = 1A \text{ to } 4A, \qquad VIN = 3 \text{ V}$		0.09	0.154	Ω	
Reverse leakage current	$\overline{\text{SHTDWN}} = 0 \text{ V}, \text{VIN} = 0 \text{ V} \text{V}_{\text{OUT}} = 5 \text{ V}$			20	μΑ	
Initial startup time	See Note 1		100		μS	
Thermal shutdown	See Note 1		170		_C	
Thermal hysteresis	See Note 1		10		_C	
Output leakage	SHTDWN = 0.2 V			20	μΑ	
	$R_{IFAULT} = 105 \text{ k}\Omega$	0.75	1	1.25	А	
	$R_{IFAULT} = 52.3 \text{ k}\Omega$	1.7	2	2.3	А	
Trip current	$R_{IFAULT} = 34.8 \text{ k}\Omega$	2.5	3	3.5	А	
	$R_{IFAULT} = 25.5 \text{ k}\Omega$	3.3	4	4.7	А	
Maximum output current	R _{IMAX} = 118 kΩ	0.3	1	1.7	А	
	$R_{IMAX} = 60.4 \text{ k}\Omega$	1	2	3	А	
	R _{IMAX} = 42.2 kΩ	2	3	4	А	
	R _{IMAX} = 33.2 kΩ	2.5	3.8	5.1	А	
	R _{IMAX} = 27.4 kΩ	3.0	4.6	6.2	А	
Fault Section						
C _T charge current	V _{CT} = 1 V	-50	-36	-22	μΑ	
C _T discharge current	$V_{CT} = 1 V$	0.5	1.2	2.0	μΑ	
Output duty cycle	VOUT = 0 V	1.5	3	6	%	
C _T fault threshold		0.8	1.3	1.8	V	
C _T reset threshold		0.25	0.5	0.75	V	
Shutdown Section						
Shutdown threshold		1.1	1.5	2.0	V	
Shutdown hysteresis			100		mV	
Input low current	SHTDWN = 0V	-500	0	500	nA	
Input high current	SHTDWN = 2V	-2	-1	-0.5	μA	
Open Drain Fault Output Section						
High level output current				1	μΑ	
Low level output voltage	I _{OUT} = 1mA		0.4	0.9	V	

electrical characteristics at $T_A = 0^{\circ}C$ to $70^{\circ}C$, VIN = 5 V, $R_{IMAX} = 42.2 \text{ k}\Omega$, $R_{IFAULT} = 52.3 \text{ k}\Omega$, SHTDWN = 2.4 V, $T_A = T_J$ (unless otherwise noted)

NOTE 1: Ensured by design. Not production tested.



SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

pin descriptions

CT: A capacitor connected to this pin sets the maximum fault time. The maximum time must be greater than the time to charge external load capacitance. The nominal fault time is defined as:

$$T_{FAULT} = 22.2 \times 10^3 \times C_T$$
⁽¹⁾

Once the fault time is reached the output shuts down for a time given by:

$$T_{SD} = 0.667 \times 10^6 \times C_T$$
 (2)

This equates to a 3% duty cycle. The recommended minimum value for the C_T capacitor is 0.1 μ F.

FAULT: Open-drain output, which pulls low on any condition that causes the output to open; Fault, Thermal Shutdown, Shutdown, and maximum sourcing current greater than the fault time.

GND: This is the most negative voltage in the circuit. All 4 ground pins should be used, and properly heat sunk on the PCB.

IFAULT: A resistor connected from this pin to ground sets the fault threshold. The resistor versus fault current is set by the formula

$$R_{\mathsf{FAULT}} = \frac{105 \text{ k}\Omega}{^{\mathsf{I}}\mathsf{TRIP}}$$
(3)

IMAX: A resistor connected from this pin to ground sets the maximum sourcing current. The resistor vs the output sourcing current is set by the formula:

$$R_{\text{IMAX}} = \frac{126 \text{ k}\Omega}{\text{Maximum Sourcing Current}}$$
(4)

SHTDWN: When this pin is brought low, the IC is put into sleep mode. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: This is the input voltage to the UCC3918. The recommended operating voltage range is 3V to 6V. All VIN pins should be connected together and to the power source.

(5)

VOUT: Output voltage for the circuit breaker. When switched the output voltage will be approximately:

 $V_{OUT} = V_{IN} - 0.075\Omega \times I_{OUT}$

All VOUT pins should be connected together and to the load.



SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

APPLICATION INFORMATION



Figure 1. Typical Application

protecting the UCC3918 from voltage transients

The parasitic inductance associated with the power distribution can cause a voltage spike at V_{IN} if the load current is suddenly interrupted by the UCC3918. *It is important to limit the peak of this spike to less than 6 V to prevent damage to the UCC3918.* This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive "+" and negative "-" leads of the power supply feeding V_{IN}, locate the power supply close to the UCC3918 or use a PCB ground plane).
- Decoupling V_{IN} with a capacitor, C_{IN} (refer to Figure 1), located close to the VIN pin. This capacitor is typically less than 1 μF to limit the inrush current.
- Clamping the voltage at V_{IN} below 6 V with a Zener diode, D1 (refer to Figure 1), located close to the VIN pin.

estimating maximum load capacitance

For circuit breaker applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited circuit breaker, the output comes up if the load requires less than the maximum available short-circuit current.

To ensure recovery of a duty-cycle of the current-limited circuit breaker from a short-circuited load condition, there is a maximum total output capacitance that can be charged for a given unit ON time (fault time). The design value of ON or fault time can be adjusted by changing the timing capacitor C_T .



SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

APPLICATION INFORMATION

estimating maximum load capacitance

For worst-case constant-current load of value just less than the trip limit; C_{OUT(max)} can be estimated from:

$$C_{OUT(max)} = \left(I_{MAX} - I_{LOAD}\right) \left(\frac{22 \times 10^3 \times C_T}{V_{OUT}}\right)$$
(6)

Where V_{OUT} is the output voltage and I_{MAX} is the maximum sourcing current.

For a resistive load of value R_{LOAD} , the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} = \left(\frac{22 \times 10^{3} \times C_{T}}{R_{LOAD} \times \ell n \left(\frac{1}{1 - \frac{VOUT}{I_{MAX} \times R_{LOAD}}}\right)}\right)$$

(7)

UDG-97071



Figure 2. Load Curent, Timing Capacitor Voltage and Output Voltage of the UCC3918 Under Fault



SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

TYPICAL CHARACTERISTICS





SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

TYPICAL CHARACTERISTICS





SLUS384B - NOVEMBER 1999 - REVISED JUNE 2000

APPLICATION INFORMATION

safety considerations

Although the UCC3918 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3918 is intended for use in safety critical applications where UL[®] or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3918 prevents the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated