High-Efficiency Integrated Dimming LED Lighting Controller

Check for Samples: TPS92070

FEATURES

- **Advanced Integrated Dimming Interface**
- **Non-Dissipative TRIAC Dimmer Management**
- **Lamp-to-Lamp Uniformity During Dimming**
- **No Low-Frequency Photometric Ripple**
- **Exponential Dimming Profile**
- **Innovative Secondary-Side Feedback Eliminates Optocoupler Devices**
- **LED Current Regulation better than 5%**
- **Programmable Minimum LED Current**
- **Valley Switching and DCM Operation for Reduced EMI and Improved Efficiency**
- **Leading Edge Dimmer Detection**
- **Power Factor > 0.8**
- **Cycle-by-Cycle Current Limit Protection**
- **Low Start-Up and Standby Currents**
- **Integrated PWM MOSFET Driver**
- **Thermal Shutdown**
- **16-Pin, TSSOP package**

APPLICATIONS

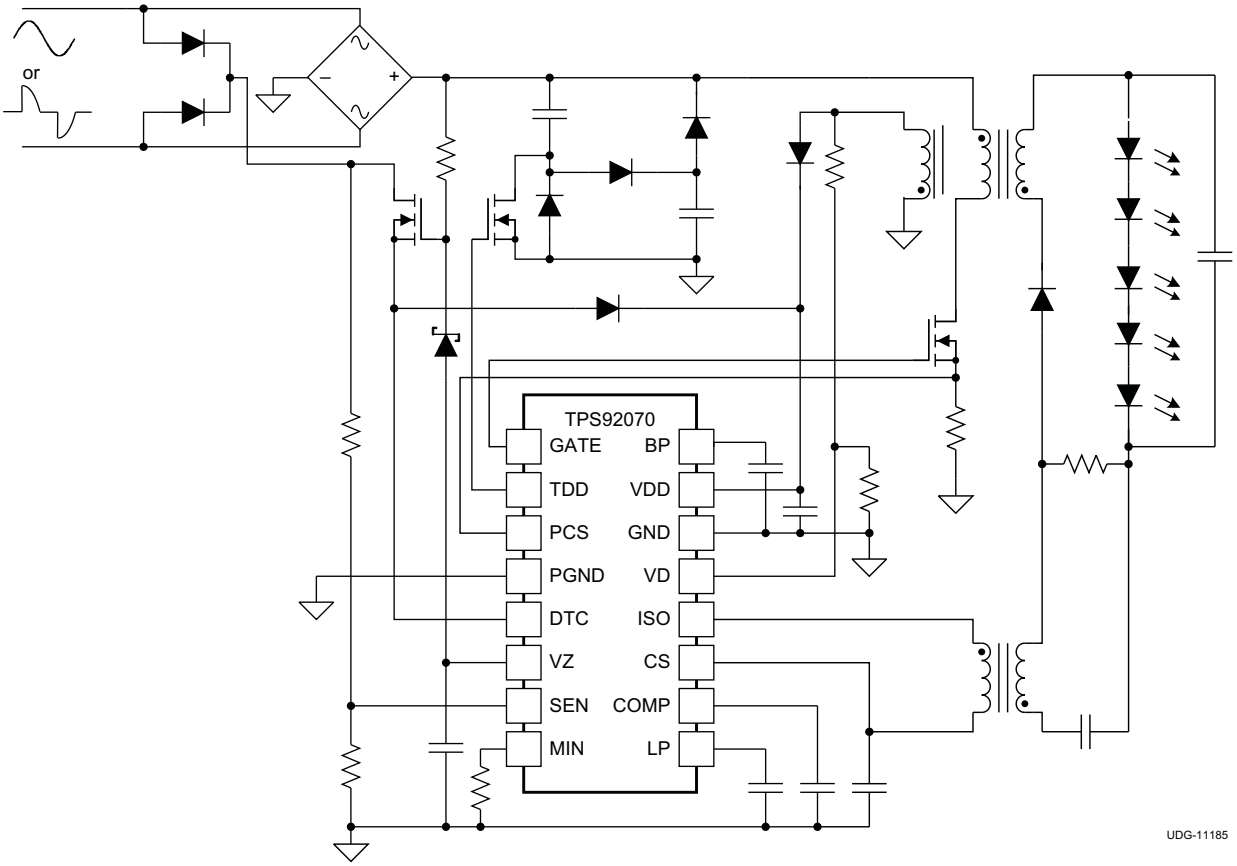
- **LED Light Bulb Replacement**
- **LED Luminaires**
- **LED Downlights**
- **LED Wall Washers**

DESCRIPTION

The TPS92070 is an advanced PWM controller ideal for use in low-power, offline, LED lighting applications. The integrated dimming interface circuit of the TPS92070 features a non-dissipative dimmer trigger control circuit. The TPS92070 controller provides DC LED current with no photometric ripple effects. The DC current also results in higher efficacy of the LEDs. The TPS92070 provides exponentially controlled light output based on the external dimmer position. High power factor is achieved with a valley fill circuit. Once a leading-edge dimmer is detected, the TPS92070 sets an output to disable the PFC circuit and thus optimizes driver operation. The LED current sense precision error amplifier implements deep dimming. The TPS92070 current sensing scheme provides tight current regulation and eliminates the need for an optocoupler. The tight current regulation allows for strong color and intensity matching amongst individual bulbs or luminaires.

The TPS92070 also contains a variety of protection features including cycle-by-cycle peak-current limit, overcurrent protection, open-LED (output overvoltage) protection, undervoltage lockout, and thermal shutdown.

APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

TEMPERATURE RANGE (T_J)	PACKAGE	PINS	TRANSPORT MATERIAL	UNITS	ORDERABLE NUMBER
–40°C to 140°C	Plastic TSSOP	16	Tube	70	TPS92070PW
			Tape and Reel	2000	TPS92070PWR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

All voltages are with respect to GND, –40°C < T_J = T_A < 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted)

			VALUE		UNITS
			MIN	MAX	
Supply voltage	VDD(4)		–0.3	25.0	
Input voltages	ISO, CS, COMP, LP, MIN, SEN, PCS		–0.3	7.0	
	BP, GATE, TDD		–0.3	7.2	
	VD		–1.4	7.0	
	VZ, DTC(5)		–0.3	20.0	
Input current	VZ (pulse < 1 ms)			5	mA
	BP		–0.5	0	
	DTC	Peak		30	
		Average		16	
	VDD			5	
Operating junction temperature(6)			–40	140	°C
Storage temperature(6)			–65	150	°C
Lead temperature (10 seconds)				260	°C

(1) These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) VDD clamped at approximately 23 V. See ELECTRICAL CHARACTERISTICS table.
(5) VZ clamped at approximately 12.5 V. See ELECTRICAL CHARACTERISTICS table.
(6) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, all voltages are with respect to GND, –40°C < T_J = T_A < 125°C.

		MIN	TYP	MAX	UNIT
VDD	Input Voltage	9		21.5	V
VZ	Current	1		100	µA
R_{MIN}	Resistor from MIN to GND (1)	25		75	kΩ
R_{VD1}	Valley detect resistor from AUX winding to VD pin	50		200	kΩ
C_{VZ}	VZ bypass capacitor	1		4.7	nF
C_{BP}	BP capacitor	0.47	1		µF
C_{VDD}	VDD capacitor	10×C_{BP7}	4.7		µF
$C_{VDD,BP}$	VDD bypass capacitor, ceramic(2)	0.1			µF

(1) R_{MIN} values greater than 75K will produce lower minimum current values. However accuracy of the minimum current will degrade, and there may be flickering at very low values of Imin.
(2) If a ceramic capacitor is used for C_{VDD} then this capacitor is not needed.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MAX	UNIT
ESD Rating, Human Body Model (HBM)	1.5	kV
ESD Rating, Charged Device Model (CDM)	500	V

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, −40°C < T_A < 125°C, T_J = T_A, V_{VDD} = 12 V, GND =0 V, I_{VZ} = 50 µA, R_{MIN} = 71.5 kΩ, C_{VDD} = 4.7µF, C_{BP} = 1 µF, C_{LP} = 220nF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS and STARTUP						
I_{START}	VZ startup current	V_{VDD} = 7 V, Measured I_{VZ}		1.0	10	µA
V_{VZ}	VZ voltage	V_{VDD} = 7 V, 15 µA < I_{VZ} < 100 µA	11.5	12.5	13.5	V
I_{VDD}	VDD startup current	V_{VDD} = 7.5 V		134	240	µA
	Standby current	V_{LP} = 0 V, V_{SEN} = 0 V		750	1500	
	Switching current	fG_{ATE} = 138 kHz, GATE – unloaded		1880	2500	
$V_{VDD(uvlo)}$	VDD UVLO threshold	Measured at VDD (falling)	7	7.88	8.4	V
$V_{VDD(ovp)}$	VDD clamp and OVP	Measured at VDD (rising)	21.5	23.5	25	V
$R_{VZ(ovp)}$	OVP VZ discharge resistance	V_{VDD} = $V_{VDD(ovp)}$, VZ = 3 V		4.8		kΩ
V_{BP}	BP Regulation voltage	9 V < V_{VDD} < 19V, I_{BP} = –0 µA	6.7	7	7.2	V
DIMMER TRIGGER CIRCUIT						
$V_{SEN(hi)}$	Dimmer sense thresholds	Measured at SEN (rising)	4.75	5	5.25	V
$V_{SEN(lo)}$		Measured at SEN (falling)	0.9	1	1.10	
$V_{SEN(clamp)}$	SEN Clamp voltage	I_{SEN} = 100 µA	5.75	6	6.25	V
$I_{DTC(lkg)}$	DTC to PGND leakage current	V_{DTC} = 12 V, V_{SEN} > $V_{SEN(hi)}$		40	100	nA
$R_{DTC(pgnd)}$	DTC to PGND resistance	V_{DTC} = 3 V, V_{SEN} (falling), $V_{SEN(lo)}$ < V_{SEN} < $V_{SEN(hi)}$	16	20	25	kΩ
		V_{DTC} = 3 V, V_{SEN} (rising), V_{SEN} < $V_{SEN(hi)}$	100	156	300	Ω
		V_{SEN} < $V_{SEN(lo)}$	100	156	300	Ω
CURRENT SETPOINT						
V_{MIN}	MIN regulation voltage			2.5		
$R_{OUT(lp)}$	LP output resistance			500		kΩ
$V_{OH(lp)}$	LP Maximum voltage level	V_{SEN} = 6 V, I_{LP} = 0 µA	2.9	3	3.1	V
$V_{OL(lp)}$	LP Minimum voltage level	V_{SEN} = 0 V, I_{LP} = 0 µA	–0.025	0	0.025	V

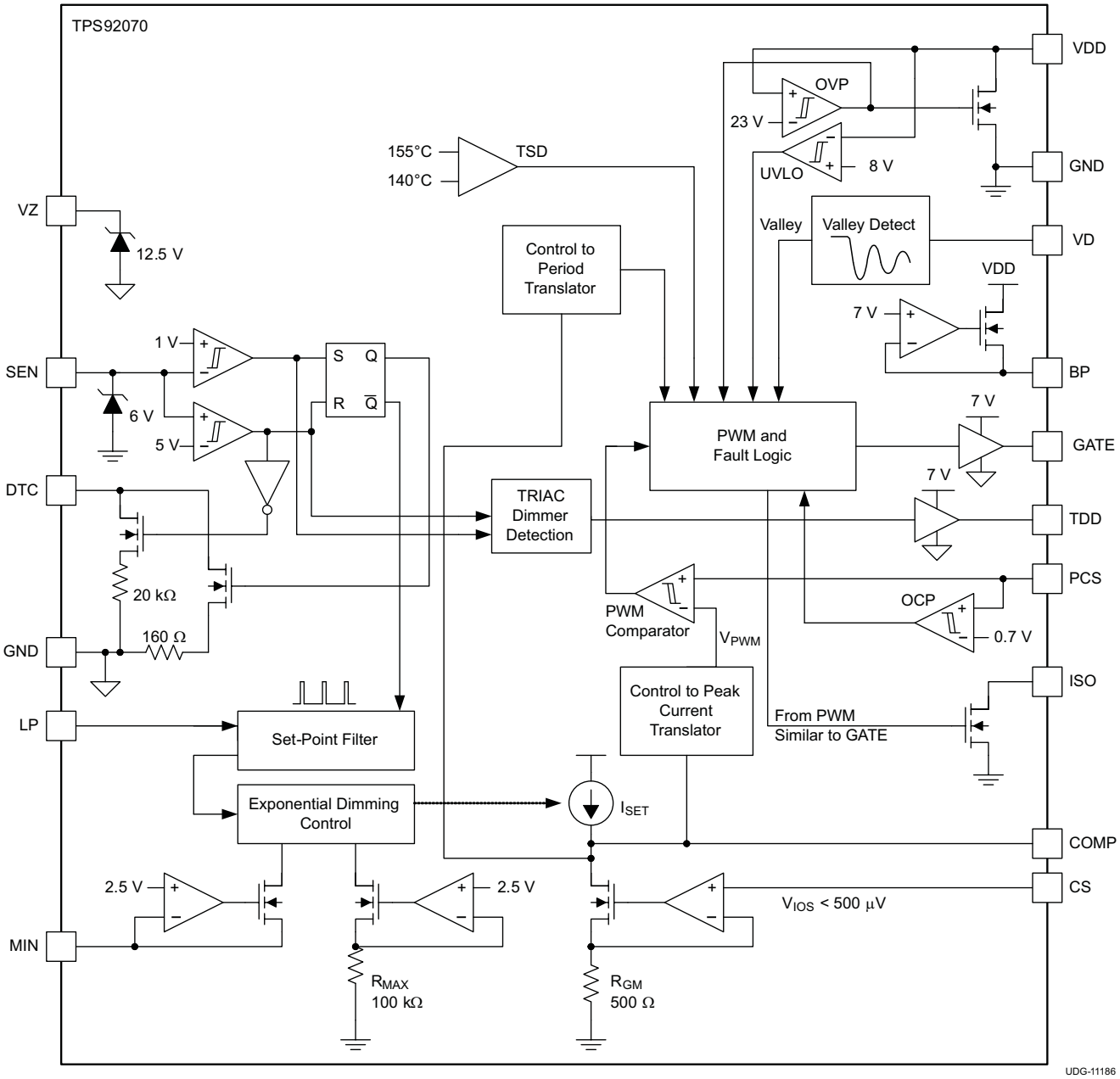
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, −40°C < T_A < 125°C, T_J = T_A, V_{VDD} = 12 V, GND =0 V, I_{VZ} = 50 µA, R_{MIN} = 71.5 kΩ, C_{VDD} = 4.7µF, C_{BP} = 1 µF, C_{LP} = 220nF

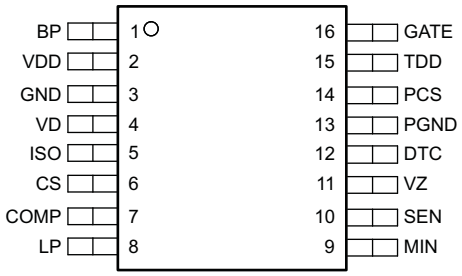
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
V_{IOS}	Input offset voltage	5 mV < V_{CS} < 100 mV, V_{COMP} = 3 V		±500		µV
$V_{COMP(min)}$	Minimum COMP clamp voltage	V_{CS} = 150 mV, V_{LP} < 3 V	1.45	1.53	1.60	V
$V_{COMP(max)}$	Maximum COMP clamp voltage	V_{CS} < 100 mV, V_{LP} > 2.1 V	3.6	3.7	3.8	V
$V_{CS(min)}$	Minimum CS reference voltage	V_{LP} = 0, R_{MIN} = 71.5 kΩ, T_A = 25°C	2.835	3.15	3.465	mV
$V_{CS(max)}$	Maximum CS reference voltage	V_{LP} > 2.1 V, T_A = 25°C	97	100	103	mV
MODULATION						
$f_{CLAMP(max)}$	Maximum frequency clamp	Measured at GATE, V_{COMP} = 3.5 V, T_A = 25°C	132	138	146	kHz
$f_{CLAMP(min)}$	Minimum frequency clamp	Measure at GATE, V_{COMP} = 1.53 V, V_{VD} = 0 V, T_A = 25°C	10	20	30	kHz
VALLEY DETECT						
VD_{CLAMP}	VD clamp	Measured when GATE is high, I_{VD} = –15 µA		–560		mV
		Measured when GATE is low and VD is falling		–125		mV
$V_{VD(en)}$	VD enable threshold	Minimum peak of resonant valley, V_{COMP} = 1.8 V	600			mV
$V_{VD(zc)}$	Zero-crossing detect threshold	Measured at VD (falling)	80	100	135	mV
$t_{VD(vw)}$	Valley wait timer	V_{COMP} > V_{MINF_DET}, V_{VD} = 0 V, wait time for next PWM pulse with zero-crossing detected	10	12.7	14	µs
$I_{VD(min)}$	Current required for valley detection		–50			µA
OVERCURRENT PROTECTION						
$V_{PCS(oc)}$	Over current limit	Measure at PCS (rising), V_{COMP} = 4 V	670	700	750	mV
$t_{PCS\_G1(oc)}$	Propagation delay	Measured between PCS and GATE falling	10	64	190	ns
PWM COMPARATOR						
t_{LEB}	Leading edge blanking	Measured at GATE, V_{COMP} = 3.5 V	180	220	300	ns
$V_{PWM(max)}$	PWM thresholds	V_{COMP} = $V_{COMP(max)}$		600	650	mV
V_{PWM}		V_{COMP} = 3.5 V	460	500	550	mV
$V_{PWM(min)}$		Measured at PCS rising, COMP ≤ 2 V	40	65	80	mV
$t_{PCS\_G1(cl)}$	Propagation delay	Measured between PCS and GATE falling	10	54	120	ns
LED ISOLATED CURRENT SENSE						
$R_{ISO(pd)}$	Pull down resistance	GATE is high	240	270	350	Ω
PWM OUTPUTS						
$V_{GATE(oh)}$	Output voltage high	Measured at GATE	6.7	7	7.2	V
$V_{GATE(ol)}$	Output voltage low		–0.01	0	0.01	V
$t_{FALL(pwm)}$	Fall time	C_{GATE} = 1 nF, T_A = 25°C		43	70	ns
$t_{RISE(pwm)}$	Rise time	CG_{ATE} = 1 nF, T_A = 25°C		105	155	ns
TRIAC DIMMER DETECTION						
$V_{TDD(oh)}$	Output voltage high	Measured at TDD	6.7	7	7.2	V
$V_{TDD(ol)}$	Output voltage low		–0.01	0	0.01	V
$t_{FALL(tdd)}$	Fall time	C_{TDD} = 1 nF		120	190	ns
$t_{RISE(tdd)}$	Rise time	C_{TDD} = 1 nF		130	220	ns
$t_{DLY\_1V\_5V}$	Minimum delay from 1V to 5V SEN signal transitions for no dimmer detection		105	135	170	µs

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



TPS92070
PW (TSSOP) PACKAGE
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
BP	1	Connect a 1-uF ceramic capacitor to GND to bypass the internal voltage regulator.
COMP	7	Loop compensation output. Connect the loop compensation components between this pin and GND
CS	6	LED current sense feedback and positive input terminal of the error amplifier.
DTC	12	Dimmer trigger control input. Connect this pin to thesource of the HV N-channel MOSFET cascode device of the DTC circuit.
GATE	16	PWM drive signal output. Connect to flyback power MOSFET.
GND	3	Ground for internal circuitry
ISO	5	Inverting input of secondary side current sense comparator and isolation transformer buffer. Connect to GND for non-isolated applications.
LP	8	Pole for DTC low pass filter. Connect a capacitor to GND to set the response time of the dimming level detection circuit.
MIN	9	Minimum current programming input. Connect a resistor to GND to set the minimum LED current.
PCS	14	Primary current sense input. Connected to shunt resistor for primary side current sense.
PGND	13	Power ground for GATE Driver. Connected to GND (1)
SEN	10	Dimmer sense input. An internal window comparator continuously monitors this pin to determine the dimmer setting.
TDD	15	TRIAC dimmer detect. Drives bypass FET in Valley Fill PFC when dimmer is detected. For non PFC applications, leave this pin open
VD	4	Valley detect input. Connect to the Aux winding through a resistor divider.
VDD	2	Provides power to the device. Connect a bypass capacitor directly to GND. See RECOMMENDED OPERATING CONDITIONS for suggested values.
VZ	11	Voltage clamp. This pin clamps the maximum voltage on the gate of the external HV DTC N-channel MOSFET.

(1) See Application Section for layout recommendations

TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤+125°C, V_{VDD} = 12 V, GND =0V, I_{VZ} = 50 µA, R_{MIN} = 71.5 kΩ, C_{VDD} = 10 µF, C_{VZ} = 1 nF, C_{LP} = 220 nF

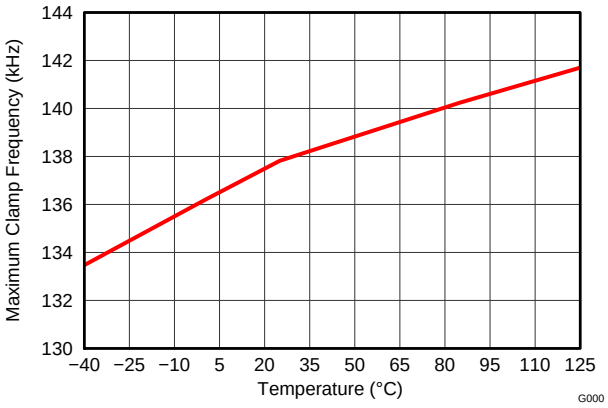


Figure 1. Maximum Clamp Frequency vs. Temperature

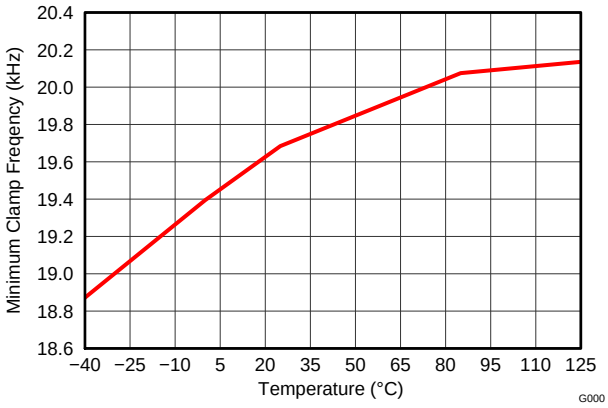


Figure 2. Minimum Clamp Frequency vs. Temperature

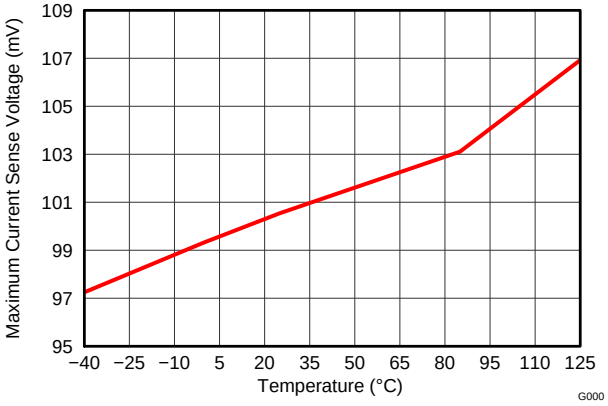


Figure 3. Maximum Current Sense Voltage vs. Temperature

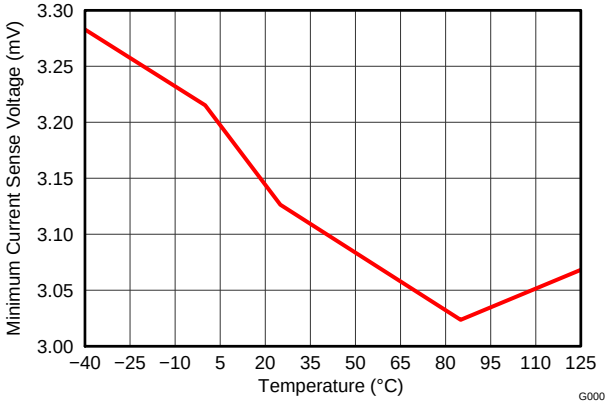


Figure 4. Minimum Current Sense Voltage vs. Temperature

APPLICATIONS

STARTUP BIAS AND UVLO

During powerup when VDD is less than the UVLO threshold of 8 V, the VZ pin is trickle charged with $I_{VZ(start)}$ of approximately 10 µA through the startup-resistor connected to the bulk rectified voltage. As VZ is being charged, VDD tracks VZ (less V_{GSTH}) through the external cascode HV MOSFET (Q1) supplying a VDD startup current of 135 µA. Once VZ reaches the TPS92070 zener clamp regulation level of 12.5 V, the device enters into a stand-by mode during which the dimmer trigger circuit (DTC), set-point filter, 7-V bias regulator, and a minimal amount of housekeeping circuitry is active. The TPS92070 remains in this state until the SEN pin exceeds 5 V indicating that adequate line voltage is present, either through TRIAC firing, or line voltage presence. The typical start-up waveforms are shown in Figure 5.

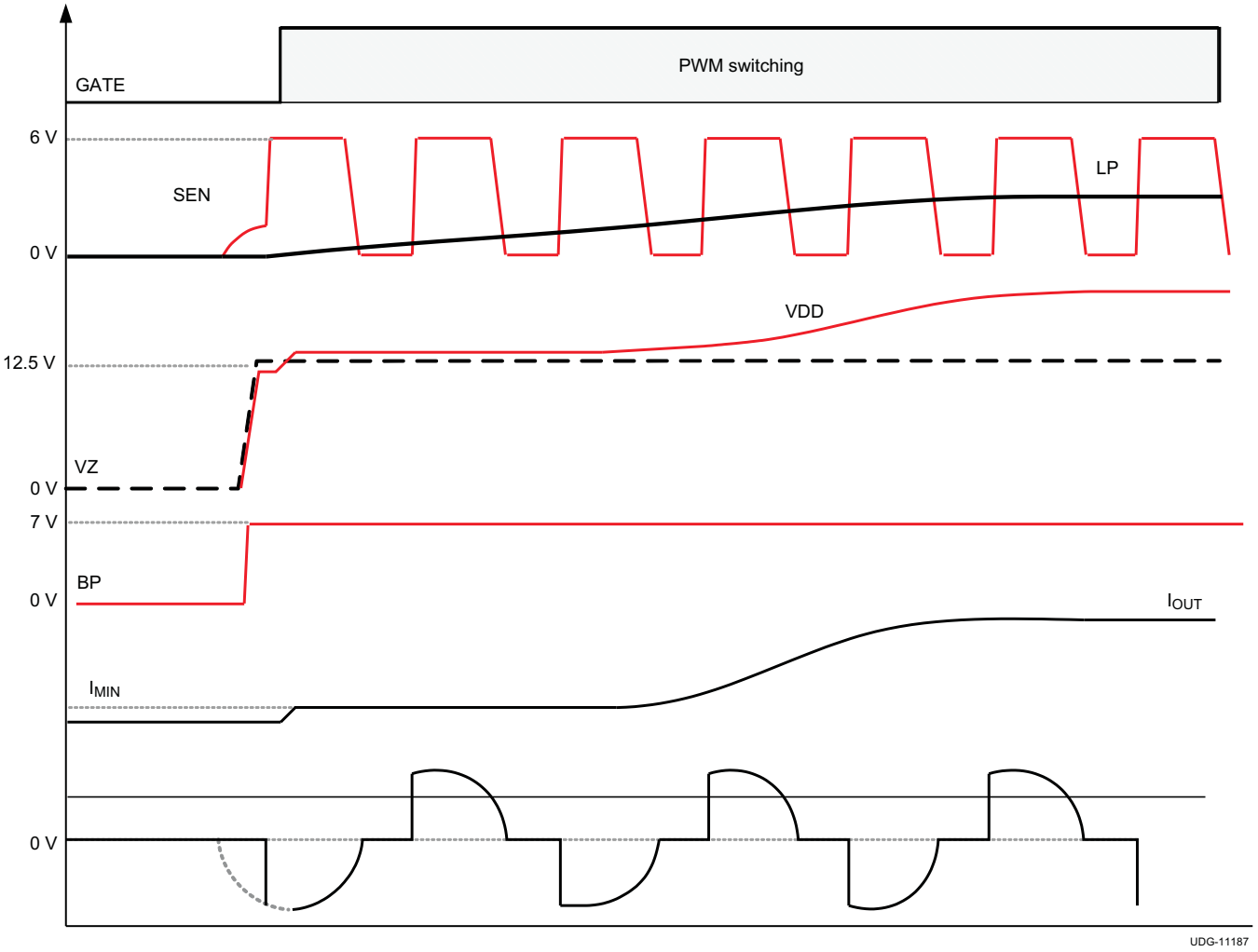


Figure 5. Typical Startup Waveforms for a TRIAC Triggered $V_{IN(ac)}$ Input

DTC and PHASE DETECTION

The DTC pin is a current sink which loads the dimmer with approximately 20 mA during the zero-crossing of the AC line to ensure that the TRIAC is reliably triggered. This current sink is switched on when the voltage on the SEN pin is below 5 V. The setpoint filter in conjunction with the SEN and LP pins is used to determine the firing angle of the TRIAC dimmer (if any) connected to the input of the LED driver. An internal window comparator monitors the SEN (dimmer sense input) pin and the resulting duty-cycle is transformed into a voltage at the LP pin using the LP filter. The relation between the TRIAC firing angle and the LP voltage is shown in Figure 6. It illlllustrates the conversion of the TRIAC firing angle to LP voltage and exponential dimming control of I_{SET} based on internal control voltage. As the voltage on the LP varies from 0 V to 3 V based on the mapping of 0% to 100% SEN duty-cycle, an internal control voltage is linearly modulated by TPS92070 from 400 mV to 200 mV.

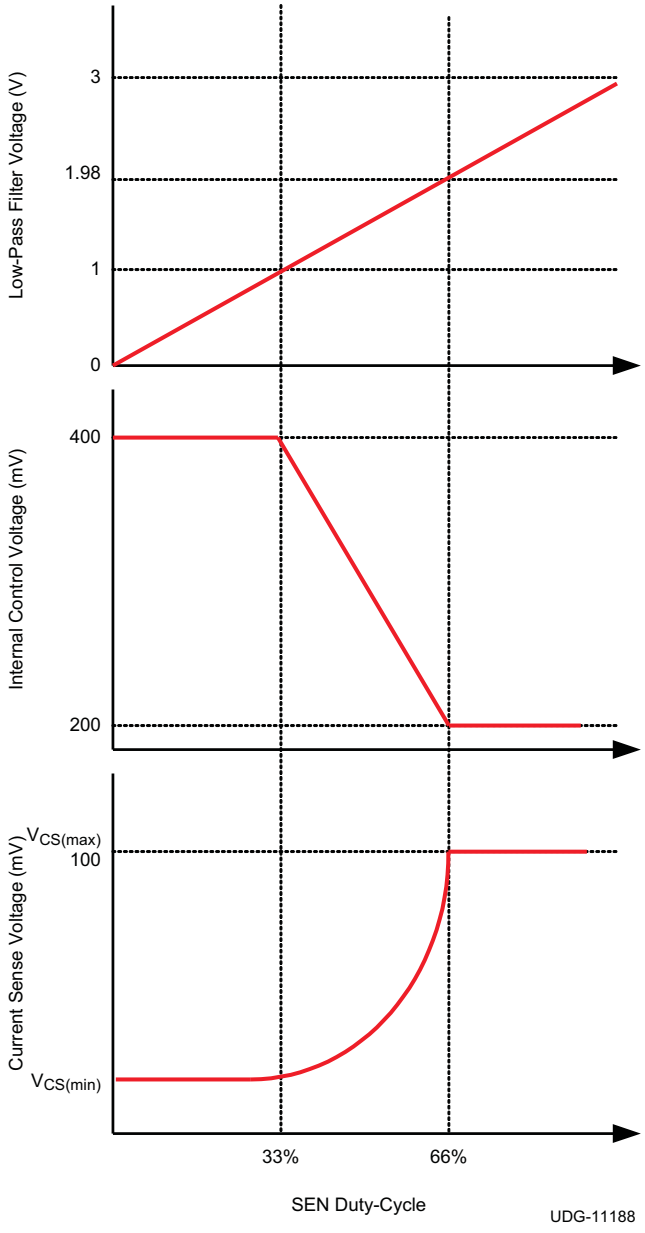


Figure 6. TRIAC Firing Angle vs. Low-Pass Filter Voltage

The internal control voltage, V_{CTRL} is clamped to 0.4 V for LP < 1 V and clamped to 0.2 V for LP > 1.98V . As the control voltage is linearly modulated between 0.4 V and 0.2 V, the current sense reference voltage V_{CS} is exponentially controlled between the pre-set maximum of 100 mV and the externally programmed minimum limit of V_{CS_MiN}. The current setpoint level, V_{CS_MiN} is programmed by R_{MIN}.

$$V_{CS(min)} = \frac{225}{R_{MIN}} \quad (1)$$

The exponential control of the set-point current extends the dimming control range and enables up to two decades of LED current-programming between the $V_{CS(min)}$ and $V_{CS(max)}$ = 100 mV levels.

LED CURRENT SENSE

The secondary-side LED current is sensed using the CS pin and tightly regulated using the low-offset (500 µV) transconductance amplifier. The transconductance (g_M) of the amplifier is internally set to approximately g_M = 1/500 S. In the direct current-sense mode (non-isolated), the ISO pin is connected to GND. In the isolated-mode, the secondary-side LED current is sensed using a small transformer with the secondary of the transformer connected between CS and ISO pins as shown in Figure 7. The ISO pin has a switched pull-down resistance of 270 Ω.

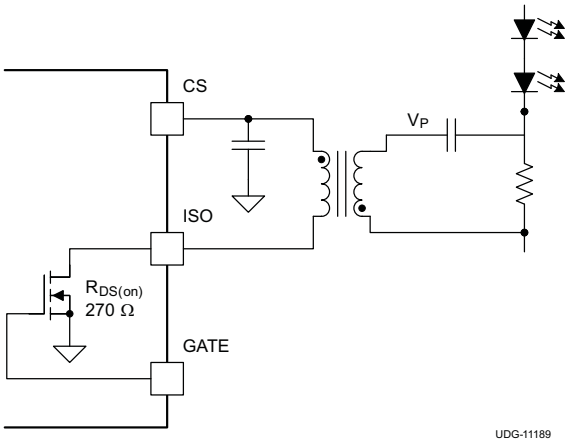


Figure 7. Isolated Current Sense

MODULATION

The internal I_{SET} current and RGM sets a reference input for the transconductance current sense amplifier which controls the voltage on the COMP pin. The COMP pin is used for loop compensation. The voltage on the COMP pin modulates the peak of the primary current and the switching frequency (frequency modulation) of the flyback converter. The modulation on the primary current and the switching frequency are shown in Figure 8. The peak of the primary current is modulated by varying the threshold on the PWM comparator. The threshold is modulated from 0.6 V to 0.065 V while the switching frequency varies between 20 kHz and 138 kHz as COMP pin varies from 3.7 V to 2.6 V. The maximum COMP pin voltage is clamped at 3.7 V allowing the maximum cycle-by-cycle peak current limit PWM threshold to be 0.6 V. The switching frequency is linearly modulated from 138 kHz to 20 kHz with the PWM threshold clamped at 0.065 V as the COMP pin varies from 2.6 V to 1.63 V. The minimum frequency is clamped at 20 kHz and TPS92070 enters the minimum frequency detect state for COMP <1.6 V. The minimum voltage on the COMP is clamped at 1.53 V. The PWM threshold is related to the COMP pin voltage as shown in Equation 2 and Equation 3.

For $2.6 \le V_{COMP} \le 3.7$,

$$V_{PWM} = \frac{V_{COMP} - 2.5}{2} \quad (2)$$

For $V_{COMP} < 2.6$ V,

$$V_{PWM} = 0.065 \quad (3)$$

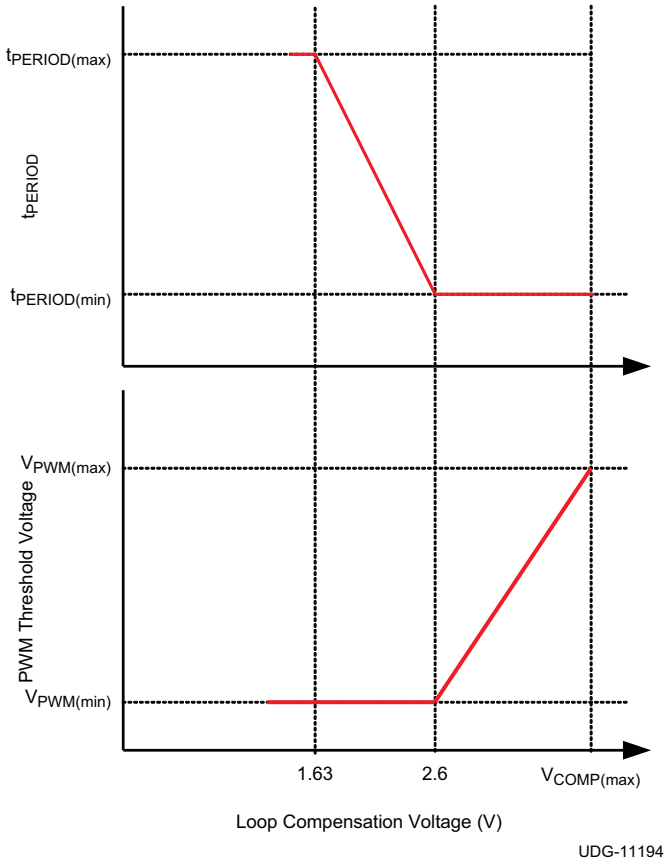


Figure 8. Switching Period and PWM Threshold Modulation Based on COMP pin Voltage

PRIMARY CURRENT SENSE

The primary current is sensed by monitoring the voltage developed across an external current-sense resistor connected between the source of the external HV MOSFET and PGND. The PCS pin is used for monitoring the voltage and it is then compared with the PWM threshold (V_{PWM}). The PWM comparator has a leading-edge blanking time of 220 ns to avoid any false-tripping of the comparator due to capacitive charge spikes on the PCS pin. The GATE output is pulled low once the PCS pin reaches the PWM threshold.

VALLEY DETECT

TPS92070 ensures that the flyback converter always operates in either DCM or QR mode of operation and initiates a new PWM switching cycle only after the energy in the flyback transformer is completely reset to zero. This is accomplished by monitoring the auxiliary winding waveform using a resistive divider connected to the VD pin. The TPS92070 initiates a new switching cycle based on the following conditions:

- For normal operation with 1.63 V ≤ V_{COMP} ≤ 3.7 V, a new PWM switching cycle is initiated when the internal timer t_{PERIOD} has expired and the next valley is detected. The VD pin must go below 100 mV ($V_{VD(zc)}$) prior to valley detection to enable the valley detector circuit.
- In the minimum frequency clamp state when V_{COMP} < 1.63 V, the switching period is fixed at $t_{PERIOD(max)}$ (corresponding to $f_{CLAMP(min)}$) and the valley detector is disabled.
- The relationship of t_{PERIOD} to the switching frequency is shown in Equation 4 and Equation 5.

$$f_{CLAMP(max)} = \frac{1}{t_{PERIOD(min)}} \quad (4)$$

$$f_{CLAMP(min)} = \frac{1}{t_{PERIOD(max)}} \quad (5)$$

By turning on the flyback power switch at the resonant valley, the switching losses are reduced thereby enabling higher efficiency. The voltage at the VD pin is clamped at –0.56 V during the negative excursions on the AUX winding when GATE is high. When GATE is low and during the resonant valley detection, the VD pin is clamped at –0.2 V. The interface to the VD pin to the AUX winding is shown in Figure 9. The TPS92070 requires that the positive peak of the resonant ring at the VD pin is higher than 0.6 V ($V_{VD(en)}$) to ensure that the valley-detect circuit is enabled for detection on the falling edge when V_{COMP} > 1.63 V. Hence, R_{VD2} need to be selected in such a way that this condition is met for all AUX voltages when V_{COMP} > 1.63 V. A current $I_{VD(min)}$ of at least 50 µA must be drawn from the VD pin when the GATE is high to ensure proper valley detection. This requirement determines the value of R_{VD1}. The waveforms associated with the valley detect are shown in Figure 10. If the voltage at the AUX winding is not sufficient for valley detection when V_{COMP} > 1.63 V, an internal valley wait timer of 12.7 µs ($t_{VD(vw)}$) expires after the t_{PERIOD} times out. The time out of the valley wait timer would initiate a new PWM switching pulse following the 100 mV threshold crossing on the VD pin.

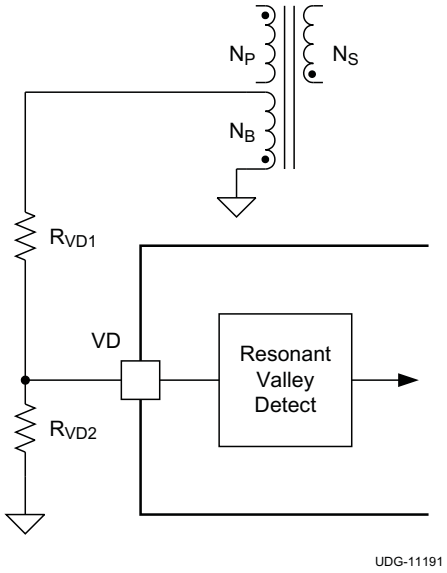


Figure 9. Auxiliary Winding Interface to VD

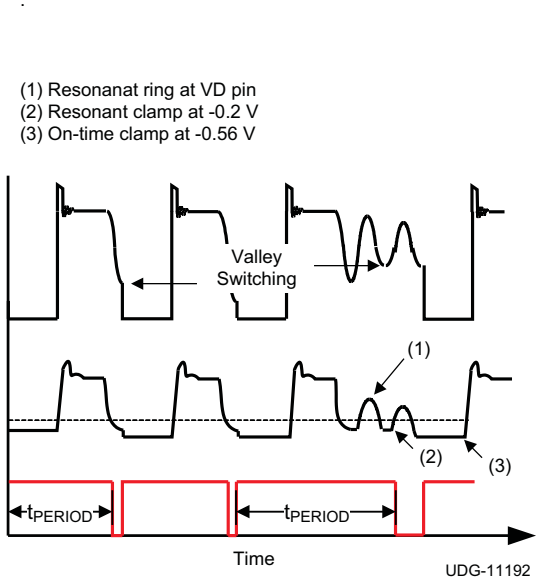


Figure 10. HV MOSFET Drain and VD Waveforms

TRIAC DIMMER DETECT

The TDD pin is used to drive an external by-pass FET that disables valley-fill PFC when a dimmer is detected by TPS92070. The TDD pin is set to logic high state ($V_{TDD(oh)}$ = 7 V) as the part is powered up and if no dimmer is detected by continuously sensing the SEN pin, the TDD pin is then reset to logic low ($V_{TDD(ol)}$ = 0 V). The presence of a dimmer is detected by monitoring the time delay in a window between 1 V and 5 V comparators that are monitoring the SEN pin. If the rise time from 1 V to 5 V is greater than 135 µs for four consecutive half-line cycles, direct connection to the AC line without dimmer is assumed, and the TDD output goes low. Otherwise the TDD pin remains high. If the TDD pin is low and the delay time ($t_{DLY\_1V\_5V}$) is detected to be less than 135 µs, for four consecutive half-line cycles, the TDD pin goes high once the SEN pin falls below 1 V indicating dimmer detection.

PROTECTION FEATURES

Output Over Voltage Protection (OVP)

Output (secondary-side) overvoltage protection / open LED detection is achieved by disabling the controller whenever the VDD voltage rises enough to trigger its internal 23 V clamp. Upon OVP detection, GATE is pulled low and the TDD pin is reset to logic-high state. The TPS92070 is disabled and an internal pull-down resistor ($R_{VZ(ovp)}$) discharges the VZ pin, until the VDD voltage drops below the UVLO threshold when a restart is triggered.

Overcurrent Protection (OCP)

Overcurrent faults are detected when the PCS pin exceeds the internal 700-mV threshold. Upon the detection of an OCP condition, the GATE signal is pulled low, and the LP pin voltage is reset to 0 V corresponding to the minimum LED output condition. GATE switching and current regulation resumes from the minimum LED light setting once the SEN pin crosses the 5 V.

Thermal Shutdown (TSD)

TPS92070 is disabled if the junction temperature of the part exceeds approximately 155°C and enters into the restart mode where the VZ pin is discharged until VDD falls below the UVLO threshold. The device stays in this restart mode until the junction temperature falls below approximately 140°C when it resumes normal operation with the light output preset to the minimum setting.

PCB Layout

Use good layout practices when constructing the PCB. Maintain the location of bypass components close to the pins being bypassed. Route power ground (PGND) separate from signal ground (GND) to keep the high current paths and the small signal paths separate. Connect PGND to GND at a single point, preferably under the device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92070PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP92070	Samples
TPS92070PWR	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125	TP92070	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

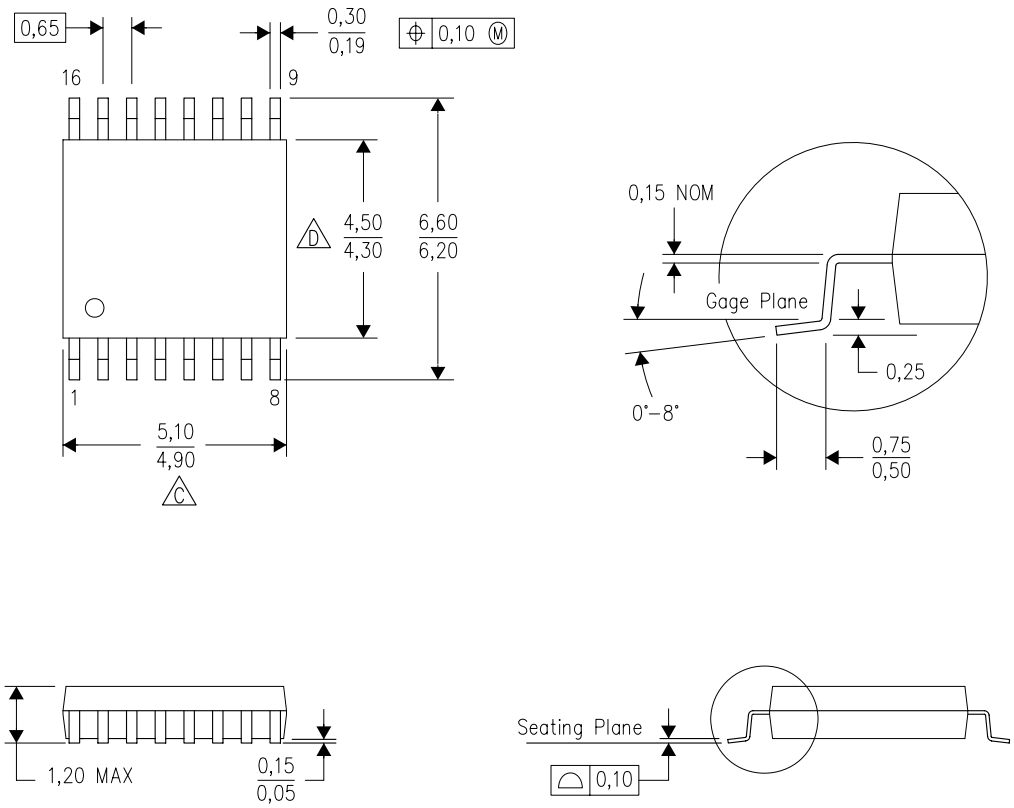
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

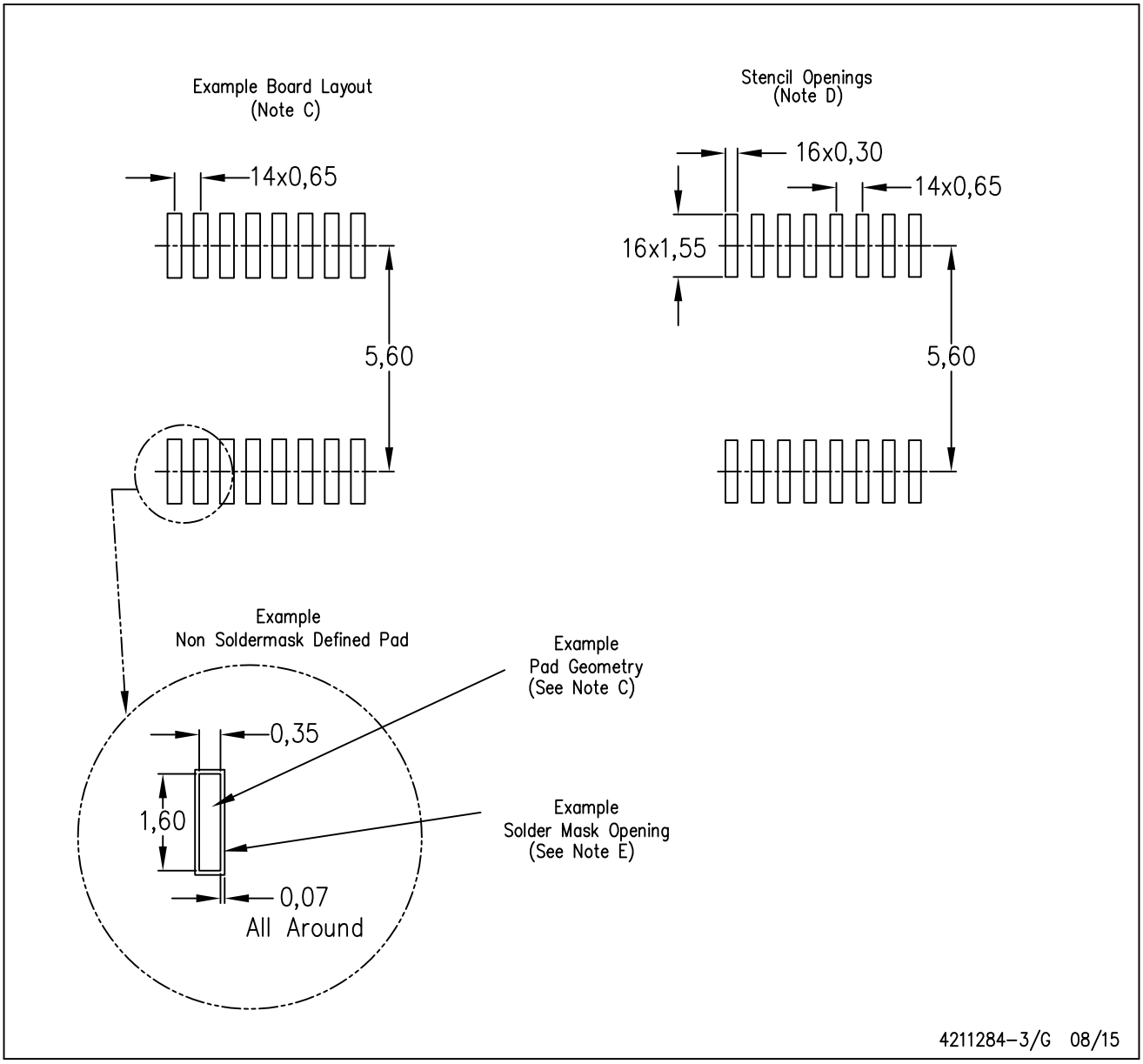
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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