

30-W STEREO DIGITAL AMPLIFIER POWER STAGE

FEATURES

- **2 × 30 W (BTL) Into 6 Ω at 1 kHz (DFD Pad-Up Package)**
 - DCA Package (Pad-Down) Recommended for Lower-Power Applications
- **95 dB Dynamic Range (in System With TAS5026)**
- **< 0.2% THD+N (in System – 30 W RMS Into 6- Ω Resistive Load)**
- **Device Power Efficiency Typical >90% Into 6- Ω Load**
- **Self-Protection Design (Including Undervoltage, Overtemperature, and Short Conditions) With Error Reports**
- **Internal Gate Drive Supply Voltage Regulator**
- **EMI Compliant When Used With Recommended System Design**

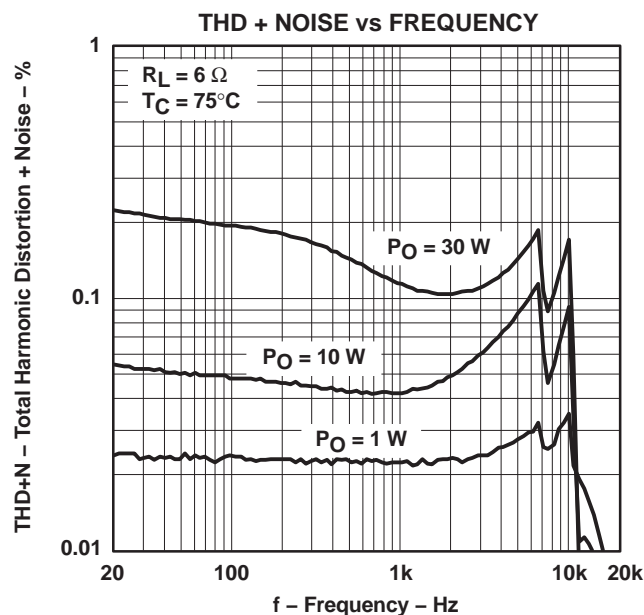
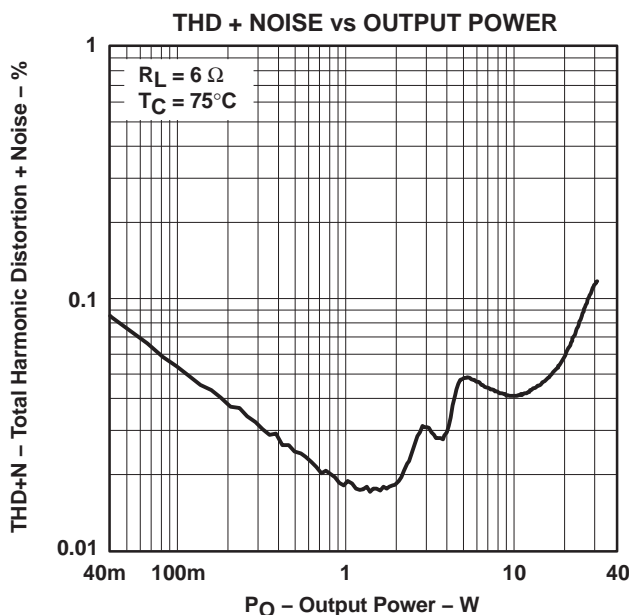
APPLICATIONS

- DVD Receiver
- Home Theatre
- Mini/Micro Component Systems
- Internet Music Appliance

DESCRIPTION

The TAS5122 is a high-performance, integrated stereo digital amplifier power stage designed to drive 6- Ω speakers at up to 30 W per channel (DFD package). The device incorporates TI's PurePath Digital™ technology and is used in conjunction with a digital audio PWM processor (TAS50XX) and a simple passive demodulation filter to deliver high-quality, high-efficiency, true-digital audio amplification.

The efficiency of this digital amplifier is typically greater than 90%, reducing the size of both the power supplies and heat sinks needed. Overcurrent protection, overtemperature protection, and undervoltage protection are built into the TAS5122, safeguarding the device and speakers against fault conditions that could damage the system.



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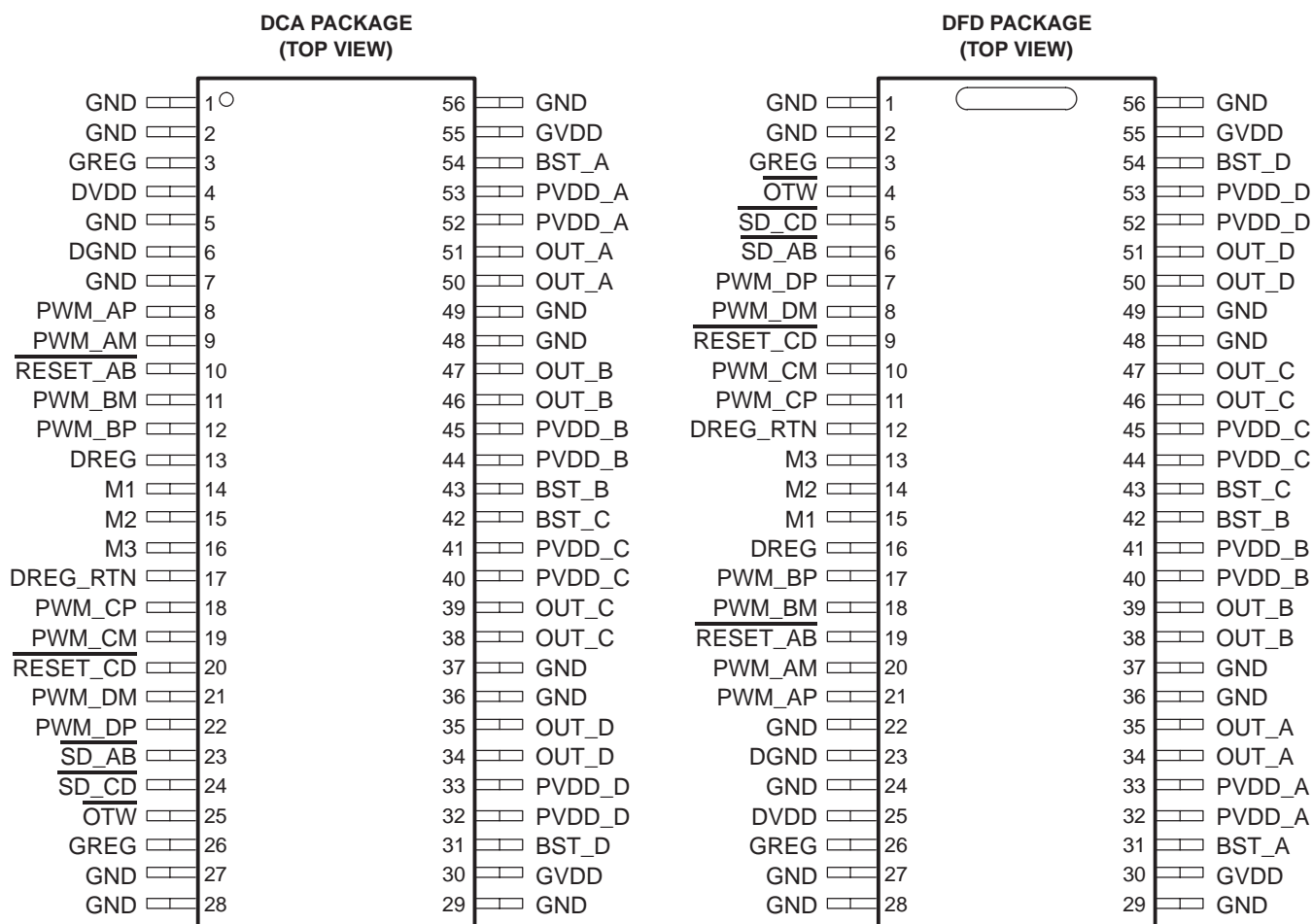


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

GENERAL INFORMATION

Terminal Assignment

The TAS5122 is offered in a thermally enhanced 56-pin TSSOP DFD package (thermal pad is on the top). The TAS5122 is also offered in a thermally enhanced 56-pin DCA package (thermal pad is on the bottom). The DCA package is recommended for lower-power applications, typically 15 W per channel. Output of the DCA package is highly dependent on thermal design. See the *Thermal Information* section.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

TAS5122	UNITS
DVDD to DGND	–0.3 V to 4.2 V
GVDD to GND	28 V
PVDD_X to GND (dc voltage)	28 V
OUT_X to GND (dc voltage)	28 V
BST_X to GND (dc voltage)	40 V
GREG to GND ⁽²⁾	14.2 V
PWM_XP, RESET, M1, M2, M3, SD, OTW	–0.3 V to DVDD + 0.3 V
Maximum operating junction temperature, T _J	–40°C to 150°C
Storage temperature	–40°C to 125°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) GREG is treated as an input when the GREG pin is overdriven by GVDD of 12 V.

ORDERING INFORMATION

T _A	PACKAGE	DESCRIPTION
0°C to 70°C	TAS5122DFD	56-pin small TSSOP
0°C to 70°C	TAS5122DCA	56-pin small TSSOP

PACKAGE DISSIPATION RATINGS

PACKAGE	R _{θJC} (°C/W)	R _{θJA} (°C/W)
56-pin DFD TSSOP	1.14	See Note 1
56-pin DCA TSSOP	1.14	See Note 1

(1) The TAS5122 package is thermally enhanced for conductive cooling using an exposed metal pad area. It is impractical to use the device with the pad exposed to ambient air as the only heat sinking of the device.

For this reason, R_{θJA} a system parameter that characterizes the thermal treatment provided in the application. An example and discussion of typical system R_{θJA} values are provided in the *Thermal Information* section. This example provides additional information regarding the power dissipation ratings. This example should be used as a reference to calculate the heat dissipation ratings for a specific application. TI application engineering provides technical support to design heat sinks if needed.

TAS5122

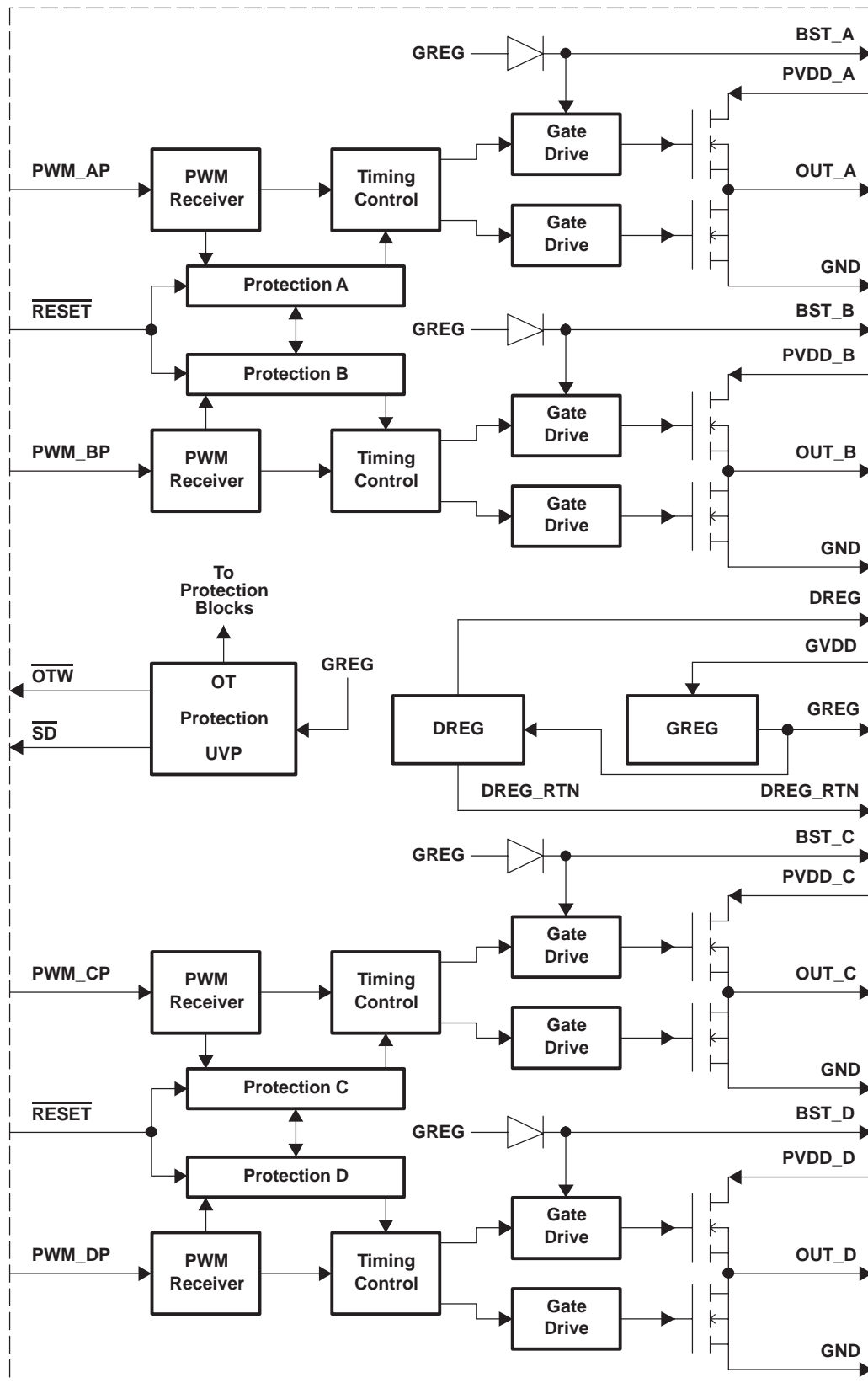
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Terminal Functions

TERMINAL			FUNCTION ⁽¹⁾	DESCRIPTION
NAME	DFD NO.	DCA NO.		
BST_A	31	54	P	HS bootstrap supply (BST), external capacitor to OUT_A required
BST_B	42	43	P	HS bootstrap supply (BST), external capacitor to OUT_B required
BST_C	43	42	P	HS bootstrap supply (BST), external capacitor to OUT_C required
BST_D	54	31	P	HS bootstrap supply (BST), external capacitor to OUT_D required
DGND	23	6	P	Digital I/O reference ground
DREG	16	13	P	Digital supply voltage regulator decoupling pin, capacitor connected to GND
DREG_RTN	12	17	P	Digital supply voltage regulator decoupling return pin
DVDD	25	4	P	I/O reference supply input (3.3V)
GND	1, 2, 22, 24, 27, 28, 29, 36, 37, 48, 49, 56	1, 2, 5, 7, 27, 28, 29, 36, 37, 48, 49, 56	P	Power ground (I/O reference ground – pin 22)
GREG	3, 26	3, 26	P	Gate drive voltage regulator decoupling pin, capacitor to GND
GVDD	30, 55	30, 55	P	Voltage supply to on-chip gate drive and digital supply voltage regulators
M1	15	14	I	Mode selection pin
M2	14	15	I	Mode selection pin
M3	13	16	I	Mode selection pin
OTW	4	25	O	Over temperature warning output, open drain w. internal pullup
OUT_A	34, 35	50, 51	O	Output, half-bridge A
OUT_B	38, 39	46, 47	O	Output, half-bridge B
OUT_C	46, 47	38, 39	O	Output, half-bridge C
OUT_D	50, 51	34, 35	O	Output, half-bridge D
PVDD_A	32, 33	52, 53	P	Power supply input for half-bridge A
PVDD_B	40, 41	44, 45	P	Power supply input for half-bridge B
PVDD_C	44, 45	40, 41	P	Power supply input for half-bridge C
PVDD_D	52, 53	32, 33	P	Power supply input for half-bridge D
PWM_AM	20	9	I	Input signal (negative), half-bridge A
PWM_AP	21	8	I	Input signal (positive), half-bridge A
PWM_BM	18	11	I	Input signal (negative), half-bridge B
PWM_BP	17	12	I	Input signal (positive), half-bridge B
PWM_CM	10	19	I	Input signal (negative), half-bridge C
PWM_CP	11	18	I	Input signal (positive), half-bridge C
PWM_DM	8	21	I	Input signal (negative), half-bridge D
PWM_DP	7	22	I	Input signal (positive), half-bridge D
RESET_AB	19	10	I	Reset signal, active low
RESET_CD	9	20	I	Reset signal, active low
SD_AB	6	23	O	Shutdown signal for half-bridges A and B
SD_CD	5	24	O	Shutdown signal for half-bridges C and D

⁽¹⁾ I = input, O = output, P = power

FUNCTIONAL BLOCK DIAGRAM



TAS5122

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RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
DVDD	Digital supply ⁽¹⁾	Relative to DGND	3	3.3	3.6	V
GVDD	Supply for internal gate drive and logic regulators	Relative to GND	16	23	25.5	V
PVDD_x	Half-bridge supply	Relative to GND, $R_L = 6\ \Omega$ to $8\ \Omega$	0	23	25.5	V
T _J	Junction temperature		0		125	°C

(1) It is recommended for DVDD to be connected to DREG via a 100- Ω resistor.

ELECTRICAL CHARACTERISTICS

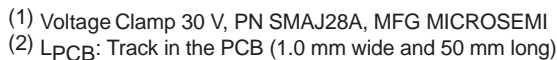
PVDD_X = 23 V, GVDD = 23 V, DVDD = 3.3 V, DVDD connected to DREG via a 100- Ω resistor, $R_L = 6\ \Omega$, $8X\ f_S = 384\ \text{kHz}$, unless otherwise noted. AC performance is recorded as a chipset with TAS5010 as the PWM processor and TAS5122 as the power stage.

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL T _A =25°C	T _A =25°C	T _{Case} = 75°C	UNITS	MIN/TYP/ MAX
AC PERFORMANCE, BTL MODE, 1 kHz							
P _O	Output power	$R_L = 8\ \Omega$, unclipped, AES17 filter			24	W	Typ
		$R_L = 8\ \Omega$, THD = 10%, AES17 filter			29	W	Typ
		$R_L = 6\ \Omega$, THD = 0.4%, AES17 filter			30	W	Typ
		$R_L = 6\ \Omega$, THD = 10%, AES17 filter			37	W	Typ
THD+N	Total harmonic distortion + noise	Po = 1 W/channel, $R_L = 6\ \Omega$, AES17 filter			0.05%		Typ
		Po = 10 W/channel, $R_L = 6\ \Omega$, AES17 filter			0.05%		Typ
		Po = 30 W/channel, $R_L = 6\ \Omega$, AES17 filter			0.2%		Typ
V _n	Output RMS noise	A-weighted, mute, $R_L = 6\ \Omega$, 20 Hz to 20 kHz, AES17 filter			240	μV	Max
SNR	Signal-to-noise ratio	f = 1 kHz, A-weighted, $R_L = 6\ \Omega$, AES17 filter			95	dB	Typ
DR	Dynamic range	f = 1 kHz, A-weighted, $R_L = 6\ \Omega$, AES17 filter			95	dB	Typ
INTERNAL VOLTAGE REGULATOR							
DREG	Voltage regulator	I _O = 1 mA, PVDD = 18 V–30.5 V	3.1			V	Typ
GREG	Voltage regulator	I _O = 1.2 mA, PVDD = 18 V–30.5 V	13.4			V	Typ
IVGDD	GVDD supply current, operating	f _S = 384 kHz, no load, 50% duty cycle		24		mA	Max
IDVDD	DVDD supply current, operating	f _S = 384 kHz, no load	1	5		mA	Max
OUTPUT STAGE MOSFETs							
R _{DSon,LS}	Forward on-resistance, LS	T _J = 25°C	155			m Ω	Max
R _{DSon,HS}	Forward on-resistance, HS	T _J = 25°C	155			m Ω	Max

ELECTRICAL CHARACTERISTICS

PVDD_x = 23 V, GVDD = 23 V, DVDD = 3.3 V, R_L = 6 Ω, 8X f_S = 384 kHz, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL T _A =25°C	T _A =25°C	T _{Case} = 75°C	UNITS	MIN/TYP/ MAX
INPUT/OUTPUT PROTECTION							
V _{uvp,G}	Undervoltage protection limit, GVDD		7.4	6.9		V	Min
				7.9		V	Max
OTW	Overtemperature warning		125			°C	Typ
OTE	Overtemperature error		150			°C	Typ
OC	Overcurrent protection			5.0		A	Min
STATIC DIGITAL SPECIFICATION							
	PWM_AP, PWM_BP, M1, M2, M3, $\overline{\text{SD}}$, $\overline{\text{OTW}}$						
V _{IH}	High-level input voltage			2		V	Min
				DVDD		V	Max
V _{IL}	Low-level input voltage			0.8		V	Max
Leakage	Input leakage current			−10		μA	Min
				10		μA	Max
OTW/SHUTDOWN (SD)							
	Internally pull up R from $\overline{\text{OTW/SD}}$ to DVDD		30	22.5		kΩ	Min
V _{OL}	Low level output voltage	I _O = 4 mA		0.4		V	Max



TYPICAL CHARACTERISTICS

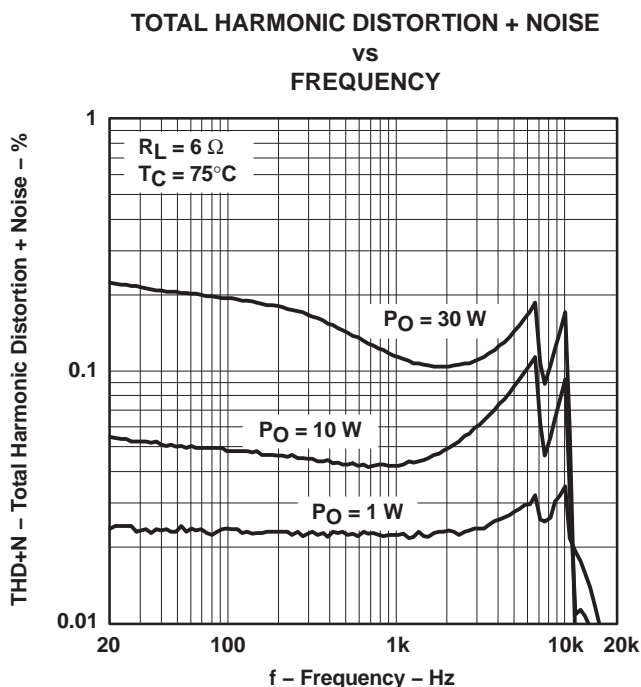


Figure 1

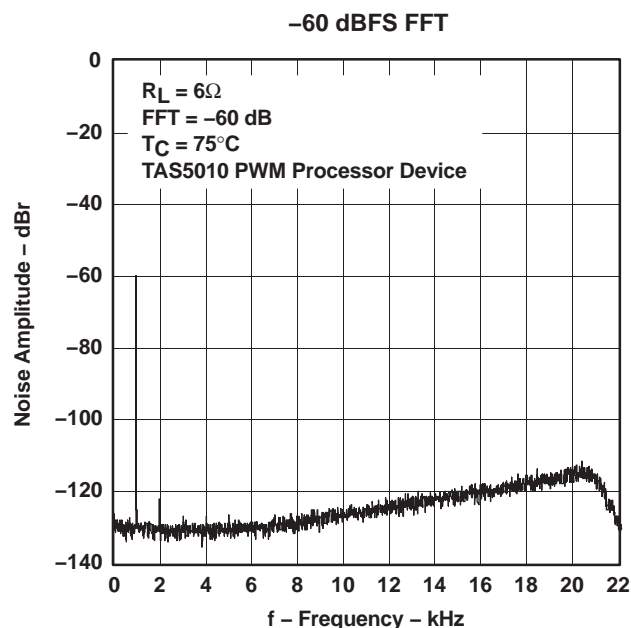


Figure 2

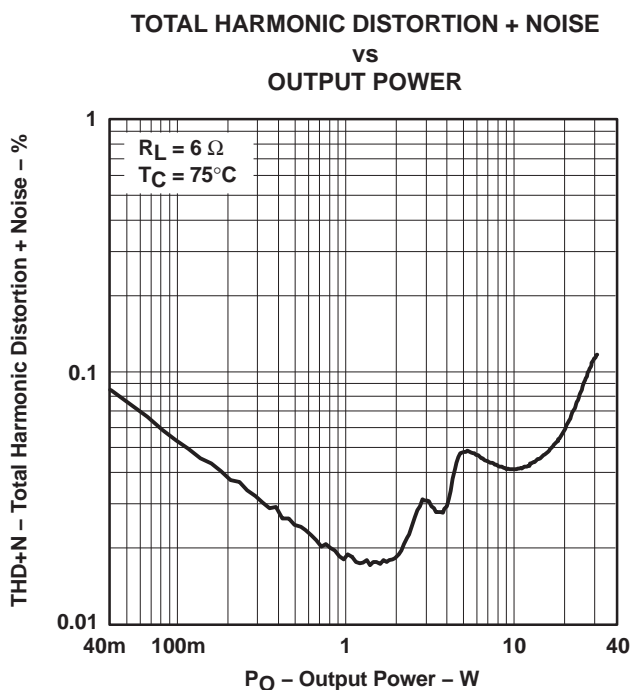


Figure 3

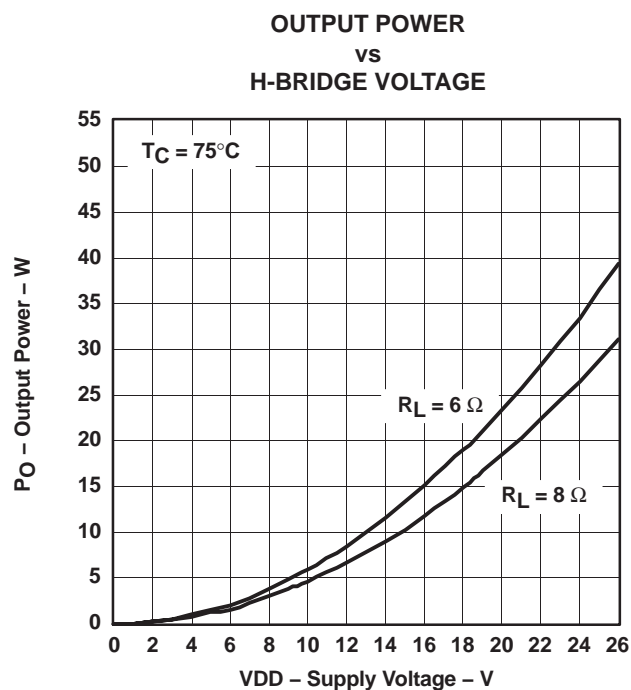


Figure 4

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SYSTEM OUTPUT STAGE EFFICIENCY
vs
OUTPUT POWER

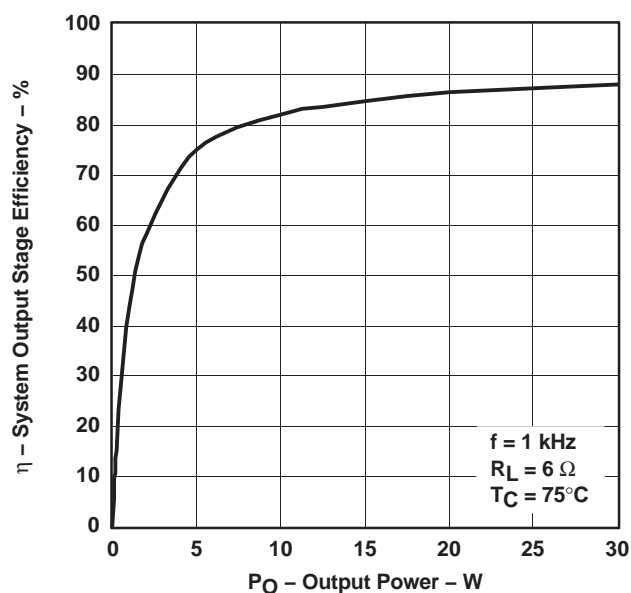


Figure 5

POWER LOSS
vs
OUTPUT POWER

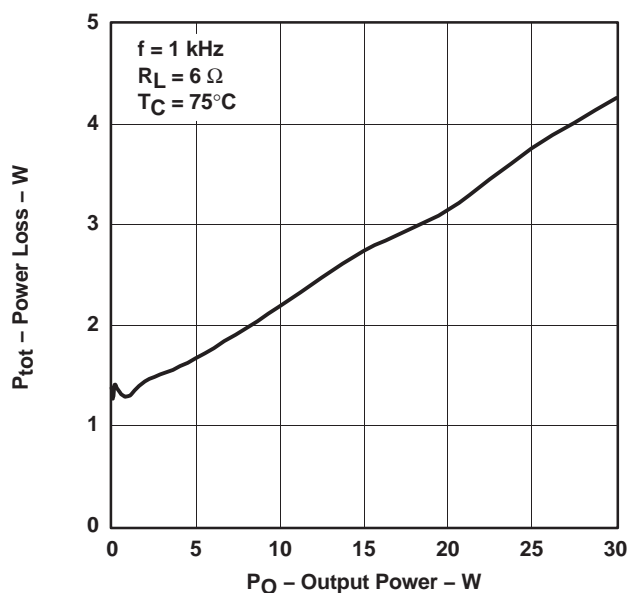


Figure 6

OUTPUT POWER
vs
CASE TEMPERATURE

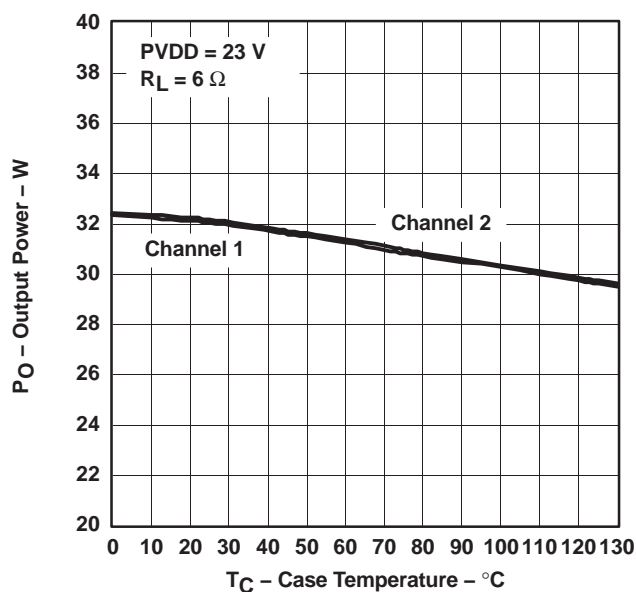


Figure 7

AMPLITUDE
vs
FREQUENCY

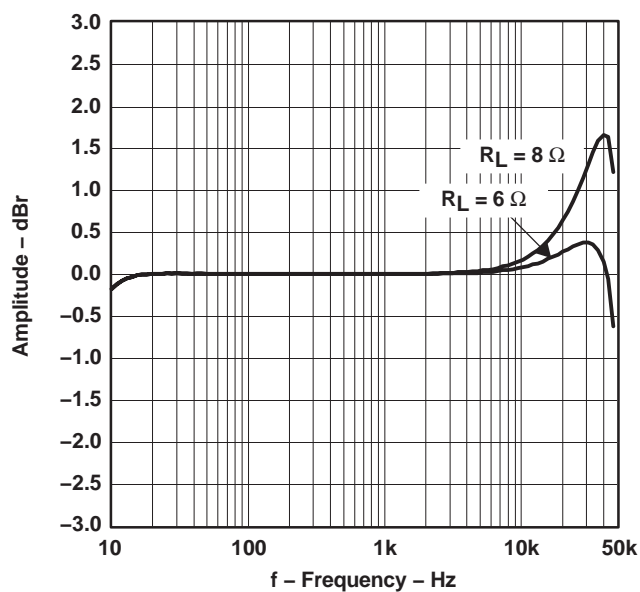


Figure 8

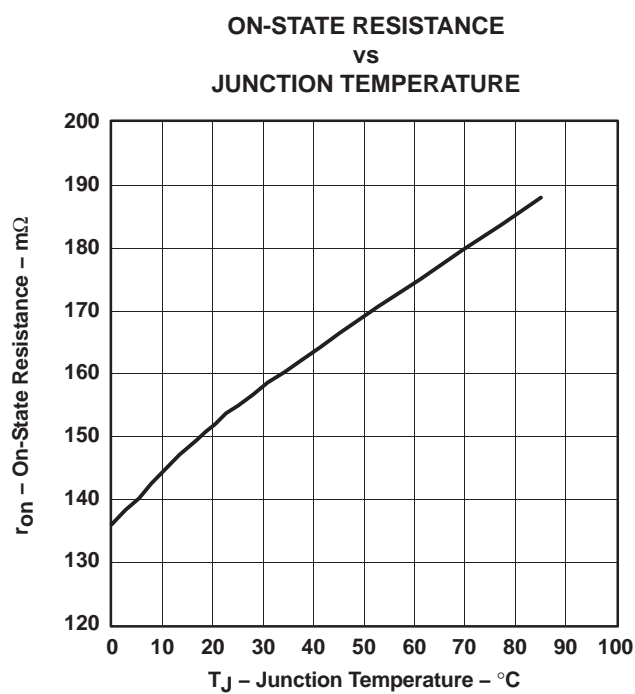


Figure 9

THEORY OF OPERATION

POWER SUPPLIES

The power device only requires two supply voltages, GVDD and PVDD_x.

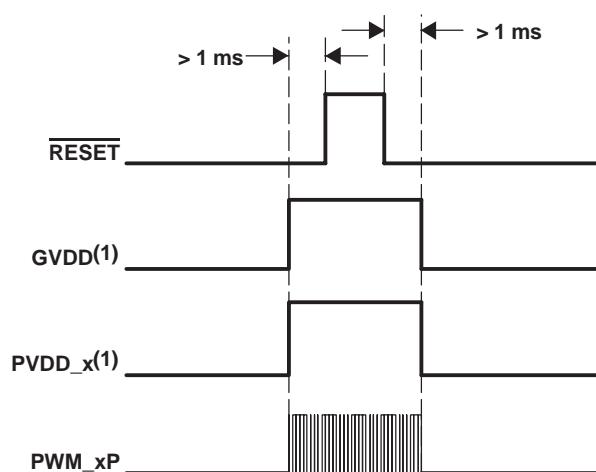
GVDD is the gate drive supply for the device, regulated internally down to approximately 12 V, and decoupled with regards to board GND on the GREG pins through an external capacitor. GREG powers both the low side and high side via a bootstrap step-up conversion. The bootstrap supply is charged after the first low-side turnon pulse. Internal digital core voltage DREG is also derived from GVDD and regulated down by internal LDRs to 3.3 V.

The gate-driver LDR can be bypassed for reducing idle loss in the device by shorting GREG to GVDD and directly feeding in 12.0 V. This can be useful in an application where thermal conduction of heat from the device is difficult. Bypassing the LDR reduces power dissipation.

PVDD_x is the H-bridge power supply pin. Two power pins exist for each half-bridge to handle the current density. It is very important that the circuitry recommendations around the PVDD_x pins are followed very carefully both topology- and layout-wise. For topology recommendations, see the *System Configuration Used for Characterization* section. Following these recommendations is important for parameters like EMI, reliability, and performance.

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up



(1) PVDD should not be powered up before GVDD.

During power up when $\overline{\text{RESET}}$ is asserted LOW, all MOSFETs are turned off and the two internal half-bridges are in the high-impedance state (Hi-Z). The bootstrap capacitors supplying high-side gate drive are at this point

not charged. To comply with the click and pop scheme and use of non-TI PWM processors it is recommended to use a 4-k Ω pulldown resistor on each PWM output node to ground. This precharges the bootstrap supply capacitors and discharges the output filter capacitor (see the *System Configuration Used for Characterization* section).

After GVDD has been applied, it takes approximately 800 μs to fully charge the BST capacitor. Within this time, $\overline{\text{RESET}}$ must be kept low. After approximately 1 ms, the power stage bootstrap capacitor is charged.

$\overline{\text{RESET}}$ can now be released if the modulator is powered up and streaming PWM signals to the power stage PWM_{xP}.

A constant HIGH dc level on PWM_{xP} is not permitted, because it would force the high-side MOSFET ON until it eventually ran out of BST capacitor energy and might damage the device.

An unknown state of the PWM output signals from the processor is illegal and should be avoided, which in practice means that the PWM processor must be powered up and initialized before $\overline{\text{RESET}}$ is de-asserted HIGH to the power stage.

Powering Down

For power down of the power stage, an opposite approach is necessary. $\overline{\text{RESET}}$ must be asserted LOW before the valid PWM signal is removed.

When TI PWM processors are used in conjunction with TI power stages, the correct timing control of $\overline{\text{RESET}}$ and PWM_{xP} is performed by the modulator.

Precaution

The TAS5122 must always start up in the high-impedance (Hi-Z) state. In this state, the bootstrap (BST) capacitor is precharged by a resistor on each PWM output node to ground. See *System Configuration Used for Characterization*. This ensures that the power stage is ready for receiving PWM pulses, indicating either HIGH- or LOW-side turnon after $\overline{\text{RESET}}$ is deasserted to the power stage.

With the following pulldown and BST capacitor size the charge time is:

$$C = 33 \text{ nF}, R = 4.7 \text{ k}\Omega$$

$$R \times C \times 5 = 775.5 \mu\text{s}$$

After GVDD has been applied, it takes approximately 800 μs to fully charge the BST capacitor. During this time, $\overline{\text{RESET}}$ must be kept low. After approximately 1 ms the power stage BST is charged and ready. $\overline{\text{RESET}}$ can now be released if the PWM modulator is ready and is streaming valid PWM signals to the power stage. Valid PWM signals are switching PWM signals with a frequency between 350–400 kHz. A constant HIGH level on the

PWM_xP forces the high side MOSFET ON until it eventually runs out of BST capacitor energy. Putting the device in this condition should be avoided.

In practice this means that the DVDD-to-PWM processor should be stable and initialization should be completed before $\overline{\text{RESET}}$ is deasserted to the power stage.

CONTROL I/O

Shutdown Pin: $\overline{\text{SD}}$

The $\overline{\text{SD}}$ pin functions as an output pin and is intended for protection-mode signaling to, for example, a controller or other PWM processor device. The pin is open-drain with an internal pullup to DVDD.

The logic output is, as shown in the following table, a combination of the device state and $\overline{\text{RESET}}$ input:

$\overline{\text{SD}}$	$\overline{\text{RESET}}$	DESCRIPTION
0	0	Not used
0	1	Device in protection mode, i.e., UVP and/or OC and/or OT error
1(2)	0	Device set high-impedance (Hi-Z), $\overline{\text{SD}}$ forced high
1	1	Normal operation

(2) $\overline{\text{SD}}$ is pulled high when $\overline{\text{RESET}}$ is asserted low independent of chip state (i.e., protection mode). This is desirable to maintain compatibility with some TI PWM processors.

Temperature Warning Pin: $\overline{\text{OTW}}$

The $\overline{\text{OTW}}$ pin gives a temperature warning signal when temperature exceeds the set limit. The pin is of the open-drain type with an internal pullup to DVDD.

$\overline{\text{OTW}}$	DESCRIPTION
0	Junction temperature higher than 125°C
1	Junction temperature lower than 125°C

Overall Reporting

The $\overline{\text{SD}}$ pin, together with the $\overline{\text{OTW}}$ pin, gives chip state information as described in Table 1.

Table 1. Error Signal Decoding

$\overline{\text{OTW}}$	$\overline{\text{SD}}$	DESCRIPTION
0	0	Overtemperature error (OTE)
0	1	Overtemperature warning (OTW)
1	0	Overcurrent (OC) or undervoltage (UVP) error
1	1	Normal operation, no errors/warnings

Chip Protection

The TAS5122 protection function is implemented in a closed loop with, for example, a system controller or other TI PWM processor device. The TAS5122 contains three individual systems protecting the device against misuse.

All of the error events covered result in the output stage being set in a high-impedance state (Hi-Z) for maximum protection of the device and connected equipment.

The device can be recovered by toggling $\overline{\text{RESET}}$ low and then high, after all errors are cleared.

Overcurrent (OC) Protection

The device has individual forward current protection on both high-side and low-side power stage FETs. The OC protection works only with the demodulation filter present at the output. See *Demodulation Filter Design* in the *Application Information* section of this data sheet for design constraints.

Overtemperature (OT) Protection

A dual temperature protection system asserts a warning signal when the device junction temperature exceeds 125°C. The OT protection circuit is shared by all half-bridges.

Undervoltage (UV) Protection

Undervoltage lockout occurs when GVDD is insufficient for proper device operation. The UV protection system protects the device under power-up and power-down situations. The UV protection circuits are shared by all half-bridges.

Reset Function

The function of the reset input is twofold:

- Reset is used for re-enabling operation after a latching error event (PMODE1).
- Reset is used for disabling output stage switching (mute function).

The error latch is cleared on the falling edge of reset and normal operation is resumed when reset goes high.

PROTECTION MODE

Latching Shutdown on All Errors (PMODE1)

In latching shutdown mode, all error situations result in a permanent shutdown (output stage Hi-Z). Re-enabling can be done by toggling the $\overline{\text{RESET}}$ pin.

Autorecovery (AR) After Errors (PMODE0)

In autorecovery mode (PMODE0) the TAS5122 is 100% self-supported in handling of error situations. All protection systems are active, setting the output stage in the high-impedance state to protect the output stage and connected equipment. However, after a short time period the device auto-recovers, i.e., operation is automatically resumed provided that the system is fully operational.

The auto-recovery timing is set by counting PWM input cycles, i.e. the timing is relative to the switching frequency.

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The AR system is common to both half-bridges.

Timing and Function

Latching Shutdown on All Errors (PMODE1)

In latching shutdown mode all error situations result in a permanent shutdown (output stage Hi-Z). Re-enabling can be done by toggling the $\overline{\text{RESET}}$ pin.

All Protection Systems Disabled (PMODE2)

In PMODE2 all protection systems are disabled. This mode is purely intended for testing and characterization purposes and thus not recommended for normal device operation.

MODE Pins Selection

The protection mode is selected by shorting M1/M2 to DREG or DGND according to Table 2.

Table 2. Protection Mode Selection

M1	M2	PROTECTION MODE
0	0	Reserved
0	1	Latching shutdown on all errors (PMODE1)
1	0	Reserved
1	1	Reserved

The output configuration mode is selected by shorting the M3 pin to DREG or DGND according to Table 3.

Table 3. Output Mode Selection

M3	OUTPUT MODE
0	Bridge-tied load output stage (BTL)
1	Reserved

APPLICATION INFORMATION

DEMODULATION FILTER DESIGN

The TDAA amplifier outputs are driven by heavy-duty DMOS transistors in an H-bridge configuration. These transistors are either off or fully on, which reduces the DMOS transistor on-state resistance, $R_{DS(on)}$, and the power dissipated in the device, thereby increasing efficiency.

The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal. For this application, EMI is considered important; therefore, the selected filter is the full-output type shown in Figure 10.

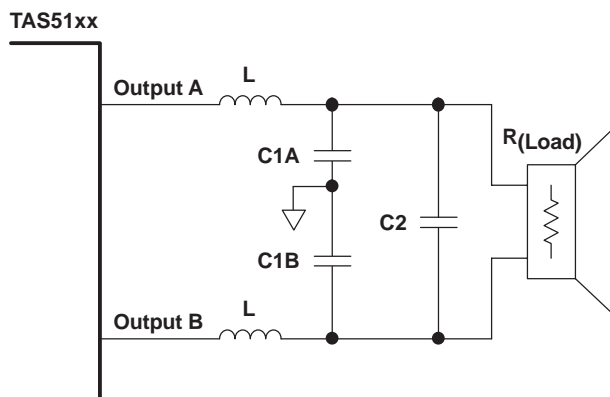


Figure 10. Demodulation Filter

The main purpose of the output filter is to attenuate the high-frequency switching component of the PurePath Digital amplifier while preserving the signals in the audio band.

If this rule is observed, the TAS5122 does not have distortion issues due to the output inductors and overcurrent conditions do not occur due to inductor saturation in the output filter.

Another parameter to be considered is the idle current loss in the inductor. This can be measured or specified as inductor dissipation (D). The target specification for dissipation is less than 0.05.

In general, 10- μH inductors suffice for most applications. The frequency response of the amplifier is slightly altered by the change in output load resistance; however, unless very tight control of frequency response is necessary (better than 0.5 dB), it is not necessary to deviate from 10 μH .

The graphs in Figure 11 display the inductance vs current characteristics of two inductors that are recommended for use with the TAS5122.

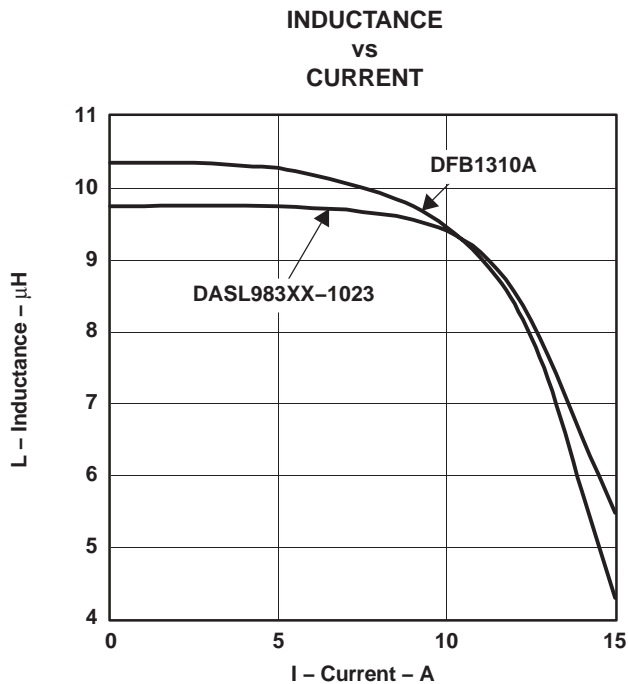


Figure 11. Inductance Saturation

The selection of the capacitor that is placed across the output of each inductor (C2 in Figure 10) is very simple. To complete the output filter, use a 0.47-μF capacitor with a voltage rating at least twice the voltage applied to the output stage (PVDD).

This capacitor should be a good quality polyester dielectric such as a Wima MKS2-047ufd/100/10 or equivalent.

In order to minimize the EMI effect of unbalanced ripple loss in the inductors, 0.1-μF 50-V SMD capacitors (X7R or better) (C1A and C1B in Figure 10) should be added from the output of each inductor to ground.

THERMAL INFORMATION

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with roughly the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the metal pad)
- Thermal grease thermal resistance
- Heat sink thermal resistance

$R_{\theta JC}$ has been provided in the *Package Dissipation Ratings* section.

The thermal grease thermal resistance can be calculated from the exposed pad area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in²/W). The area thermal resistance of the example thermal grease with a 0.002 inch thick layer is about 0.1 °C-in²/W. The approximate exposed pad area is as follows:

56-pin HTSSOP 0.045 in²

Dividing the example thermal grease area resistance by the surface area gives the actual resistance through the thermal grease for both ICs inside the package:

56-pin HTSSOP 2.27 °C/W

The thermal resistance of thermal pads is generally considerably higher than a thin thermal grease layer. Thermal tape has an even higher thermal resistance. Neither pads nor tape should be used with either of these two packages. A thin layer of thermal grease with careful clamping of the heat sink is recommended. It may be difficult to achieve a layer 0.001 inch thick or less, so the modeling below is done with a 0.002 inch thick layer, which may be more representative of production thermal grease thickness.

Heat sink thermal resistance is generally predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus, for a single monaural IC, the system $R_{\theta JA} = R_{\theta JC} + \text{thermal grease resistance} + \text{heat sink resistance}$.

DFD THERMAL INFORMATION

The thermally augmented package provided with the TAS5122DFD is designed to be interfaced directly to heat sinks using a thermal interface compound (for example, Wakefield Engineering type 126 thermal grease.) The heat sink then absorbs heat from the ICs and couples it to the local air. If the heatsink is carefully designed, this process can reach equilibrium and heat can be continually removed from the ICs. Because of the efficiency of the TAS5122DFD, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

Table 4 and Table 5 indicate modeled parameters for one or two TAS5122DFD ICs on a single heat sink. The final junction temperature is set at 110°C in all cases. It is assumed that the thermal grease is 0.002 inch thick and that it is similar in performance to Wakefield Type 126 thermal grease. It is important that the thermal grease layer is ≤0.002 inches thick and that thermal pads or tape are not used in the pad-to-heat sink interface due to the high power density that results in these extreme power cases.

TAS5122

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Table 4. Case 1 (2×30 W Unclipped Into $6\ \Omega$, Both Channels in Same IC) (1)

	56-Pin HTSSOP
Ambient temperature	25°C
Power to load (per channel)	30 W (unclipped)
Power dissipation	2.8 W
Delta T inside package	6.3°C, note 2 \times channel dissipation
Delta T through thermal grease	22.8°C, note 2 \times channel dissipation
Required heat sink thermal resistance	10.2°C/W
Junction temperature	110°C
System $R_{\theta JA}$	15.5°C/W
$R_{\theta JA}$ * power dissipation	85°C
Junction temperature	85°C + 25°C = 110°C

(1) This case represents a stereo system with only one package. See Case 2 if doing a full-power, 2-channel test in a multichannel system.

Table 5. Case 2 (2×30 W Unclipped Into $6\ \Omega$, Channels in Separate Packages) (1)

	56-Pin HTSSOP
Ambient temperature	25°C
Power to load (per channel)	30 W (unclipped)
Power dissipation	2.8 W
Delta T inside package	3.1°C
Delta T through thermal grease	11.4°C
Required heat sink thermal resistance	12.8°C/W
Junction temperature	110°C
System $R_{\theta JA}$	15.5°C/W
$R_{\theta JA}$ * power dissipation	85°C
Junction temperature	85°C + 25°C = 110°C

(1) In this case, the power is separated into two packages. Note that this allows a considerably smaller heat sink because twice as much area is available for heat transfer through the thermal grease. For this reason, separating the stereo channels into two ICs is recommended in full-power stereo tests made on multichannel systems.

DCA THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin HTSSOP, but includes a thermal pad (see Figure 12) to provide an effective thermal contact between the IC and the PCB.

The PowerPAD package (thermally enhanced HTSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of an HTSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipater, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

Thermal Methodology for the DCA 56-Pin, 2×15 -W, $8\text{-}\Omega$ Package

The thermal design for the DCA part (e.g., thermal pad soldered to the board) should be similar to the design as in the following figures. The cooling approach is to conduct the dissipated heat into the via pads on the board, through the vias in the board, and into a heat sink (aluminum bar) (if necessary).

Figure 12 shows a recommended land pattern on the PCB.

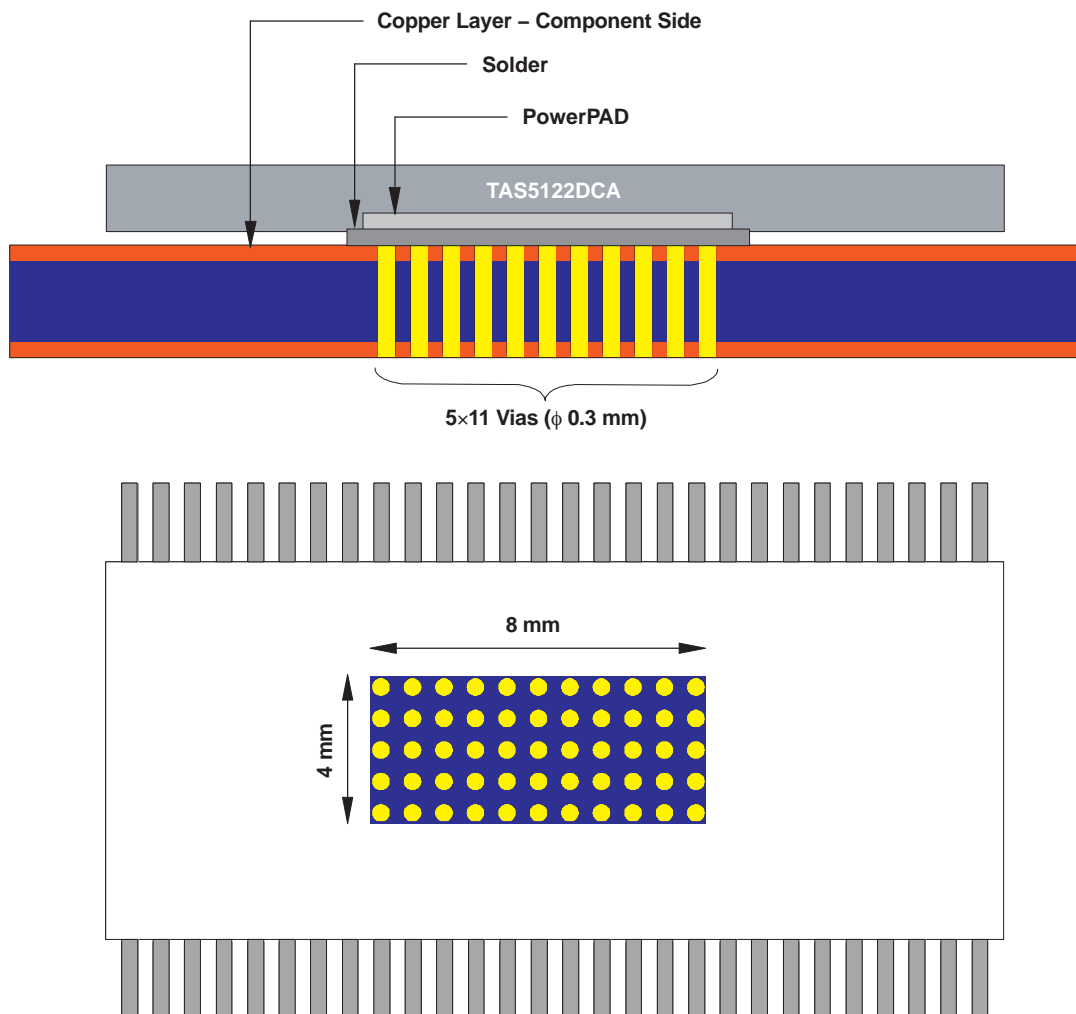


Figure 12. Recommended Land Pattern

The lower via pad area, slightly larger than the IC pad itself, is exposed with a window in the solder resist on the bottom surface of the board. It is not coated with solder during the board construction to maintain a flat surface. In production, this can be accomplished with a peelable solder mask.

An aluminum bar is used to keep the through-hole leads

from shorting to the chassis. The thermal compound shown has a pad-to-aluminum bar thermal resistance of about 3.2° C/W.

The chassis provides the only heat sink to air and is chosen as representative of a typical production cooling approach.

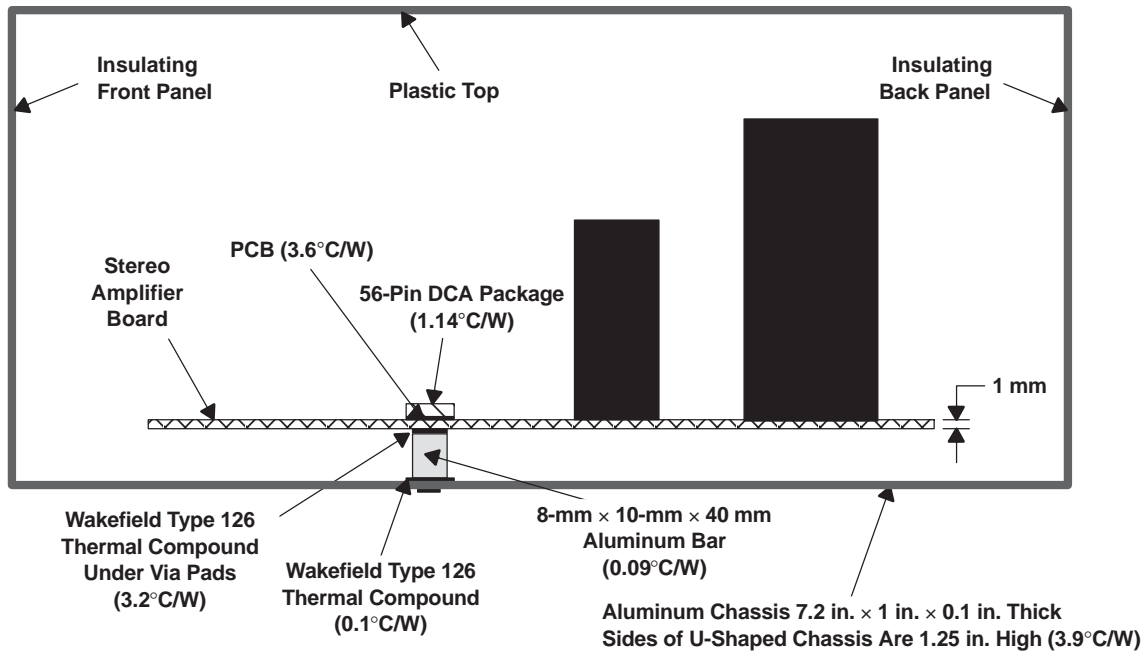


Figure 13. 56-Pin DCA Package Cross-Sectional View (Side)

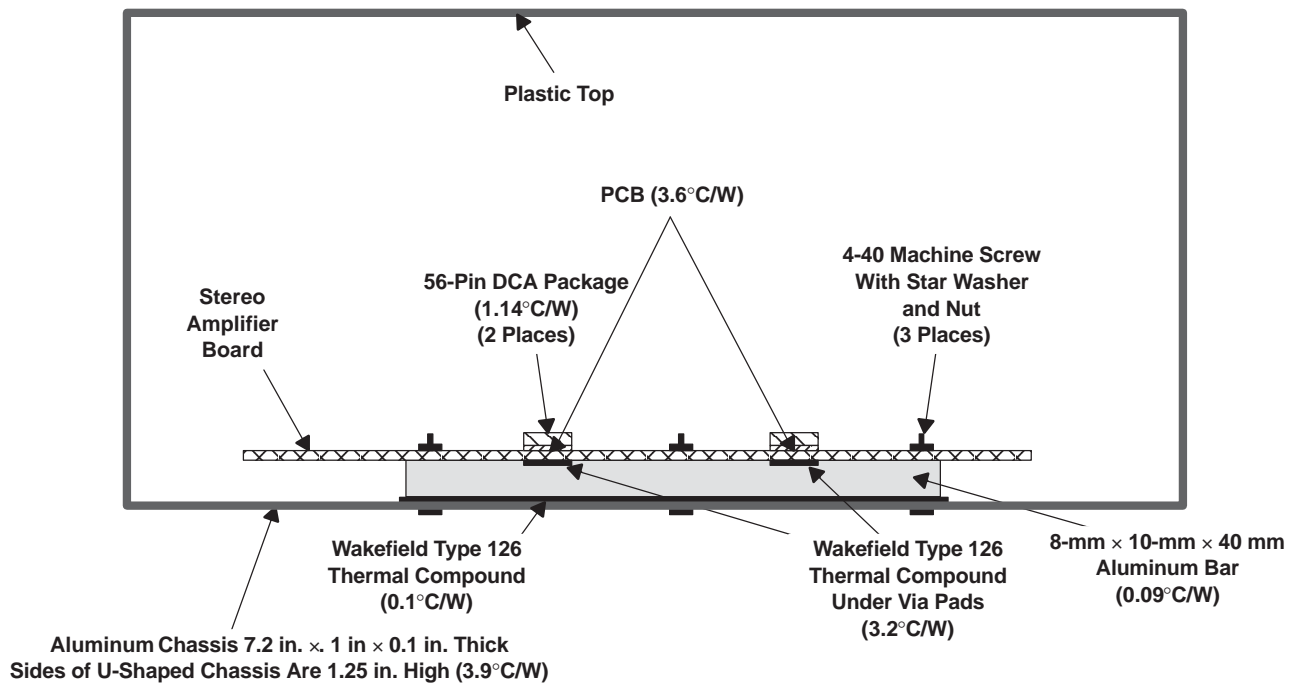


Figure 14. Spatial Separation With Multiple Packages

The land pattern recommendation shown in Figure 12 is for optimal performance with aluminum bar thermal resistance of 0.09 ° C/W. The following table shows the

decrease in thermal resistance through the PCB with a corresponding increase in the land pattern size. Use the table for thermal design tradeoffs.

LAND PATTERN	PCB THERMAL RESISTANCE
7×13 vias (5×10 mm)	2.2°C/W
5×11 vias (4×8 mm)	3.6°C/W

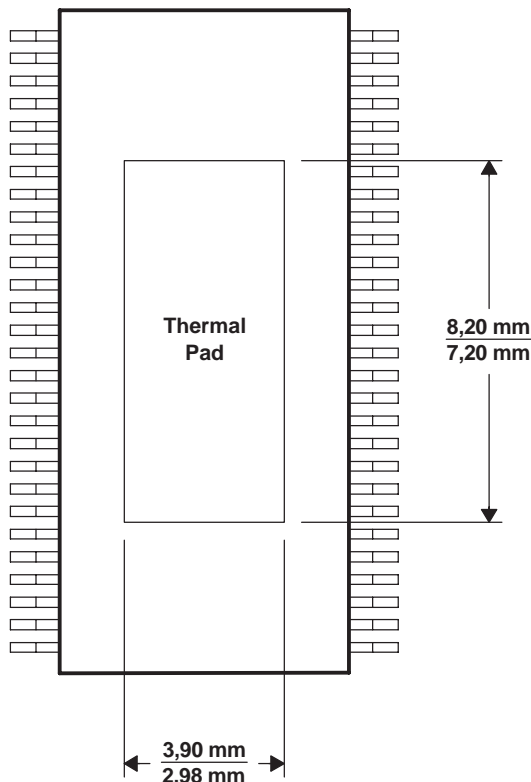


Figure 15. Thermal Pad Dimensions for DFD and DCA Packages

CLICK AND POP REDUCTION

TI modulators feature a pop and click reduction system that controls the timing when switching starts and stops.

Going from non-switching to switching operation causes a spectral energy burst to occur within the audio bandwidth, which is heard in the speaker as an audible click, for instance, after having asserted **RESET** LH during a system start-up.

To make this system work properly, the following design rules must be followed when using the TAS5122 power stage:

- The relative timing between the PWM_AP/M_x signals and their corresponding VALID_x signal should not be skewed by inserting delays, because this increases the audible amplitude level of the click.
- The output stage must start switching from a fully discharged output filter capacitor. Because

the output stage prior to operation is in the high-impedance state, this is done by having a passive pulldown resistor on each speaker output to GND (see *System Configuration Used for Characterization*).

Other things that can affect the audible click level:

- The spectrum of the click seems to follow the speaker impedance vs frequency curve—the higher the impedance, the higher the click energy.
- Crossover filters used between woofer and tweeter in a speaker can have high impedance in the audio band, which should be avoided if possible.

Another way to look at it is that the speaker impulse response is a major contributor to how the click energy is shaped in the audio band and how audible the click is.

The following mode transitions feature click and pop reduction in Texas Instruments PWM processors.

STATE	CLICK AND POP REDUCED
Normal(1) → Mute	Yes
Mute → Normal(1)	Yes
Normal(1) → Error recovery (ERRCVY)	Yes
Error recovery → Normal(1)	Yes
Normal(1) → Hard Reset	No
Hard Reset → Normal(1)	Yes

(1) Normal = switching

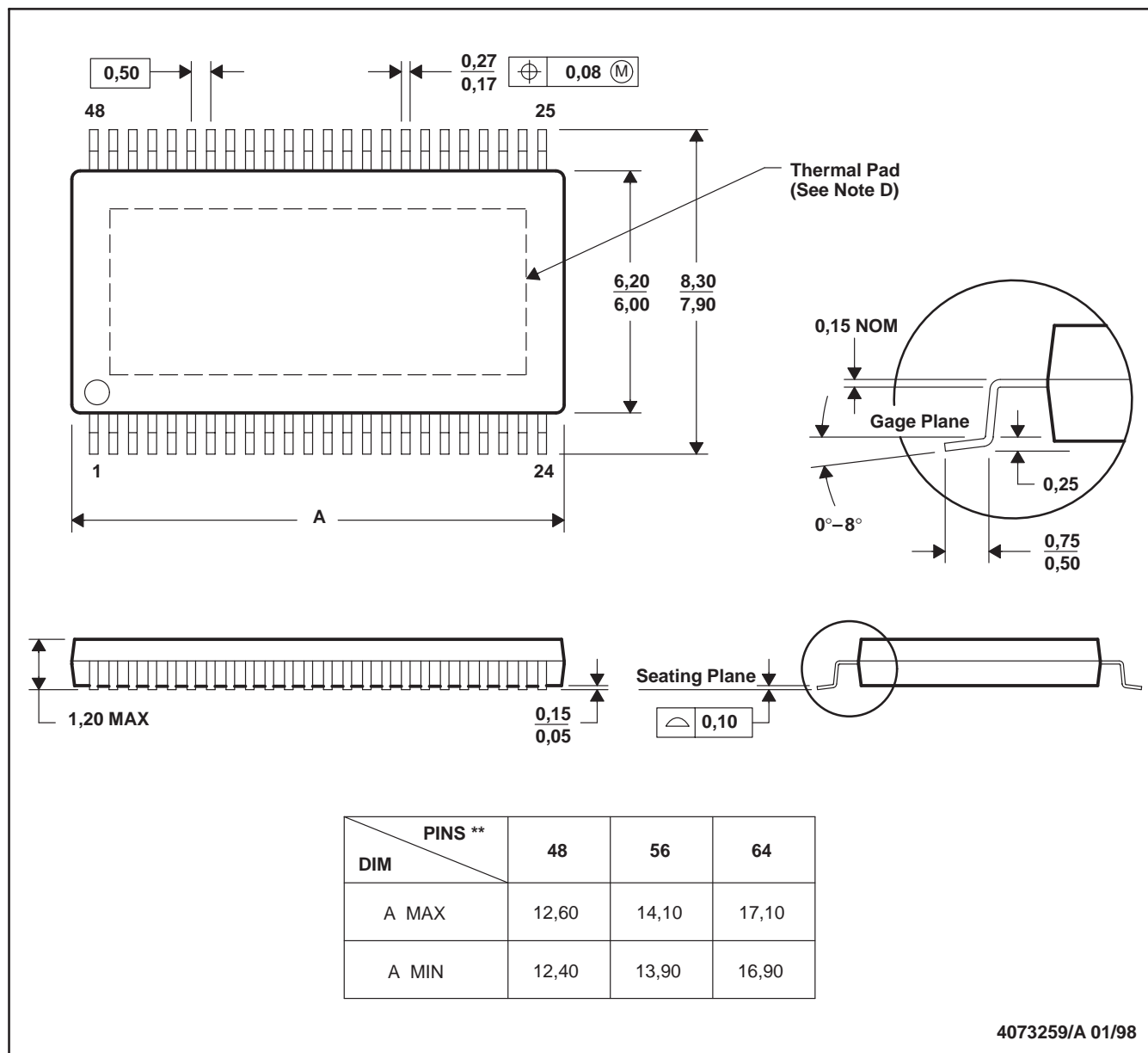
REFERENCES

1. *TAS5000 Digital Audio PWM Processor* data manual – TI (SLAS270)
2. *True Digital Audio Amplifier TAS5001 Digital Audio PWM Processor* data sheet – TI (SLES009)
3. *True Digital Audio Amplifier TAS5010 Digital Audio PWM Processor* data sheet – TI (SLAS328)
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9. *System Design Considerations for True Digital Audio Power Amplifiers* application report – TI (SLAA117)

DCA (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments Incorporated.

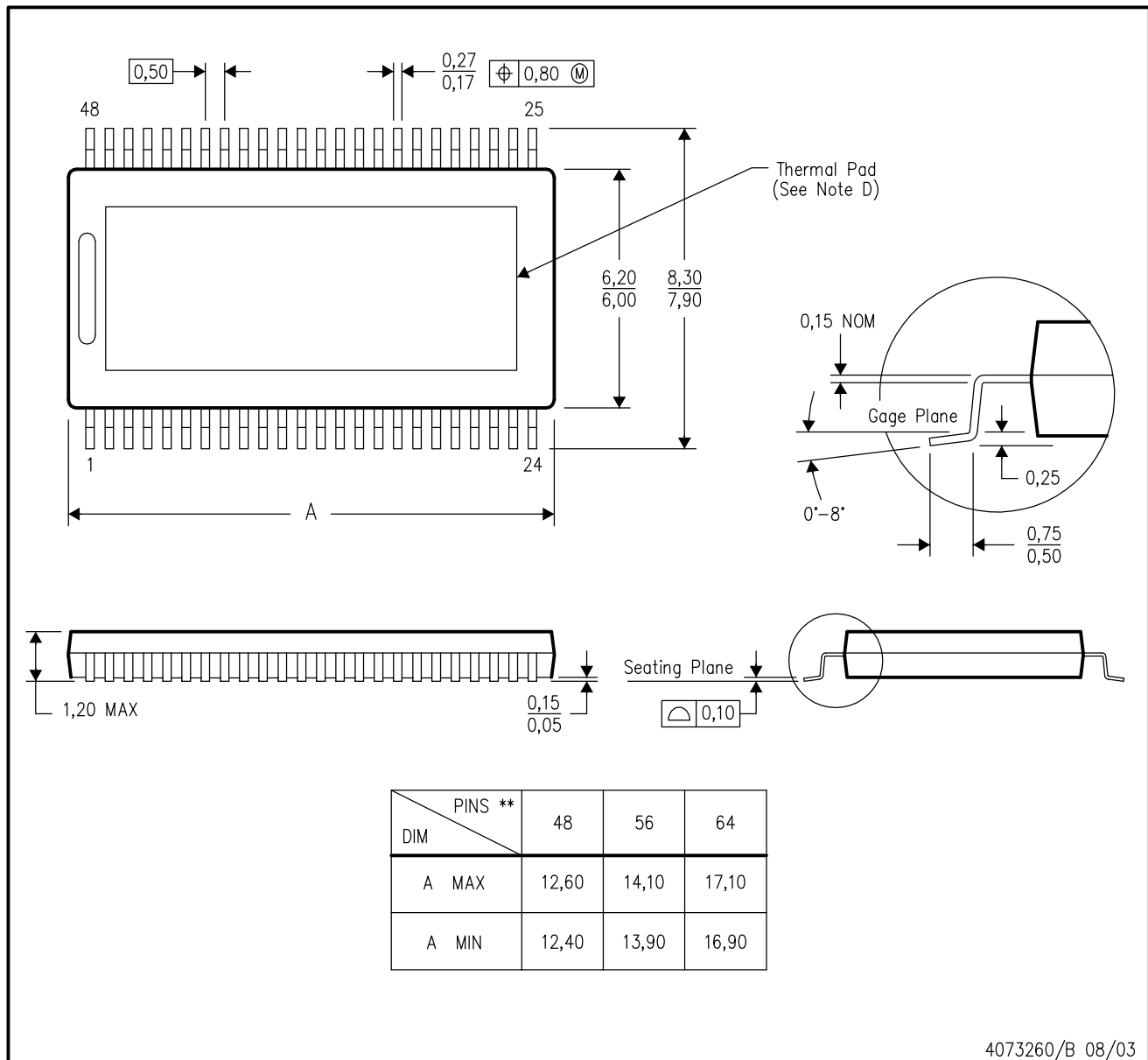


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DFD (R-PDSO-G**)

48 PIN SHOWN

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions include mold flash or protrusion.
 - The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 - Falls within JEDEC MO-153

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