

## FEATURES

- Single-Chip Mixer/Oscillator and PLL Synthesizer
- Three-Band Local Oscillator
- I<sup>2</sup>C Bus Protocol (Bidirectional Data Transmission)
- 30-V Tuning Voltage Output
- Four NPN-Type Band-Switch Drivers
- Programmable Reference Divider Ratio (512, 640, or 1024 )
- 5-V Power Supply
- 30-Pin TSSOP Package

## APPLICATIONS

- TV
- VCR/DVD Recorder
- Set-Top Box

## DESCRIPTION

The SN761681 is a synthesized tuner IC designed for TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, 30-V output tuning amplifier, four NPN band-switch drivers, and is available in a small-outline package. A 15-bit programmable counter and reference divider are controlled by I<sup>2</sup>C bus protocol. Tuning step frequency is selectable by this reference divider ratio for a crystal oscillator.

**DBT PACKAGE  
(TOP VIEW)**

VHI OSC C	1	30	UHF RF IN2
VHI OSC B	2	29	UHF RF IN1
OSC GND	3	28	VHF RF IN
VLO OSC C	4	27	RF GND
VLO OSC B	5	26	MIX OUT2
UHF OSC B1	6	25	MIX OUT1
UHF OSC C1	7	24	BS4
UHF OSC C2	8	23	BS2
UHF OSC B2	9	22	BS1
IF GND	10	21	BS3
VCC	11	20	ADC
IF OUT1	12	19	AS
IF OUT2	13	18	SDA
CP	14	17	SCL
VTU	15	16	XTAL

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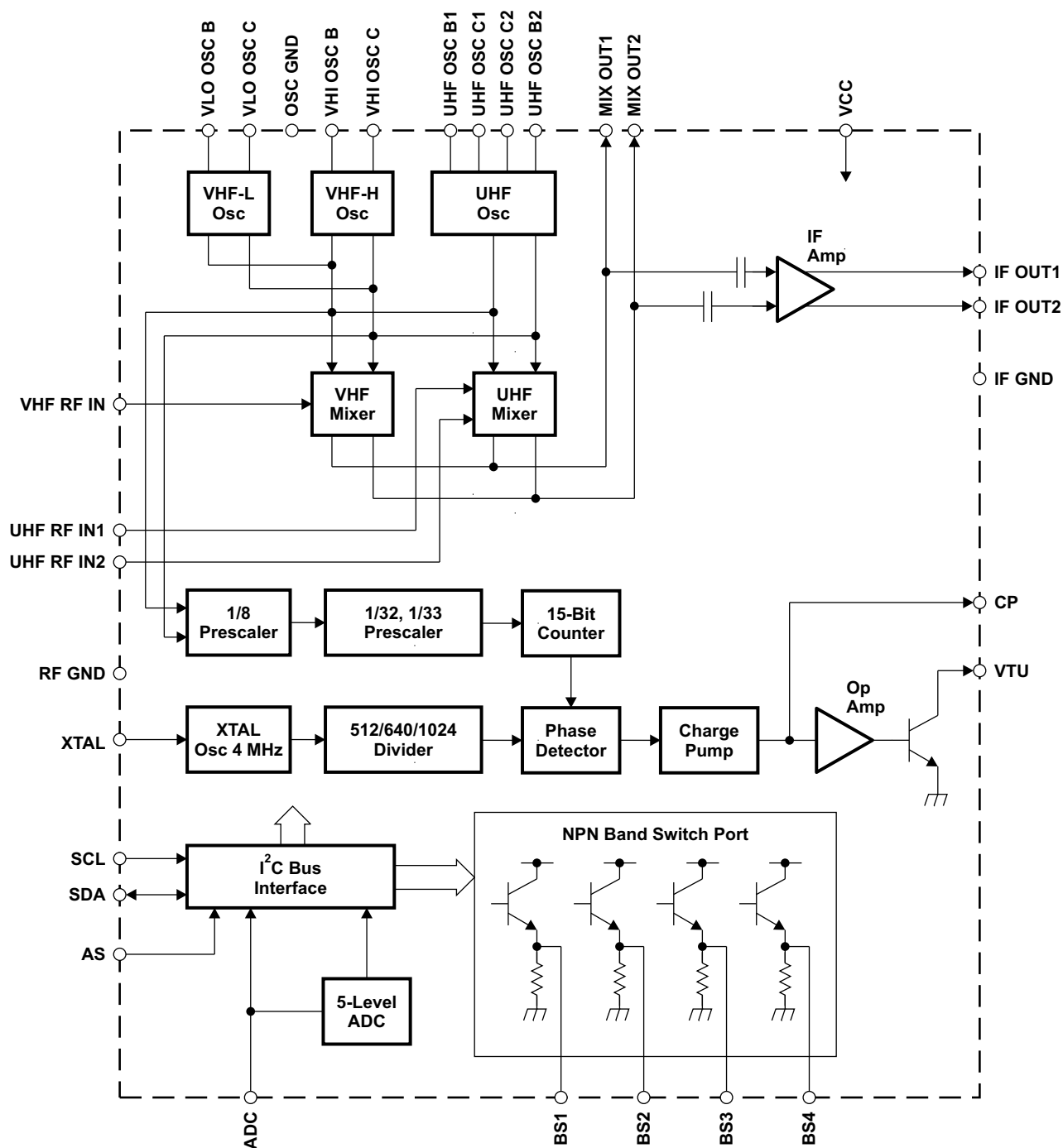


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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

## Functional Block Diagram



B0089-02

## Pin Assignments

### Pin Description

TERMINAL		DESCRIPTION	SCHEMATIC
NAME	NO.		
ADC	20	ADC input	<a href="#">Figure 1</a>
AS	19	Address selection input	<a href="#">Figure 2</a>
BS1	22	Band switch1 output (NPN emitter follower)	<a href="#">Figure 3</a>
BS2	23	Band switch2 output (NPN emitter follower)	<a href="#">Figure 3</a>
BS3	21	Band switch3 output (NPN emitter follower)	<a href="#">Figure 3</a>
BS4	24	Band switch4 output (NPN emitter follower)	<a href="#">Figure 3</a>
CP	14	Charge pump output	<a href="#">Figure 4</a>
IF GND	10	IF ground	
IF OUT1	12	IF output	<a href="#">Figure 5</a>
IF OUT2	13	IF output	<a href="#">Figure 5</a>
MIX OUT1	25	Mixer output	<a href="#">Figure 6</a>
MIX OUT2	26	Mixer output	<a href="#">Figure 6</a>
OSC GND	3	Oscillator ground	
RF GND	27	RF ground	
SCL	17	Serial clock input	<a href="#">Figure 7</a>
SDA	18	Serial data input/output	<a href="#">Figure 8</a>
UHF OSC B1	6	UHF oscillator base1	<a href="#">Figure 9</a>
UHF OSC B2	9	UHF oscillator base2	<a href="#">Figure 9</a>
UHF OSC C1	7	UHF oscillator collector1	<a href="#">Figure 9</a>
UHF OSC C2	8	UHF oscillator collector2	<a href="#">Figure 9</a>
UHF RF IN1	29	UHF RF input	<a href="#">Figure 10</a>
UHF RF IN2	30	UHF RF input	<a href="#">Figure 10</a>
VCC	11	Supply voltage for mixer/oscillator/PLL: 5-V	
VHF RF IN	28	VHF RF input	<a href="#">Figure 11</a>
VHI OSC B	2	VHF HIGH oscillator base	<a href="#">Figure 12</a>
VHI OSC C	1	VHF HIGH oscillator collector	<a href="#">Figure 12</a>
VLO OSC B	5	VHF LOW oscillator base	<a href="#">Figure 13</a>
VLO OSC C	4	VHF LOW oscillator collector	<a href="#">Figure 13</a>
VTU	15	Tuning voltage amplifier output	<a href="#">Figure 14</a>
XTAL	16	4-MHz crystal oscillator input	<a href="#">Figure 15</a>

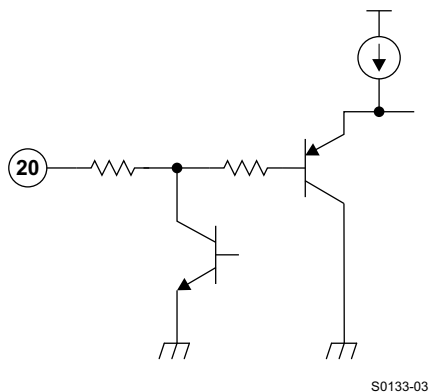


Figure 1.

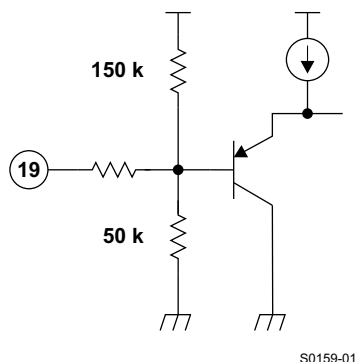


Figure 2.

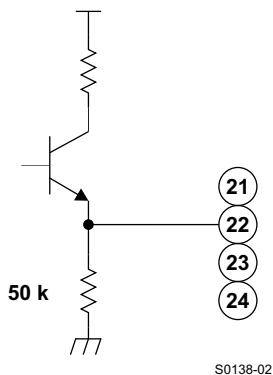


Figure 3.

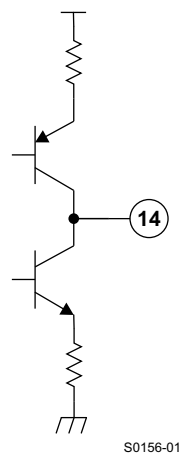


Figure 4.

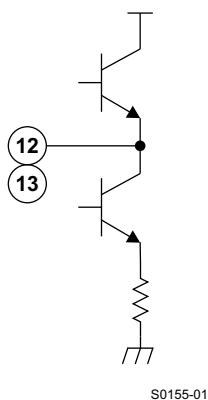


Figure 5.

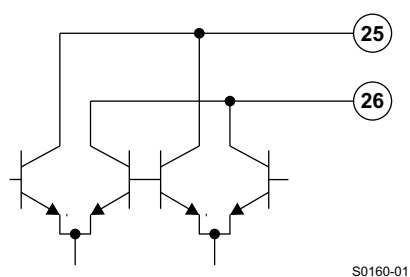


Figure 6.

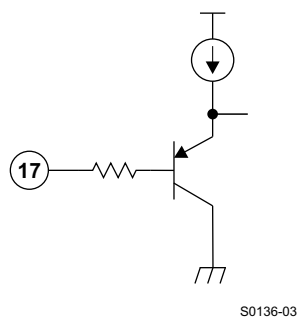


Figure 7.

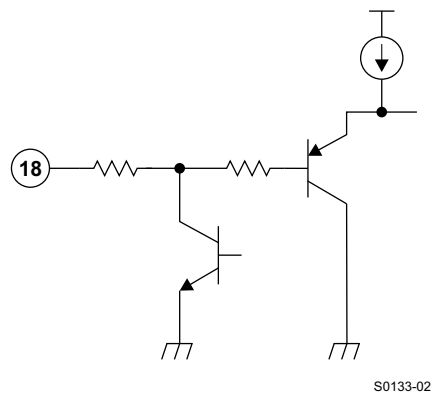
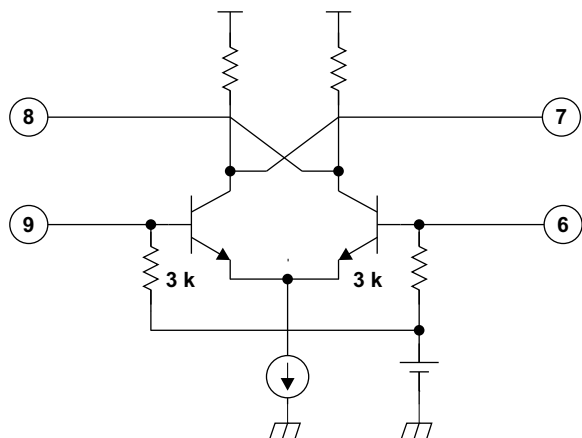
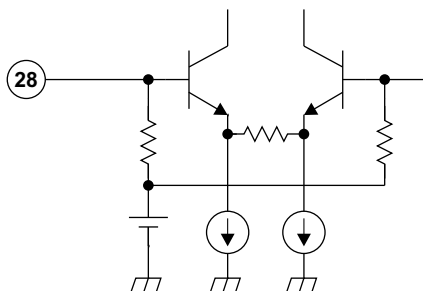


Figure 8.



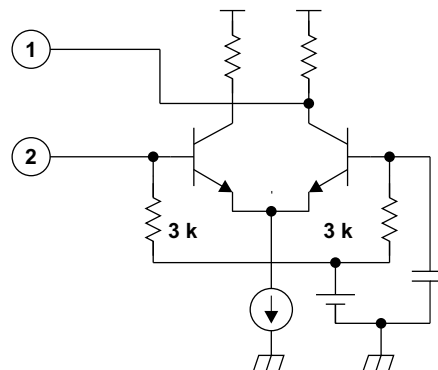
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Figure 9.



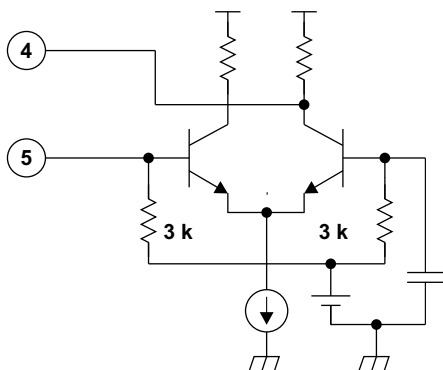
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Figure 10.



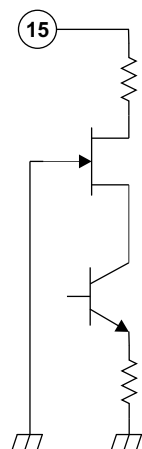
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Figure 11.



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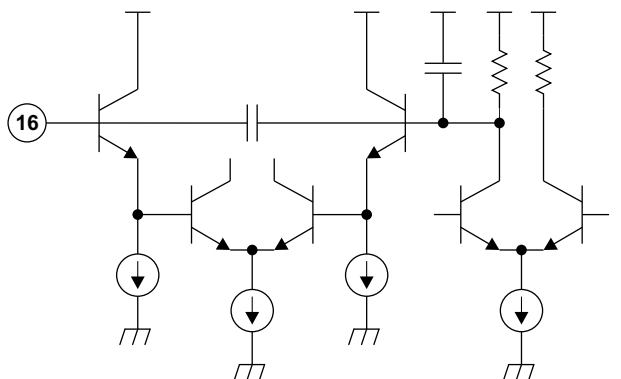
Figure 12.



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Figure 13.

Figure 14.



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Figure 15.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

Supply voltage, $V_{CC}$ <sup>(2)</sup>	$V_{CC}$ (Pin 11)	–0.4 V to 6.5 V
Input voltage 1, $V_{GND}$ <sup>(2)</sup>	RF GND, OSC GND (Pins 3, 27)	–0.4 V to 0.4 V
Input voltage 2, $V_{VTU}$ <sup>(2)</sup>	VTU	–0.4 V to 35 V
Input voltage 3, $V_{IN}$ <sup>(2)</sup>	Other pins (Pins 1, 2, 4–9, 12–14, 16–26, 28–30)	–0.4 V to 6.5 V
Continuous total dissipation, $P_D$ <sup>(3)</sup>	$T_A \leq 25^\circ\text{C}$	1071 mW
Operating free-air temperature, $T_A$		–20°C to 85°C
Storage temperature range, $T_{stg}$		–65°C to 150°C
Maximum junction temperature, $T_J$		150°C
Maximum short-circuit time, $t_{SC(max)}$	Each pin to $V_{CC}$ or to GND	10 s

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage values are with respect to the IF GND of the circuit.
- (3) Derating factor is 8.57 mW/°C for  $T_A \geq 25^\circ\text{C}$ .

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.5	5	5.5	V
Tuning supply voltage, $V_{TU}$			30	33	V
Output current of band switch, $I_{BS}$	One port on			10	mA
Operating free-air temperature, $T_A$		–20		85	°C

## ELECTRICAL CHARACTERISTICS, Total Device and Serial Interface

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -20^\circ\text{C to }85^\circ\text{C}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC1}$	Supply current 1			60		mA
$I_{CC2}$	Supply current 2	One band switch on ( $I_{BS} = 10\text{ mA}$ )		70		mA
$V_{IH}$	High-level input voltage (SCL, SDA)		2.8		$V_{CC}$	V
$V_{IL}$	Low-level input voltage (SCL, SDA)				1.4	V
$I_{IH}$	High-level input current (SCL, SDA)				10	$\mu\text{A}$
$I_{IL}$	Low-level input current (SCL, SDA)		-10			$\mu\text{A}$
$V_{POR}$	Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode)		2.1	2.8	3.5	V
<b>I<sup>2</sup>C INTERFACE</b>						
$V_{ASH}$	Address-select high-input voltage (AS)	$V_{CC} = 5\text{ V}$	4.5		5	V
$V_{ASM1}$	Address-select mid1-input voltage (AS)	$V_{CC} = 5\text{ V}$	2		3	V
$V_{ASM2}$	Address-select mid2-input voltage (AS)	$V_{CC} = 5\text{ V}$	1		1.5	V
$V_{ASL}$	Address-select low-input voltage (AS)	$V_{CC} = 5\text{ V}$			0.5	V
$I_{ASH}$	Address-select high-input current (AS)				140	$\mu\text{A}$
$I_{ASL}$	Address-select low-input current (AS)		-50			$\mu\text{A}$
$V_{ADC}$	ADC input voltage	See <a href="#">Table 8</a>	0		$V_{CC}$	V
$I_{ADH}$	ADC high-level input current	$V_{ADC} = V_{CC}$			10	$\mu\text{A}$
$I_{ADL}$	ADC low-level input current	$V_{ADC} = 0\text{ V}$	-50			$\mu\text{A}$
$V_{OL}$	Low-level output voltage (SDA)	$V_{CC} = 5\text{ V}$ , $I_{OL} = 3\text{ mA}$			0.4	V
$I_{SDAH}$	High-level output leakage current (SDA)	$V_{SDA} = 5.5\text{ V}$			10	$\mu\text{A}$
$f_{SCL}$	Clock frequency (SCL)			100	400	kHz
<b>I<sup>2</sup>C Timing (see timing chart, <a href="#">Figure 16</a>)</b>						
$t_{hd(DAT)}$	Data hold time		0			$\mu\text{s}$
$t_{(BUF)}$	Bus free time		1.3			$\mu\text{s}$
$t_{hd(STA)}$	Start hold time		0.6			$\mu\text{s}$
$t_{(Low)}$	SCL-low hold time		1.3			$\mu\text{s}$
$t_{(High)}$	SCL-high hold time		0.6			$\mu\text{s}$
$t_{su(STA)}$	Start setup time		0.6			$\mu\text{s}$
$t_{su(DAT)}$	Data setup time		0.1			$\mu\text{s}$
$t_r$	SCL, SDA rise time				0.3	$\mu\text{s}$
$t_f$	SCL, SDA fall time				0.3	$\mu\text{s}$
$t_{su(STO)}$	Stop setup time		0.6			$\mu\text{s}$

## ELECTRICAL CHARACTERISTICS, PLL and Band Switch

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -20^\circ\text{C to }85^\circ\text{C}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	256		32767	
$f_{XTAL}$	Crystal oscillator frequency	$R_{XTAL} = 25\ \Omega \text{ to } 300\ \Omega$	3.2	4	4.48	MHz
$Z_{XTAL}$	Crystal oscillator input impedance			1.6		k $\Omega$
$V_{IXTAL2}$	Minimum reference input sensitivity (XTAL)	4 MHz, ac coupling with 0.1 $\mu\text{F}$ capacitor			100	mVp-p
$V_{VTUL}$	Tuning amplifier low-level output voltage	$R_L = 22\text{ k}\Omega$ , $V_{TU} = 33\text{ V}$	0.3	0.4	0.5	V
$I_{VTUOFF}$	Tuning amplifier leakage current (off)	OS = 1, $V_{TU} = 33\text{ V}$			10	$\mu\text{A}$
$I_{CPH}$	Charge-pump high-level input current	CP = 1		280		$\mu\text{A}$
$I_{CPL}$	Charge-pump low-level input current	CP = 0		60		$\mu\text{A}$
$V_{CP}$	Charge-pump output voltage	PLL locked		1.95		V
$I_{CPOFF}$	Charge-pump leakage current	T2 = 0, T1 = 1, $V_{CP} = 2\text{ V}$ , $T_A = 25^\circ\text{C}$	-15		15	nA
$I_{BS}$	Band-switch driver output current				10	mA
$V_{BS1}$	Band-switch driver output voltage	$I_{BS} = 10\text{ mA}$	3			V
$V_{BS2}$		$I_{BS} = 10\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$	3.5	3.9		
$I_{BSOFF}$	Band-switch driver leakage current	$V_{BS} = 0\text{ V}$			3	$\mu\text{A}$

## ELECTRICAL CHARACTERISTICS, Mixer, Oscillator, IF Amplifier

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in Figure 17 reference measurement circuit at 50- $\Omega$  system,  
IF filter characteristics:  $f_{\text{peak}} = 43\text{ MHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G <sub>c1</sub>	Conversion gain (mixer-IF amplifier), VHF-LOW	f <sub>in</sub> = 58 MHz <sup>(1)</sup>	22	25	28	dB
G <sub>c3</sub>		f <sub>in</sub> = 130 MHz <sup>(1)</sup>	22	25	28	
G <sub>c4</sub>	Conversion gain (mixer-IF amplifier), VHF-HIGH	f <sub>in</sub> = 136 MHz <sup>(1)</sup>	22	25	28	dB
G <sub>c6</sub>		f <sub>in</sub> = 364 MHz <sup>(1)</sup>	22	25	28	
G <sub>c7</sub>	Conversion gain (mixer-IF amplifier), VHF-UHF	f <sub>in</sub> = 370 MHz <sup>(1)</sup>	26	29	32	dB
G <sub>c9</sub>		f <sub>in</sub> = 804 MHz <sup>(1)</sup>	25	28	31	
NF <sub>1</sub>	Noise figure, VHF-LOW	f <sub>in</sub> = 55.25 MHz		9.5		dB
NF <sub>3</sub>		f <sub>in</sub> = 127.25 MHz		9.5		
NF <sub>4</sub>	Noise figure, VHF-HIGH	f <sub>in</sub> = 133.25 MHz		10		dB
NF <sub>6</sub>		f <sub>in</sub> = 361.25 MHz		10		
NF <sub>7</sub>	Noise figure, UHF	f <sub>in</sub> = 367.25 MHz		11		dB
NF <sub>9</sub>		f <sub>in</sub> = 801.25 MHz		11		
CM <sub>1</sub>	1% cross-modulation distortion, VHF-LOW	f <sub>in</sub> = 55.25 MHz <sup>(2)</sup>		89		dBμV
CM <sub>3</sub>		f <sub>in</sub> = 127.25 MHz <sup>(2)</sup>		89		
CM <sub>4</sub>	1% cross-modulation distortion, VHF-HIGH	f <sub>in</sub> = 133.25 MHz <sup>(2)</sup>		86		dBμV
CM <sub>6</sub>		f <sub>in</sub> = 361.25 MHz <sup>(2)</sup>		86		
CM <sub>7</sub>	1% cross-modulation distortion, UHF	f <sub>in</sub> = 367.25MHz <sup>(2)</sup>		87		dBμV
CM <sub>9</sub>		f <sub>in</sub> = 801.25 MHz <sup>(2)</sup>		87		
V <sub>IFO1</sub>	IF output voltage, VHF-LOW	f <sub>in</sub> = 55.25 MHz <sup>(3)</sup>		117		dBμV
V <sub>IFO3</sub>		f <sub>in</sub> = 127.25 MHz <sup>(3)</sup>		117		
V <sub>IFO4</sub>	IF output voltage, VHF-HIGH	f <sub>in</sub> = 133.25 MHz <sup>(3)</sup>		117		dBμV
V <sub>IFO6</sub>		f <sub>in</sub> = 361.25 MHz <sup>(3)</sup>		117		
V <sub>IFO7</sub>	IF output voltage, UHF	f <sub>in</sub> = 367.25MHz <sup>(3)</sup>		117		dBμV
V <sub>IFO9</sub>		f <sub>in</sub> = 801.25 MHz <sup>(3)</sup>		117		
Φ <sub>OSC1</sub>	Phase noise, VHF-LOW	f <sub>in</sub> = 55.25 MHz <sup>(4)</sup>		88		dBc/Hz
Φ <sub>OSC3</sub>		f <sub>in</sub> = 127.25 MHz <sup>(4)</sup>		88		
Φ <sub>OSC4</sub>	Phase noise, VHF-HIGH	f <sub>in</sub> = 133.25 MHz <sup>(4)</sup>		86		dBc/Hz
Φ <sub>OSC6</sub>		f <sub>in</sub> = 361.25 MHz <sup>(4)</sup>		86		
Φ <sub>OSC7</sub>	Phase noise, UHF	f <sub>in</sub> = 367.25MHz <sup>(4)</sup>		84		dBc/Hz
Φ <sub>OSC9</sub>		f <sub>in</sub> = 801.25 MHz <sup>(4)</sup>		84		
Prescaler beat <sup>(5)</sup>					25	dBμV

- (1) IF = 43 MHz, RF input level = 80 dB $\mu$ V
- (2)  $f_{\text{undes}} = f_{\text{des}} \pm 6\text{ MHz}$ ,  $P_{\text{in}} = 80\text{ dB}\mu\text{V}$ , AM 1 kHz, 30%, DES/CM = S/I = 46 dB
- (3) IF = 45.75 MHz
- (4) Offset = 10 kHz, RF input level = 70 dB $\mu$ V
- (5) Design parameter, not tested

## Functional Description

### I<sup>2</sup>C Bus Mode

#### I<sup>2</sup>C Write Mode ( $R/\overline{W} = 0$ )

**Table 1. Write Data Format**

	MSB							LSB	(1)
Address byte (ADB)	1	1	0	0	0	MA1	MA0	$R/\overline{W} = 0$	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Band-switch byte (BB)	X	X	X	X	BS4	BS3	BS2	BS1	A

(1) A: Acknowledge

**Table 2. Description of Data Symbols**

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address-set bits (see <a href="#">Table 3</a> , <i>Address Selection</i> )	
N[14:0]	Programmable counter set bits $N = N14 \times 2^{14} + N13 \times 2^{13} + \dots + N1 \times 2 + N0$ Oscillation frequency = $f_r \times 8 \times N$ $f_r$ = Reference frequency = 4 MHz/Reference divider	$N14 = N13 = N12 = \dots = N0 = 0$
CP	Charge-pump current-set bit 60 $\mu$ A (CP = 0), 280 $\mu$ A (CP = 1)	CP = 1
T[2:0]	TEST bits (see <a href="#">Table 4</a> , <i>Test Bits</i> ) Normal mode: T2 = 0, T1 = 0, T0 = 1/0	T[2:0] = 001
RSA, RSB	Reference divider ratio selection bits See Table 6, Reference Divider Ratio.	RSA = 0, RSB = 1
OS	Tuning amplifier control bit Tuning voltage on (OS = 0) Tuning voltage off, high impedance (OS = 1)	OS = 0
BS[4:1]	Band-switch control bits $BSn = 0: Tr = OFF \quad BSn = 1: Tr = ON$ Band selection by BS1, BS2, BS4 <b>BS1(VL)   BS2(VH)   BS4(U)</b> 1        0        0    VHF-LO X        1        0    VHF-HI X        X        1    UHF	$BSn = 0$
X	Don't care	

**Table 3. Address Selection**

MA1	MA0	Voltage Applied on AS Input
0	0	LOW: 0 V to 0.1 V <sub>CC</sub>
0	1	MID2: open, or 0.2 V <sub>CC</sub> to 0.3 V <sub>CC</sub>
1	0	MID1: 0.4 V <sub>CC</sub> to 0.6 V <sub>CC</sub>
1	1	HIGH: 0.9 V <sub>CC</sub> to V <sub>CC</sub>

**Table 4. Test Bits <sup>(1)</sup>**

T2	T1	T0	Device Operation	Note
0	0	0	Normal operation	
0	0	1	Normal operation	Default
0	1	X	Charge pump is off.	
1	1	0	Charge pump is sink.	
1	1	1	Charge pump is source.	
1	0	X	Test mode	ADC not available

(1) Not used for other bit patterns

**Table 5. Reference Divider Ratio**

RSA	RSB	Reference Divider Ratio
X	0	640
0	1	1024
1	1	512

## I<sup>2</sup>C Read Mode (R/W = 1)

**Table 6. Read Data Format**

	MSB							LSB	(1)
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W = 1	A
Status byte (SB)	POR	FL	1	1	1	A2	A1	A0	–

(1) A: Acknowledge

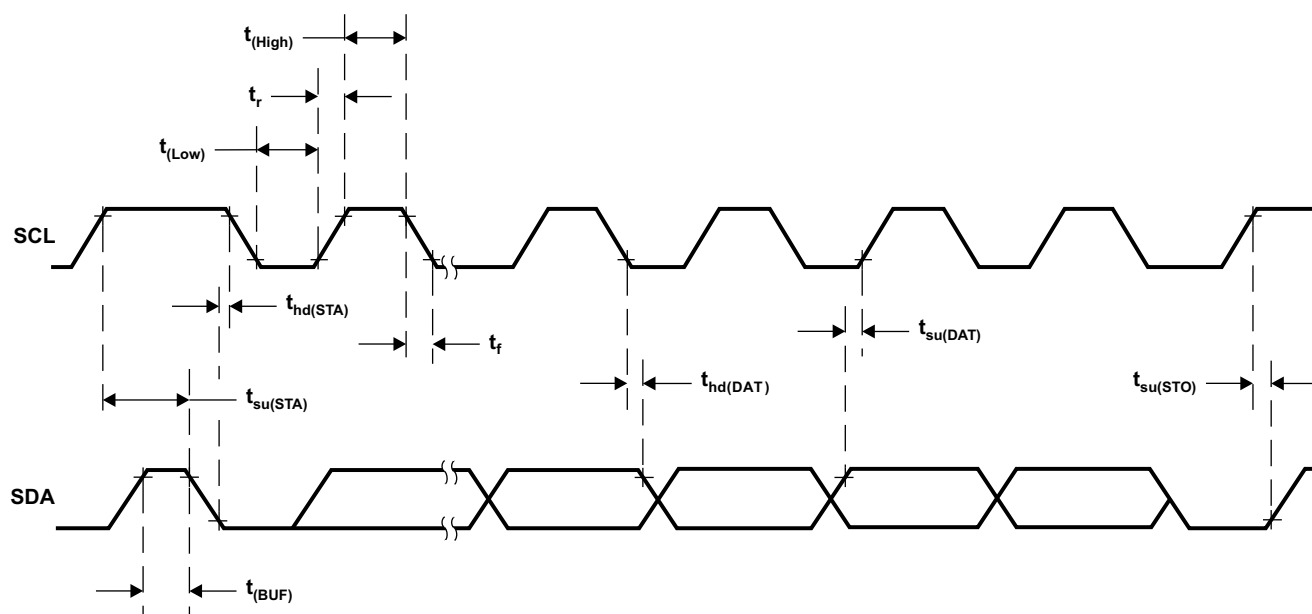
**Table 7. Description of Data Symbols**

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address-set bits (see <a href="#">Table 3</a> , <i>Address Selection</i> )	
POR	Power-on-reset flag POR set: Power on POR reset: End-of-data transmission procedure	POR = 1
FL	In-lock flag PLL locked (FL = 1), PLL unlocked (FL = 0)	
A[2:0]	Digital data of ADC (see <a href="#">Table 8</a> , <i>ADC Level</i> )	

**Table 8. ADC Level**

A2	A1	A0	Voltage Applied on ADC Input <sup>(1)</sup>
1	0	0	0.6 V <sub>CC</sub> to V <sub>CC</sub>
0	1	1	0.45 V <sub>CC</sub> to 0.6 V <sub>CC</sub>
0	1	0	0.3 V <sub>CC</sub> to 0.45 V <sub>CC</sub>
0	0	1	0.15 V <sub>CC</sub> to 0.3 V <sub>CC</sub>
0	0	0	0 V to 0.15 V <sub>CC</sub>

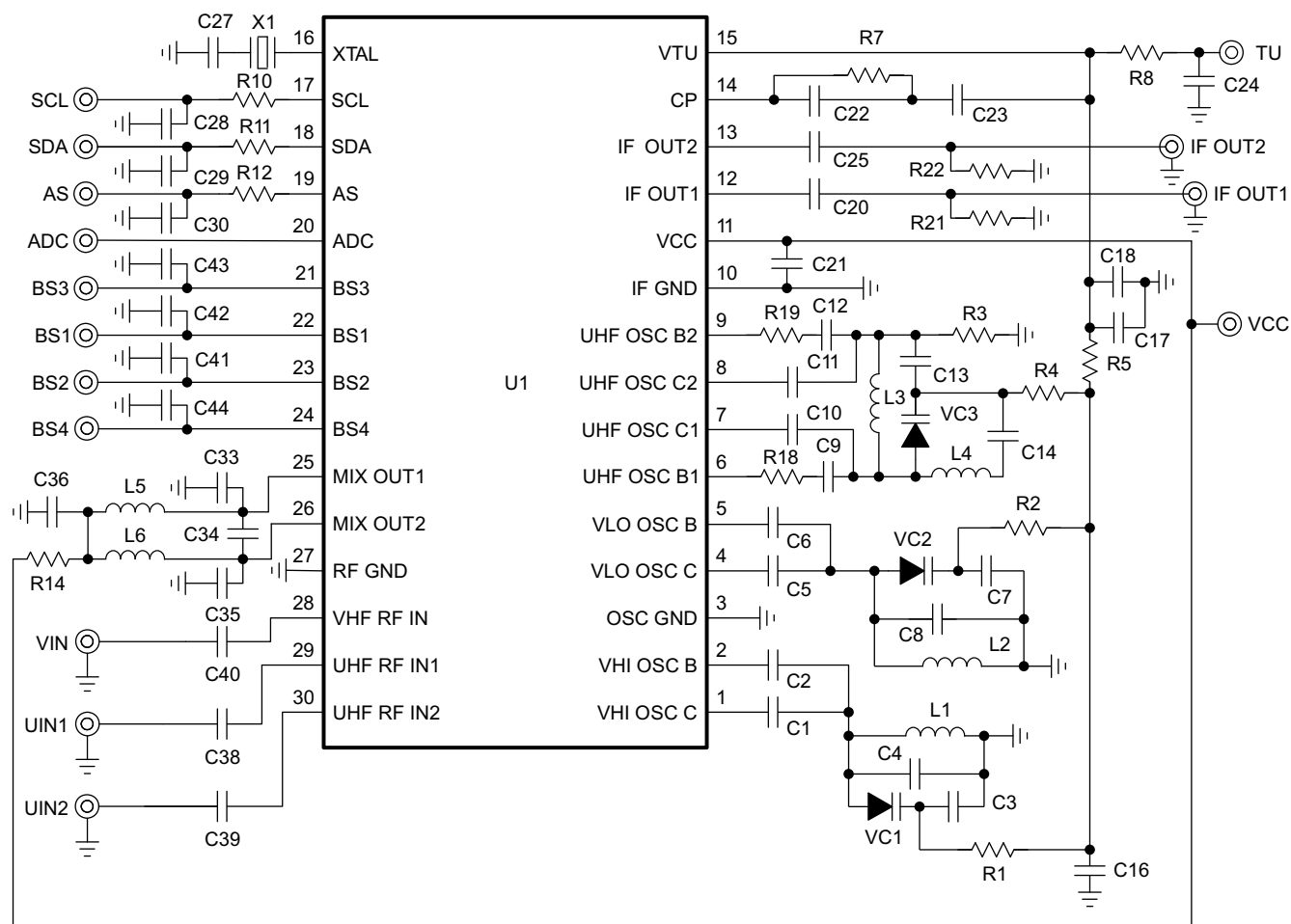
(1) Accuracy is  $0.03 \times V_{CC}$ .



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**Figure 16. I²C Timing Chart**

### Reference Measurement Circuit



S0161-01

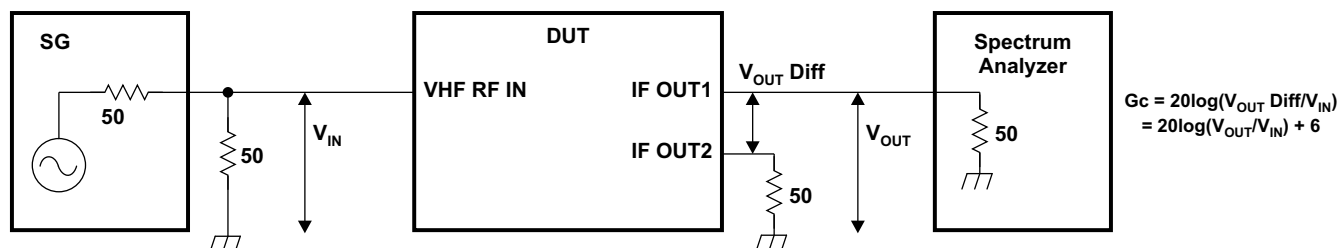
### Figure 17. Reference Measurement Circuit

## APPLICATION INFORMATION (continued)

### Component Values for Measurement Circuit

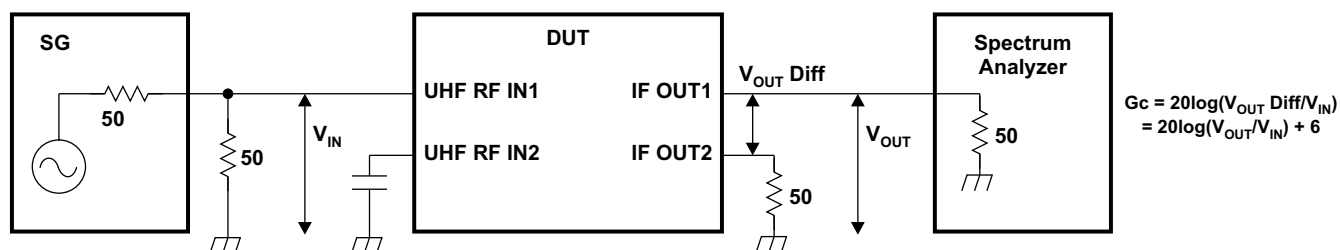
PART NAME	VALUE	PART NAME	VALUE
C1 (VHI OSC C)	3 pF	C39 (UIN2)	2.2 nF
C2 (VHI OSC B)	2 pF	C40 (VIN)	2.2 nF
C3 (VHI OSC)	68 pF	C41 (BS2)	2.2 nF
C4 (VHI OSC)	Open	C42 (BS1)	2.2 nF
C5 (VLO OSC C)	1 pF	C43 (BS3)	2.2 nF
C6 (VLO OSC B)	1 pF	C44 (BS4)	2.2 nF
C7 (VLO OSC)	47 pF	L1 (VHI OSC)	φ2,4 mm, 4T, wire 0,4 mm
C8 (VLO OSC)	3 pF	L2 (VLO OSC)	φ3 mm, 8T, wire 0,32 mm
C9 (UHF OSC B1)	1.5 pF	L3 (UHF OSC)	φ3 mm, 2T, wire 0,4 mm
C10 (UHF OSC C1)	1.5 pF	L4 (UHF OSC)	φ2 mm, 3T, wire 0,4 mm
C11 (UHF OSC C2)	1.5 pF	L5 (MIXOUT)	φ2,4 mm, 16T, wire 0,26 mm
C12 (UHF OSC B2)	1.5 pF	L6 (MIXOUT)	φ2,4 mm, 16T, wire 0,26 mm
C13 (UHF OSC)	12 pF	R1(VHI OSC)	33 kΩ
C14 (UHF OSC)	100 pF	R2 (VLO OSC)	33 kΩ
C16 (VTU)	2.2 nF/50 V	R3 (UHF OSC)	22 kΩ
C17 (VTU)	2.2 nF/50 V	R4 (UHF OSC)	33 kΩ
C18 (VTU)	2.2 nF/50 V	R5 (VTU)	22 kΩ
C20 (IF OUT1)	2.2 nF	R7 (CP)	22 kΩ
C21 (VCC)	4.7 nF	R8 (VTU)	22 kΩ
C22 (CP)	2.2 nF	R10 (SCL)	330 Ω
C23 (CP)	0.1 μF/50 V	R11 (SDA)	330 Ω
C24 (VTU)	2.2 nF/50 V	R12 (AS)	330 Ω
C25 (IF OUT2)	2.2 nF	R14 (MIXOUT)	0
C27 (XTAL)	68 pF	R18 (UHF OSC)	0
C28 (SCL)	Open	R19 (UHF OSC)	0
C29 (SDA)	Open	R21 (IF OUT1)	Open
C30 (AS)	Open	R22 (IF OUT2)	51 Ω
C33 (MIXOUT)	Open	U1	SN761681
C34 (MIXOUT)	22 pF	VC1 (VHI OSC)	1T363A
C35 (MIXOUT)	Open	VC2 (VLO OSC)	1T363A
C36 (MIXOUT)	4.7 nF	VC3 (UHF OSC)	1T363A
C38 (UIN1)	2.2 nF	X1	4-MHz crystal

## Test Circuits



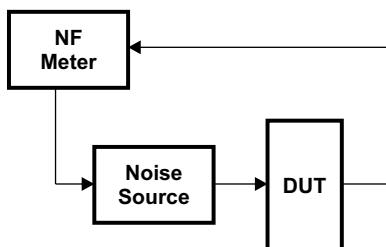
S0144-02

Figure 18. VHF-Conversion Gain-Measurement Circuit



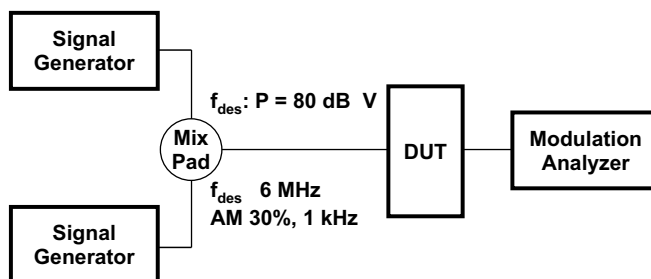
S0145-01

Figure 19. UHF-Conversion Gain-Measurement Circuit



B0090-01

Figure 20. Noise-Figure Measurement Circuit



B0091-01

Figure 21. 1% Cross-Modulation Distortion Measurement Circuit

## TYPICAL CHARACTERISTICS

### Band-Switch Driver Output Voltage (BS1–BS4)

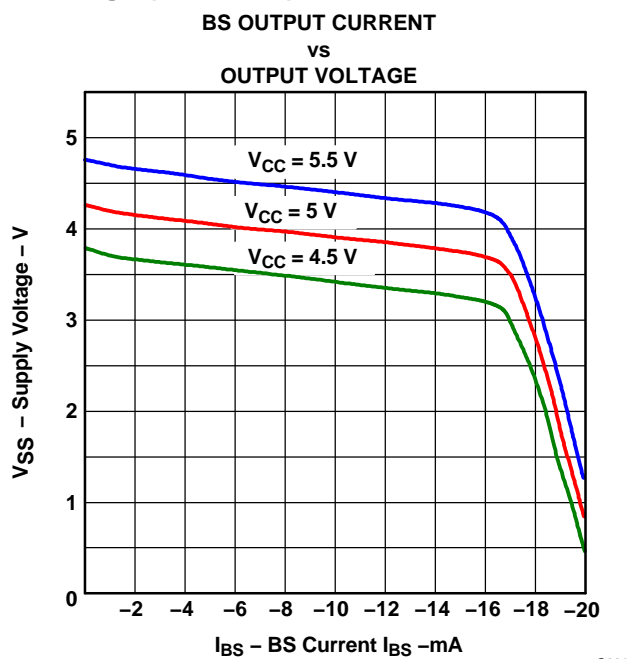


Figure 22. Band-Switch Driver Output Voltage

### S-Parameter

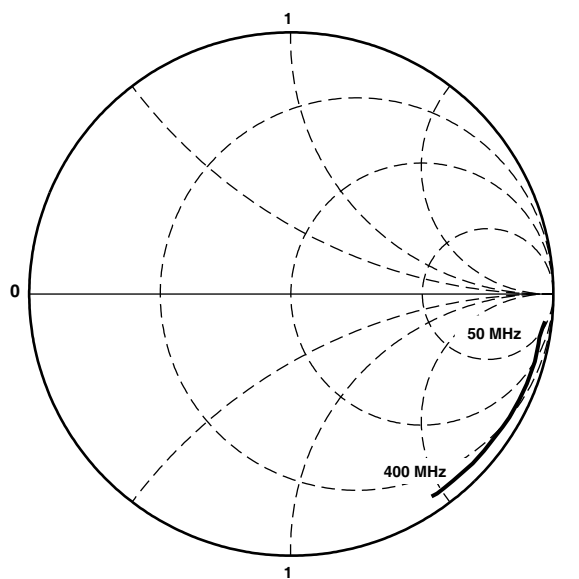
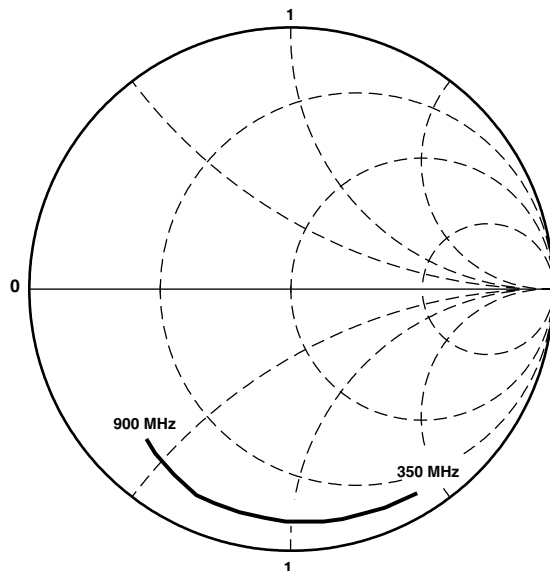


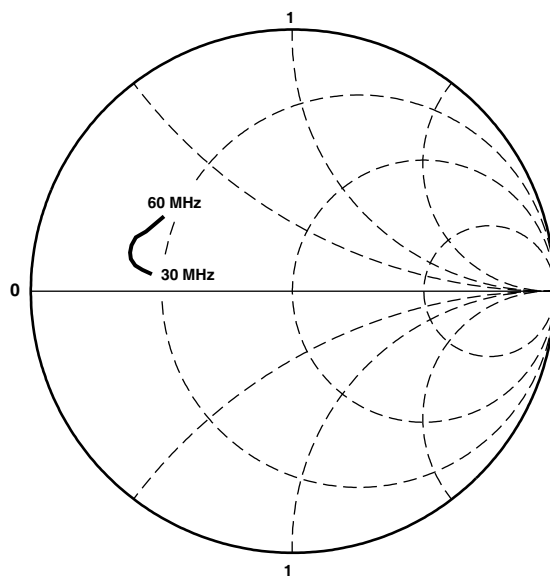
Figure 23. VHF Input

## TYPICAL CHARACTERISTICS (continued)



M0047-05

**Figure 24. UHF Input**



M0047-06

**Figure 25. IF Output**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN761681DBT	OBSOLETE	TSSOP	DBT	30		TBD	Call TI	Call TI	-20 to 85	B1681	
SN761681DBTG4	OBSOLETE	TSSOP	DBT	30		TBD	Call TI	Call TI	-20 to 85		
SN761681DBTR	OBSOLETE	TSSOP	DBT	30		TBD	Call TI	Call TI	-20 to 85	B1681	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

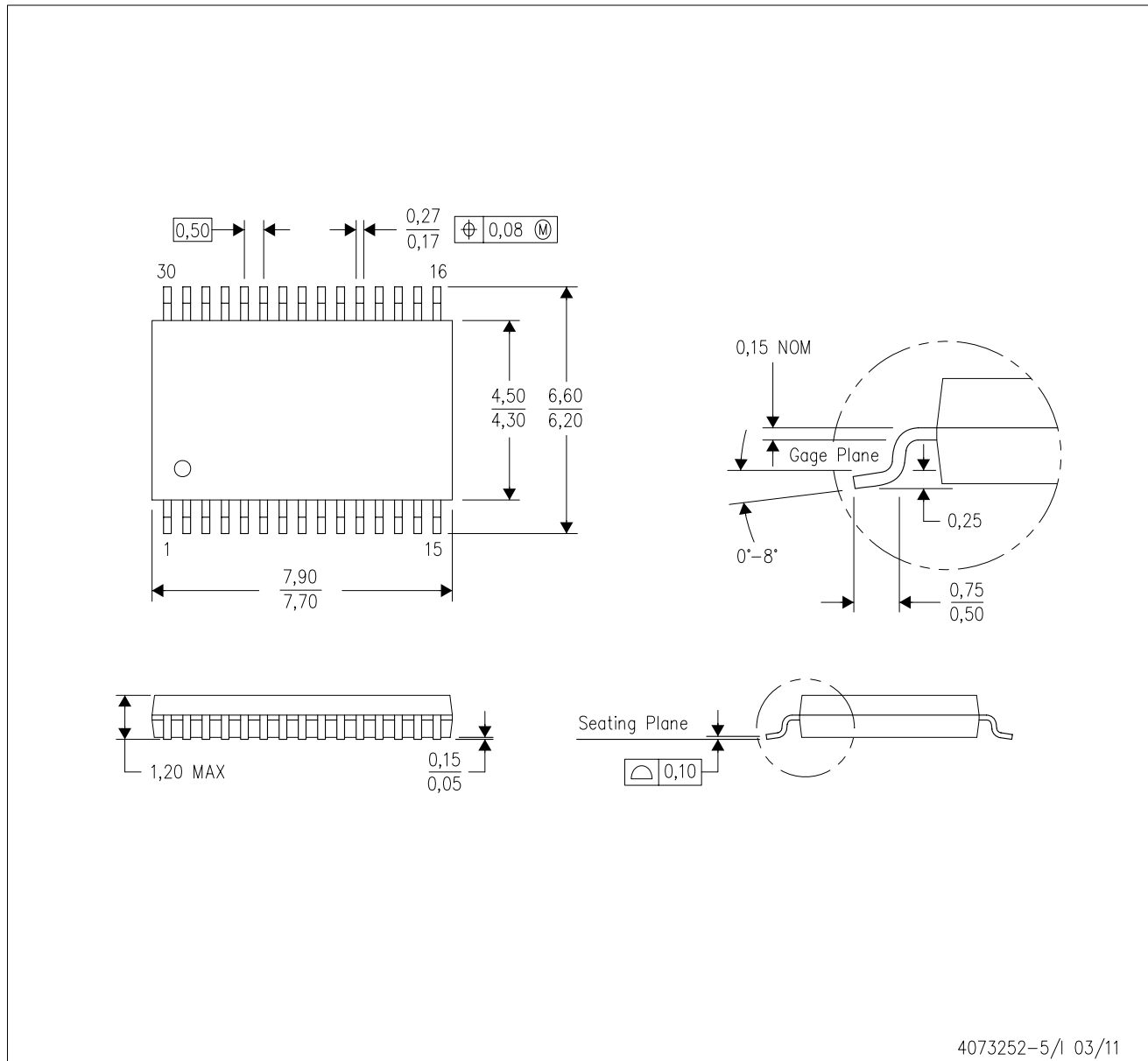
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DBT (R-PDSO-G30)

PLASTIC SMALL OUTLINE



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  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-153.

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