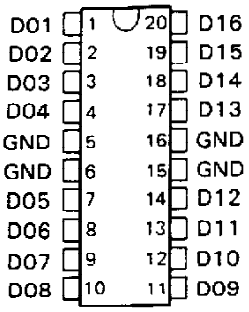
SN74S1052
16-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

SDLS016A D3229, JULY 1989—REVISED MARCH 1990

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 200 mA**
- **16-Bit Array Structure Suited for Bus-Oriented Systems**
- **ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)

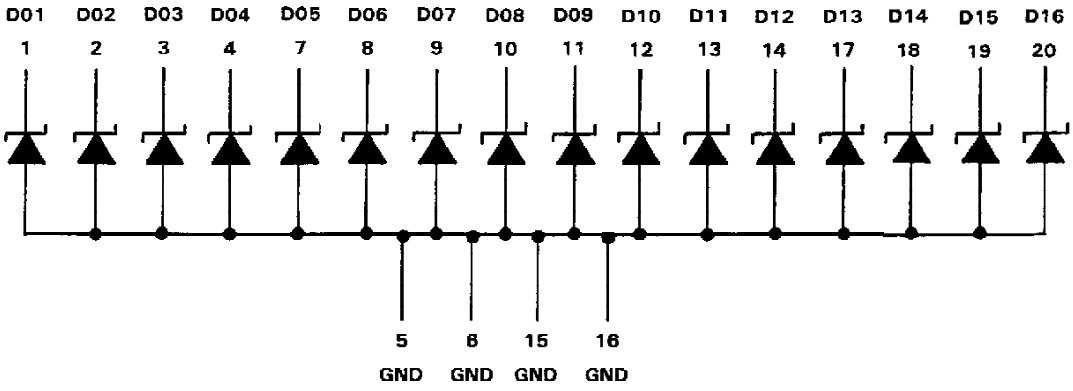


description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1052 is characterized for operation from 0°C to 70°C.

schematic diagram



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R . . . . . 7 V
Continuous forward current, I_F: any D terminal from GND . . . . . 50 mA
total through all GND terminals . . . . . 170 mA
Repetitive peak forward current,‡ I_{FRM}: any D terminal from GND . . . . . 200 mA
total through all GND terminals . . . . . 1 A
Continuous total power dissipation at (or below) 25°C free-air temperature . . . . . 735 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡These values apply for $t_w \leq 100\ \mu s$, duty cycle $\leq 20\%$.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
I_R	Static reverse current	V_R = 7 V			5	μA
V_F	Static forward voltage	I_F = 18 mA		0.75	0.95	V
		I_F = 50 mA		0.95	1.2	
V_{FM}	Peak forward voltage	I_F = 200 mA		1.45		V
C_T	Total capacitance	V_R = 0, f = 1 MHz		5	10	pF
		V_R = 2 V, f = 1 MHz		4	8	

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total I_F = 1 A, See Note 2		0.6	2	mA
		Total I_F = 270 mA, See Note 2		0.02	0.2	

§All typical values are at T_A = 25°C.
NOTE 2. I_X is measured under the following conditions with one diode static and all others switching:
Switching diodes: t_w = 100 μs, duty cycle = 20%; static diode: V_R = 5 V.
The static diode's input current is the internal crosstalk current I_X.

switching characteristics at 25°C free-air temeprature (see Figures 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	I_F = 10 mA, $I_{RM(REC)}$ = 10 mA, $i_{R(REC)}$ = 1 mA, R_L = 100 Ω		8	16	ns

PARAMETER MEASUREMENT INFORMATION

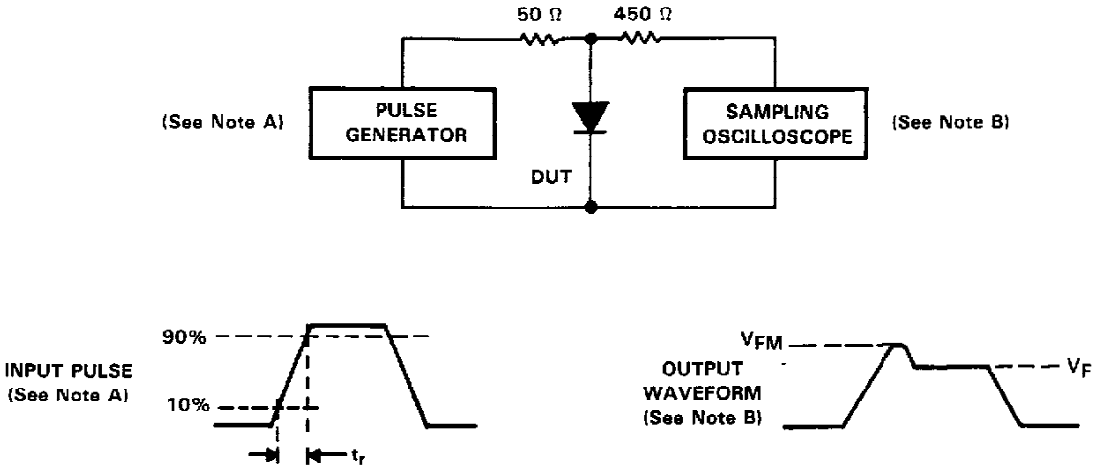


FIGURE 1. FORWARD RECOVERY VOLTAGE

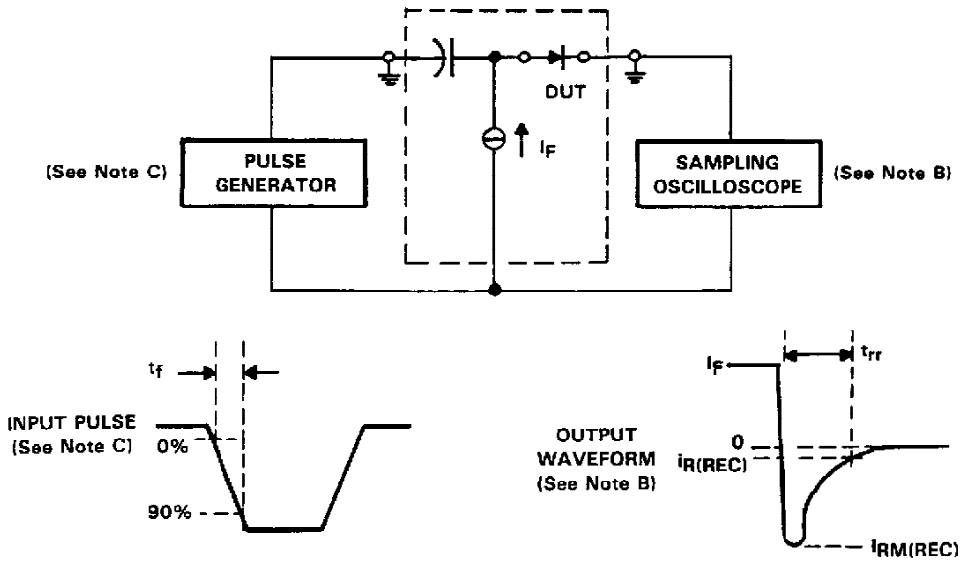


FIGURE 2. REVERSE RECOVERY TIME

NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: t_r = 20 ns, Z_{out} = 50 Ω, f_{PR} = 500 Hz, duty cycle = 0.01.
B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq$ 350 ps, R_{in} = 50 Ω, $C_{in} = \leq$ 5 pF.
C. The input pulse is supplied by a pulse generator having the following characteristics: t_f = 0.5 ns, Z_{out} = 50 Ω, $t_w = \leq$ 50 ns, duty cycle ≥ 0.01.

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 3.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 4 was evaluated. The resulting waveforms with and without the diode are shown in Figure 5.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

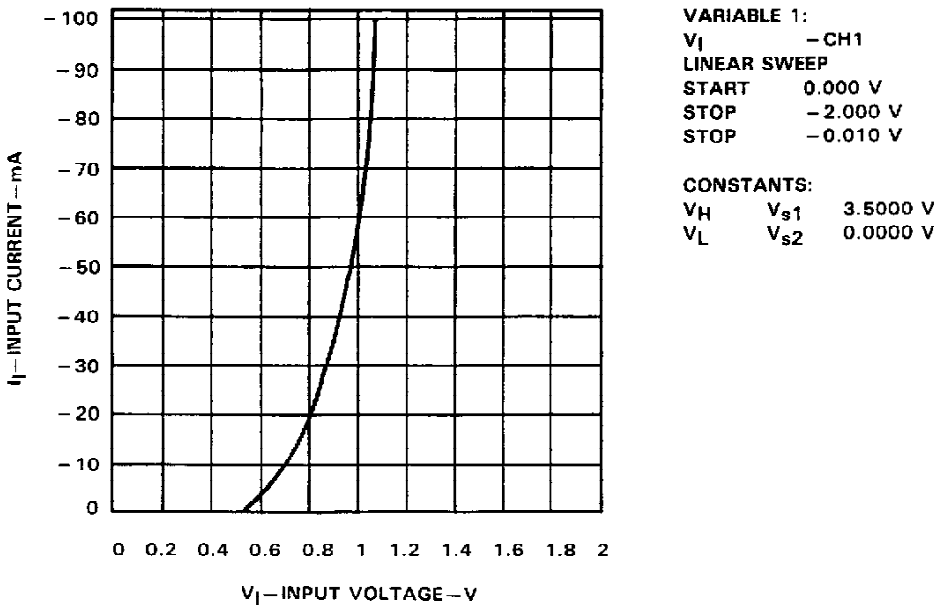


FIGURE 3. TYPICAL CURRENT-VOLTAGE CURVE

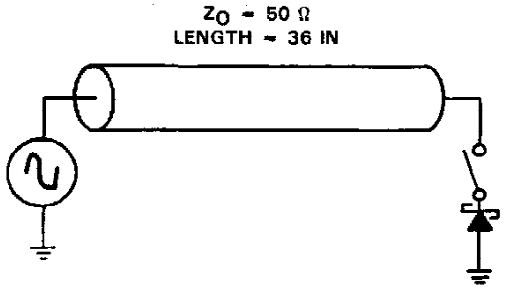


FIGURE 4. DIODE TEST SETUP

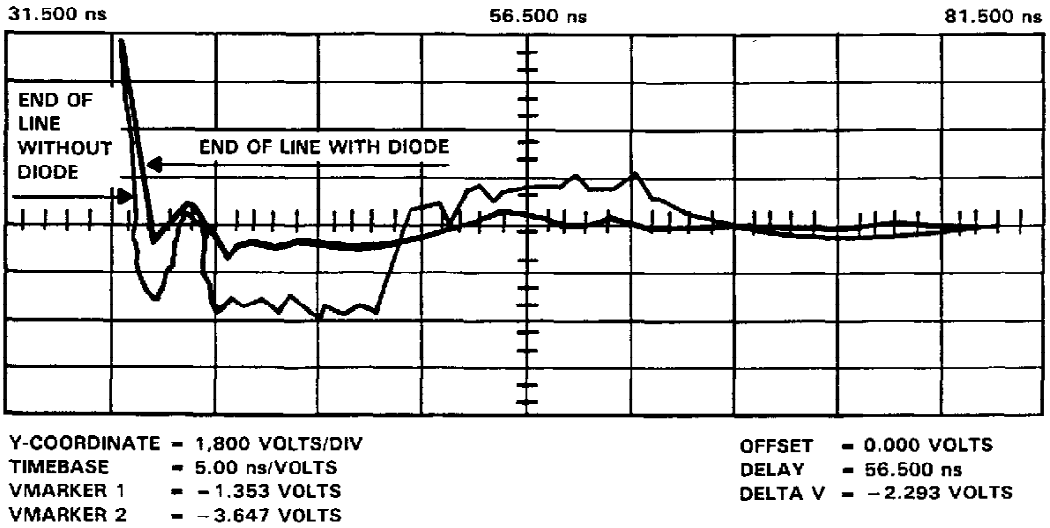


FIGURE 5. SCOPE DISPLAY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S1052DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S1052	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

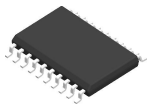
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

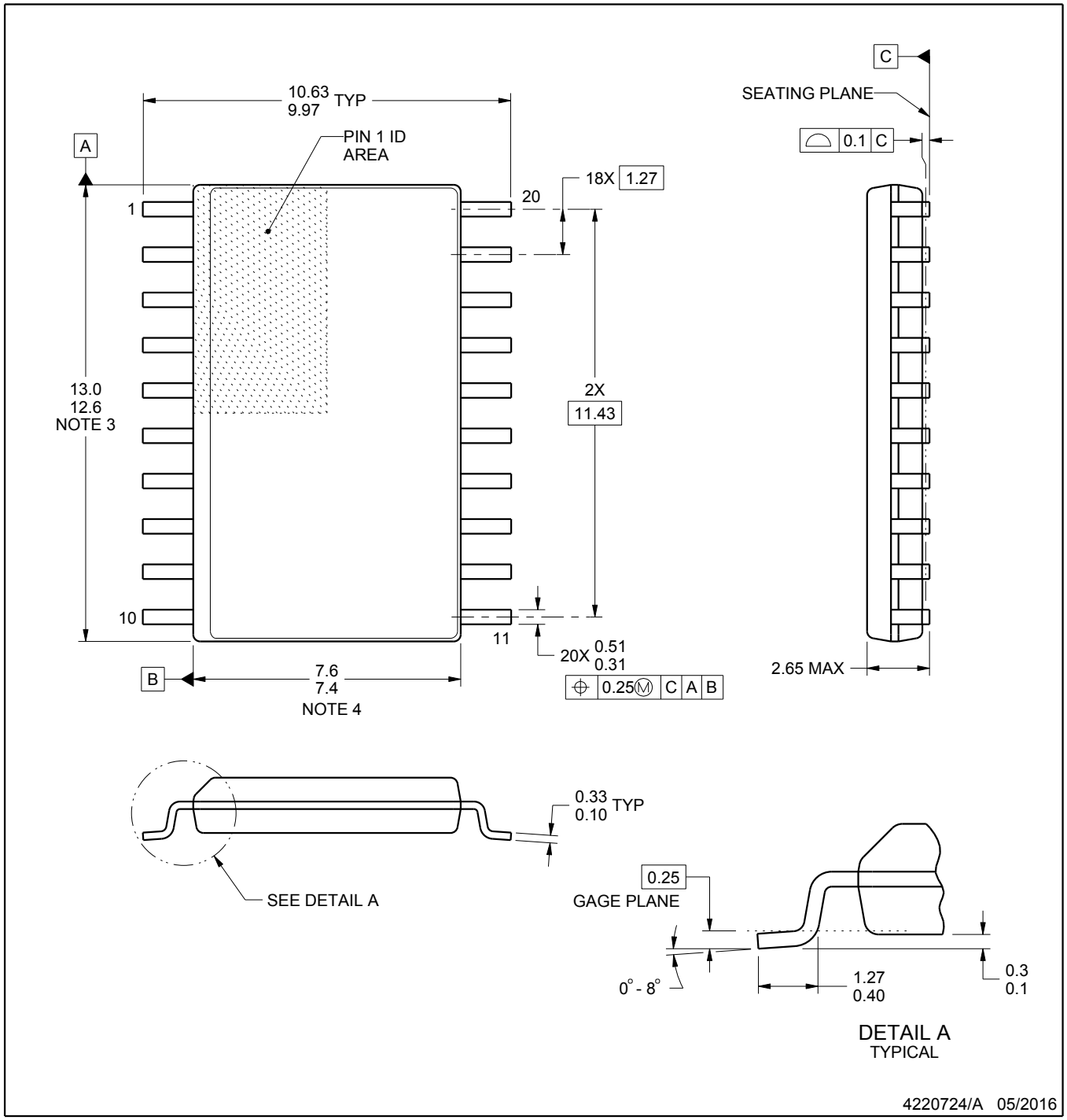


PACKAGE OUTLINE

DW0020A

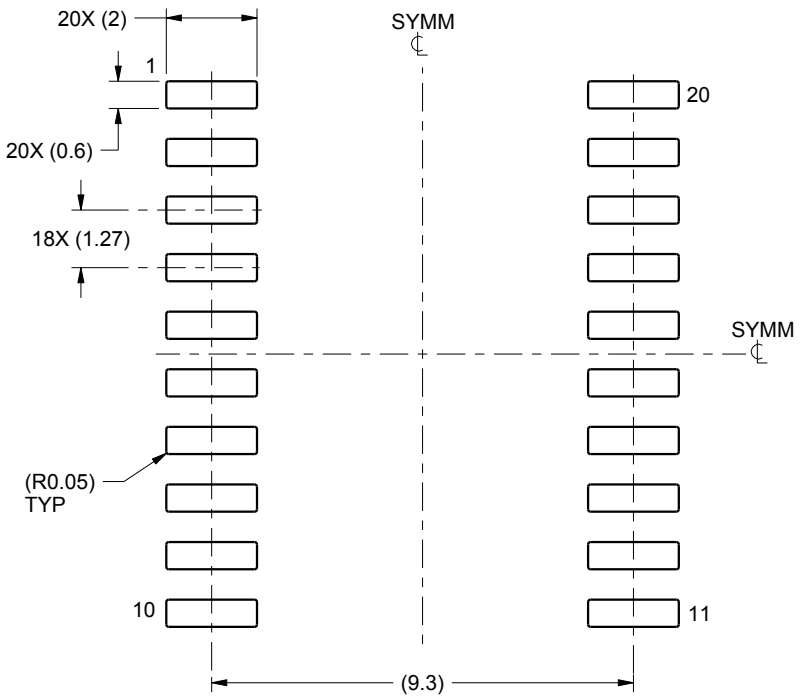
SOIC - 2.65 mm max height

SOIC

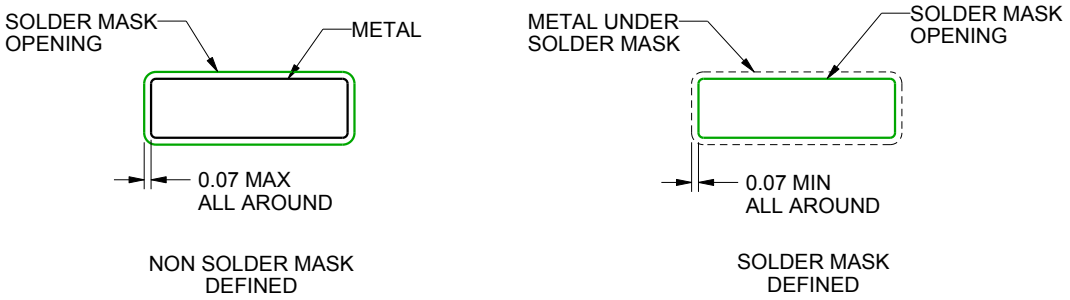


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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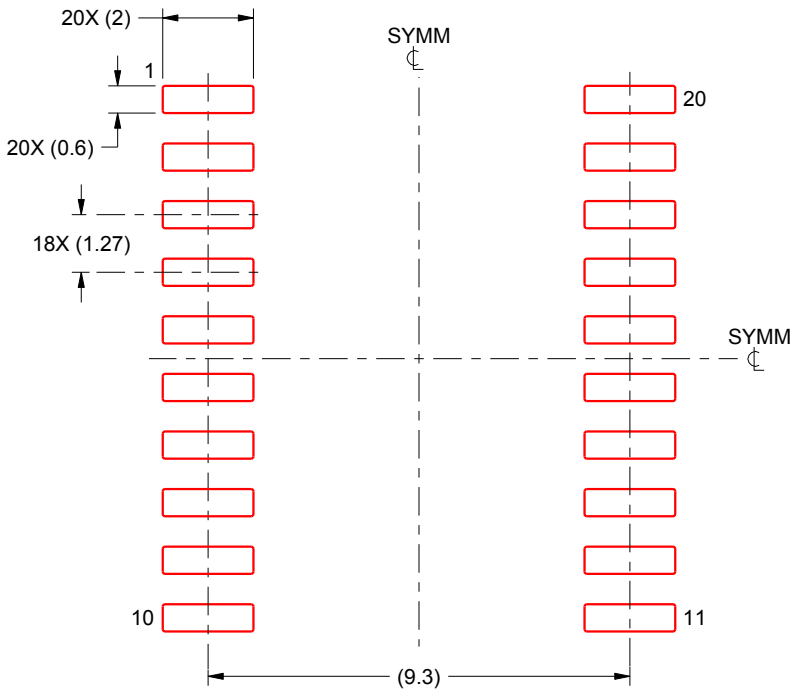
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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