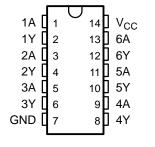
SN74LVCU04A

#### **FEATURES**

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 3.8 ns
- Typical V<sub>OLP</sub> (Output Ground Bounce)
  <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
  >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Inputs Accept Voltages to 5.5 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



#### **DESCRIPTION/ORDERING INFORMATION**

This hex inverter is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCU04A contains six independent inverters with unbuffered outputs and performs the Boolean function  $Y = \overline{A}$ .

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

#### ORDERING INFORMATION

T <sub>A</sub>	PACK	AGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	Tube of 50		SN74LVCU04AD	İ	
	SOIC - D	Reel of 2500	SN74LVCU04ADR	LVCU04A	
		Reel of 250	SN74LVCU04ADT		
	SOP - NS	Reel of 2000	SN74LVCU04ANSR	LVCU04A	
–40°C to 85°C	SSOP – DB	Reel of 2000	SN74LVCU04ADBR	LCU04A	
		Tube of 90	SN74LVCU04APW		
	TSSOP – PW	Reel of 2000	SN74LVCU04APWR	LCU04A	
		Reel of 250	SN74LVCU04APWT		
	TVSOP – DGV	Reel of 2000	SN74LVCU04ADGVR	LCU04A	

<sup>(1)</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
Н	L
L	Н



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



## LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



## **Absolute Maximum Ratings**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range <sup>(2)</sup>		-0.5	6.5	V
Vo	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current		±50	mA	
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		D package		86	
		DB package		96	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGV package		127	°C/W
		NS package		76	
		PW package		113	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>3)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



# Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT	
V	Supply voltage	Operating	1.65	3.6	V	
V <sub>CC</sub>	Supply voltage	Data retention only	1.5		V	
		V <sub>CC</sub> = 1.65 V	1.32			
		$V_{CC} = 2.3 \text{ V}$	1.84			
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7 \text{ V}$	2.16		V	
		V <sub>CC</sub> = 3 V	2.4			
		V <sub>CC</sub> = 3.6 V	2.88			
		V <sub>CC</sub> = 1.65 V		0.4		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3 \text{ V}$		0.5	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.65		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	$V_{CC}$	V	
		V <sub>CC</sub> = 1.65 V		-4		
	High level output ourrent	$V_{CC} = 2.3 \text{ V}$		-8	mA	
I <sub>OH</sub>	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12 m/		
		$V_{CC} = 3 V$		-24		
		V <sub>CC</sub> = 1.65 V		4		
	Low level output ourrent	$V_{CC} = 2.3 \text{ V}$	V <sub>CC</sub> = 2.3 V			
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA	
		V <sub>CC</sub> = 3 V		24		
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST (	CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
	$I_{OH} = -100 \mu A,$	V <sub>IL</sub> = 0 V	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			
	$I_{OH} = -4 \text{ mA},$	$V_{IL} = 0 V$	1.65 V	1.2			
$V_{OH}$	$I_{OH} = -8 \text{ mA},$	V <sub>IL</sub> =0 V	2.3 V	1.7			V
VOH	l – 12 mΛ	$V_{II} = 0 V$	2.7 V	2.2			V
	$I_{OH} = -12 \text{ mA},$	VIL = U V	3 V	2.4			
	$I_{OH} = -24 \text{ mA},$	$V_{IL} = 0 V$	3 V	2.2			
	$I_{OL} = 100 \mu A$ ,	$V_{IH} = V_{CC}$	1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA},$	$V_{IH} = V_{CC}$	1.65 V			0.45	
$V_{OL}$	$I_{OL} = 8 \text{ mA},$	$V_{IH} = V_{CC}$	2.3 V			0.7	V
	$I_{OL} = 12 \text{ mA},$	$V_{IH} = V_{CC}$	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA},$	$V_{IH} = V_{CC}$	3 V			0.55	
l <sub>l</sub>	$V_I = 5.5 \text{ V or GND}$		3.6 V			±5	μΑ
I <sub>CC</sub>	$V_I = V_{CC}$ or GND,	I <sub>O</sub> = 0	3.6 V			10	μΑ
$\Delta I_{CC}$	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V	·		500	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND		3.3 V		5		pF

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

# SN74LVCU04A HEX INVERTER



## **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER FROM (INPUT) (OL			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
	(INPOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Y	1	7.3	1	6.7	1	4.7	1	3.8	ns
t <sub>sk(o)</sub>										1	ns

# **Operating Characteristics**

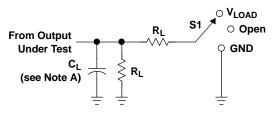
T<sub>A</sub> = 25°C

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per inverter	f = 10 MHz	3	4	5	pF

SN74LVCU04A



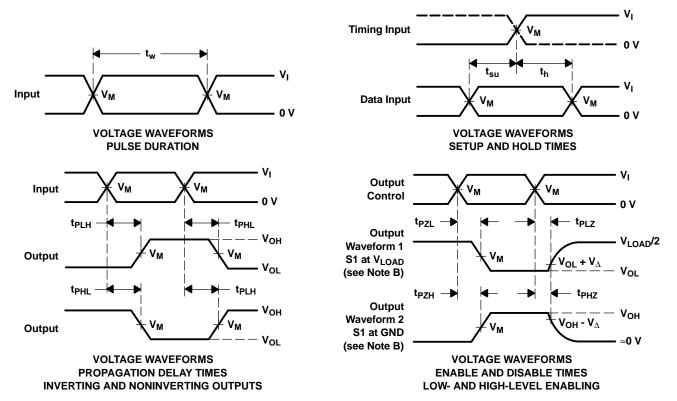
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

**LOAD CIRCUIT** 

.,	INF	PUTS	.,	.,		_	.,	
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	R <sub>L</sub>	$V_{\!\scriptscriptstyle \Delta}$	
1.8 V $\pm$ 0.15 V	v <sub>cc</sub>	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V	
2.5 V $\pm$ 0.2 V	V <sub>CC</sub>	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V	
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
3.3 V $\pm$ 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50~\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
SN74LVCU04AD	ACTIVE	SOIC	Drawing	14	50	(2) Green (RoHS & no Sb/Br)	CU NIPDAU	(3) Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74LVCU04ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04ADTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCU04A	Samples
SN74LVCU04APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples



## PACKAGE OPTION ADDENDUM

26-Aug-2013

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
SN74LVCU04APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74LVCU04APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCU04A	Samples
SN74LVCU04APWTE4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LCU04A	Samples
SN74LVCU04APWTG4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LCU04A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



## **PACKAGE OPTION ADDENDUM**

26-Aug-2013

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**PACKAGE MATERIALS INFORMATION** 

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## TAPE AND REEL INFORMATION





_	_	
		3
	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCU04ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVCU04ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVCU04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCU04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCU04ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCU04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCU04ADBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LVCU04ADGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74LVCU04ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVCU04ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LVCU04ADT	SOIC	D	14	250	367.0	367.0	38.0
SN74LVCU04APWR	TSSOP	PW	14	2000	367.0	367.0	35.0

## DGV (R-PDSO-G\*\*)

#### **24 PINS SHOWN**

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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