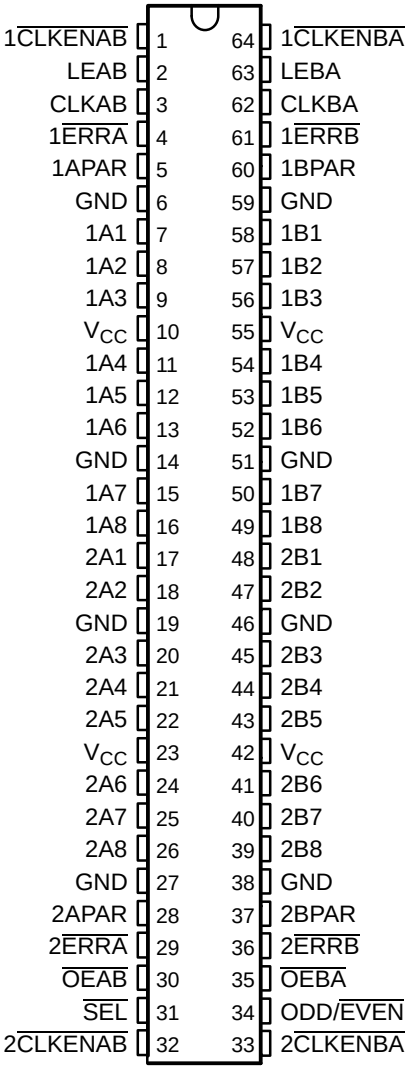
FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.4 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Simultaneously Generates and Checks Parity**
- **Option to Select Generate Parity and Check or Feedthrough Data/Parity in A-to-B or B-to-A Direction**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class I**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**

DGG PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 18-bit (dual-octal) noninverting registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver, or it can generate/check parity from the two 8-bit data buses in either direction.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74LVCH16901DGGR	LVCH16901

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74LVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) inputs. It also provides parity-enable ($\overline{\text{SEL}}$) and parity-select (ODD/$\overline{\text{EVEN}}$) inputs and separate error-signal ($\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$) outputs for checking parity. The direction of data flow is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) inputs. When $\overline{\text{SEL}}$ is low, the parity functions are enabled. When $\overline{\text{SEL}}$ is high, the parity functions are disabled, and the device acts as an 18-bit registered transceiver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLES

FUNCTION(1)

INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0(2)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0(2)
L	L	L	H	X	B_0(3)

(1) A-to-B data flow is shown: B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKENBA}}$.
(2) Output level before the indicated steady-state input conditions were established
(3) Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY ENABLE

INPUTS			OPERATION OR FUNCTION	
$\overline{\text{SEL}}$	$\overline{\text{OEBA}}$	$\overline{\text{OEAB}}$		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are disabled; device acts as a standard 18-bit registered transceiver.	Q_A data to B, Q_B data to A
H	L	H		Q_B data to A
H	H	L		Q_A data to B
H	H	H		Isolation

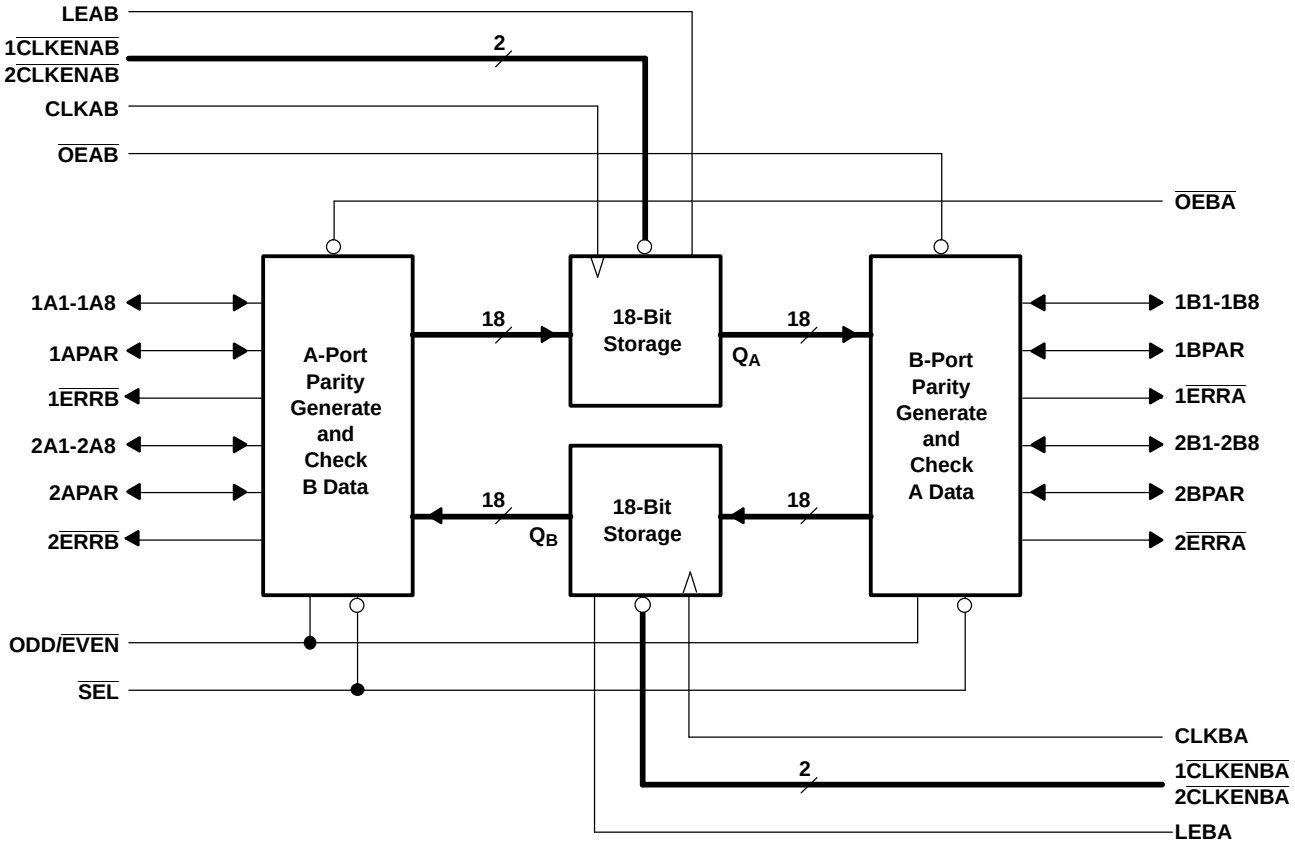
FUNCTION TABLES (CONTINUED)

PARITY

INPUTS								OUTPUTS			
$\overline{SEL}$	$\overline{OEBA}$	$\overline{OEAB}$	ODD/$\overline{EVEN}$	Σ OF INPUTS A1–A8 = H	Σ OF INPUTS B1–B8 = H	APAR	BPAR	APAR	$\overline{ERRA}$	BPAR	$\overline{ERRB}$
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	L	Z	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE(1)	Z	PE(1)	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO(2)	Z	PO(2)	Z

(1) Parity output is set to the level so that the specific bus side is set to even parity.
(2) Parity output is set to the level so that the specific bus side is set to odd parity.

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]			55	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		1.65 V to 3.6 V	V_{CC} – 0.2			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.7			
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2.2			
V_{OL}		I_{OL} = 100 µA		1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.7	
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Control inputs	V_I = 0 to 5.5 V		3.6 V			±5	µA
$I_{I(hold)}$	A or B ports	V_I = 0.58 V		1.65 V	25			µA
		V_I = 1.07 V			–25			
		V_I = 0.7 V		2.3 V	45			
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V(2)		3.6 V			±600	
I_{off}		V_I or V_O = 5.5 V		0			±10	µA
I_{OZ}(3)		V_O = 0 to 5.5 V		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			20	µA
		3.6 V ≤ V_I ≤ 5.5 V(4)					20	
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		7		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		9.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current, but not $I_{I(hold)}$.
(4) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 1.8 V(1)		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			125		125		125		125	MHz
t_w	Pulse duration	CLK↑	4		3		3		3		ns
		LE high	3		3		3		3		
t_{su}	Setup time	A, APAR or B, BPAR before CLK↑	4.7		2.7		2.8		2.5		ns
		$\overline{CLKEN}$ before CLK↑	4.5		2.9		2.9		2.5		
		A, APAR or B, BPAR before LE↓	0		2.2		2.1		2		
t_h	Hold time	A, APAR or B, BPAR after CLK↑	0		1.2		1.2		1.3		ns
		$\overline{CLKEN}$ after CLK↑	0		1.3		1.3		1.5		
		A, APAR or B, BPAR after LE↓	1		1.7		1.9		1.7		

(1) Texas Instruments SPICE simulation data

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V(1)		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			125		125		125		125		MHz
t_{pd}	A or B	B or A		5.9	1	6.2		5.8	1	5.4	ns
		BPAR or APAR		12.7	2	9.9		8.6	2	7.7	
	APAR or BPAR	BPAR or APAR		7	1	6.7		6.2	1	5.7	
		$\overline{ERRA}$ or $\overline{ERRB}$		13	2	10.7		9.7	2	8.5	
	ODD/$\overline{EVEN}$	$\overline{ERRA}$ or $\overline{ERRB}$		9.9	1.5	9.7		8.9	1.5	7.8	
		BPAR or APAR		10.4	1.5	9.3		8.6	1.5	7.5	
	$\overline{SEL}$	BPAR or APAR		6.9	1	7.1		6.9	1	6.1	
	CLKAB or CLKBA	A or B		6.9	1	7.4		6.8	1	6.1	
		BPAR or APAR parity feedthrough		8.5	1.5	8.1		7.3	1.5	6.6	
		BPAR or APAR parity generated		14.1	2.5	11.2		9.7	2	8.7	
		$\overline{ERRA}$ or $\overline{ERRB}$		14.3	2.5	11.5		9.9	2	8.9	
	LEAB or LEBA	A or B		6.8	1	7		6.5	1	5.8	
		BPAR or APAR parity feedthrough		7.9	1.5	7.7		7	1.5	6.3	
		BPAR or APAR parity generated		13.6	2.5	10.8		9.3	2	8.4	
		$\overline{ERRA}$ or $\overline{ERRB}$		13.5	2.5	10.9		9.5	2	8.5	
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR		6.8	1.4	7.3		7.1	1	6.3	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR		6.9	1.3	7.1		6.2	1.5	5.9	ns
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$		7.4	1.4	7.2		6.5	1	5.9	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$		9.3	1.3	8.3		7.5	1	6.7	ns
t_{en}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$		7.6	1.4	7.7		7.5	1	6.5	ns
t_{dis}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$		7.8	1.3	7.4		6.4	1.5	5.9	ns

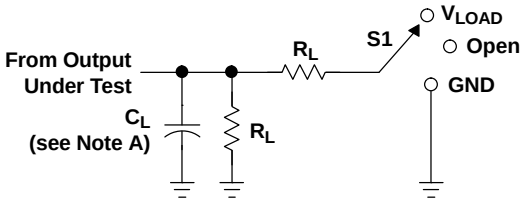
(1) Texas Instruments SPICE simulation data

Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	37	52	68	pF
		Outputs disabled		16	22	28	

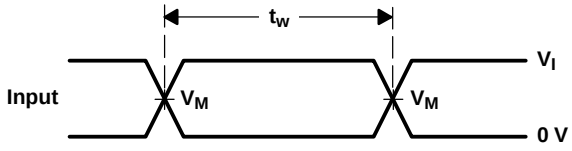
PARAMETER MEASUREMENT INFORMATION



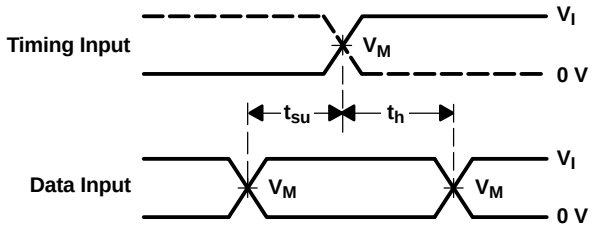
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

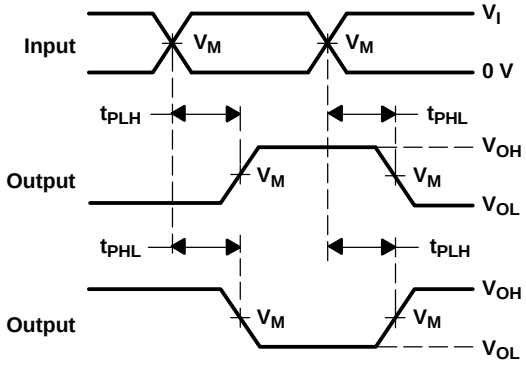
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



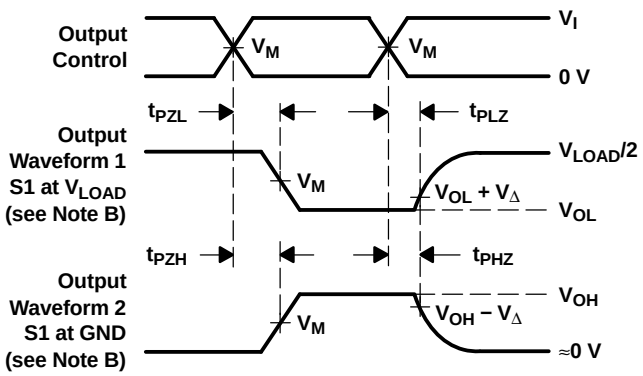
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVCH16901DGGRE4	NRND	TSSOP	DGG	64		TBD	Call TI	Call TI	-40 to 85		
74LVCH16901DGGRG4	NRND	TSSOP	DGG	64		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

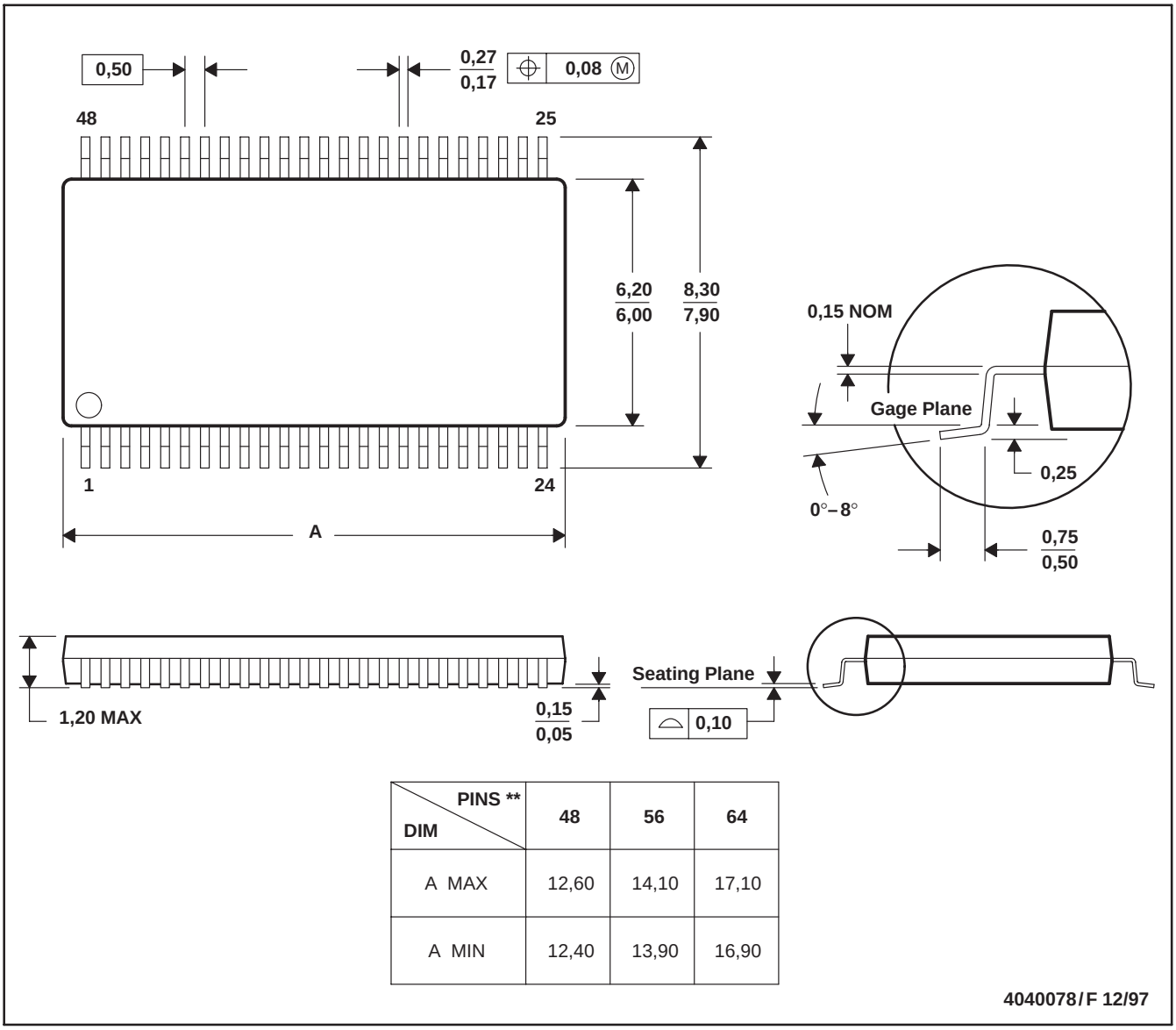
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153