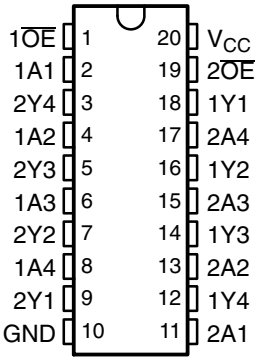
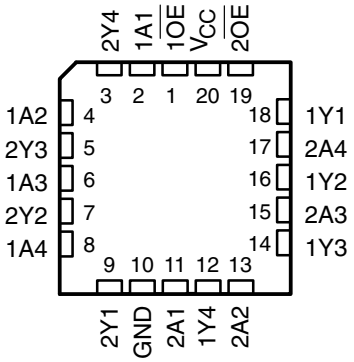
- **Operating Voltage Range of 4.5 V to 5.5 V**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

SN54BCT2240 . . . J OR W PACKAGE
SN74BCT2240 . . . DB, DW, N,OR NS PACKAGE
(TOP VIEW)



SN54BCT2240 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN74BCT2241 and the 'BCT2244 devices, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

The 'BCT2240 devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The outputs, which are designed to source or sink up to 12 mA, include 33-Ω series resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT2240N	SN74BCT2240N
	SOIC – DW	Tube	SN74BCT2240DW	BCT2240
		Tape and reel	SN74BCT2240DWR	
	SOP – NS	Tape and reel	SN74BCT2240NSR	BCT2240
	SSOP – DB	Tape and reel	SN74BCT2240DBR	BA240
–55°C to 125°C	CDIP – J	Tube	SNJ54BCT2240J	SNJ54BCT2240J
	CFP – W	Tube	SNJ54BCT2240W	SNJ54BCT2240W
	LCCC – FK	Tube	SNJ54BCT2240FK	SNJ54BCT2240FK

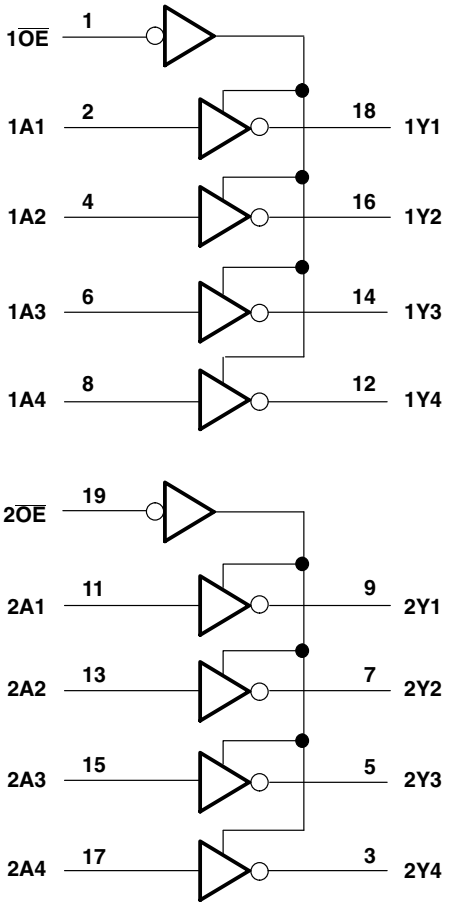
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

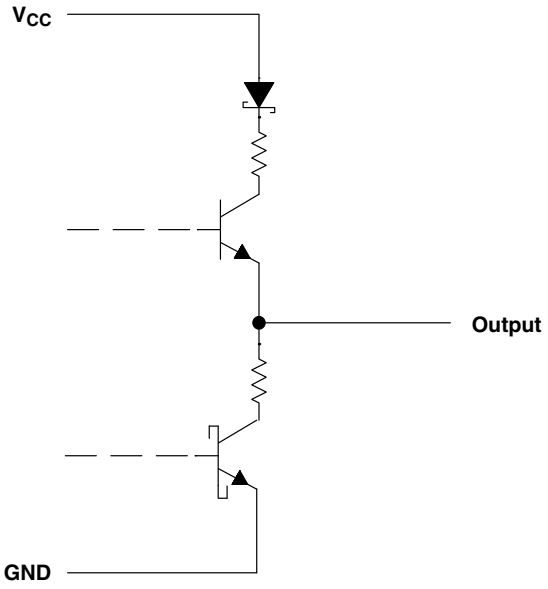
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic diagram (positive logic)



schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} . . . . . –30 mA
Current into any output in the low state . . . . . 24 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54BCT2240			SN74BCT2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–12			–12	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

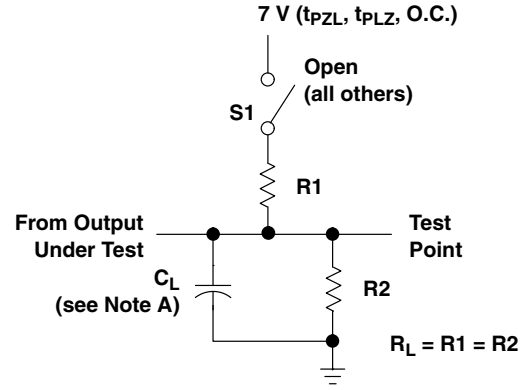
PARAMETER	TEST CONDITIONS		SN54BCT2240			SN74BCT2240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = –12 mA	2	3.2		2	3.2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			–1			–1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–50			–50	µA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	–100		–225	–100		–225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		19	32		19	32	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		46	76		46	76	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		6	8		6	8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
† Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

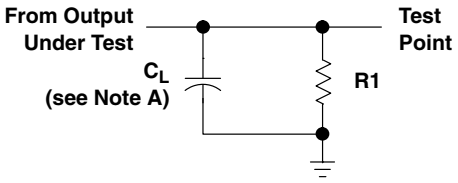
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L =50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT2240		SN74BCT2240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	3.4	4.8	0.5	6.3	0.5	5.7	ns
t_{PHL}			0.5	2.8	4	0.5	4.6	0.5	4.4	
t_{PZH}	$\overline{OE}$	Y	2.6	6.2	8.2	2.6	10.1	2.6	9.3	ns
t_{PZL}			4.3	8.8	10.9	4.3	12.9	4.3	12.4	
t_{PHZ}	$\overline{OE}$	Y	2	5.3	7.1	2	9.2	2	8.7	ns
t_{PLZ}			2.2	6.7	8.5	2.2	12.2	2.2	10.6	

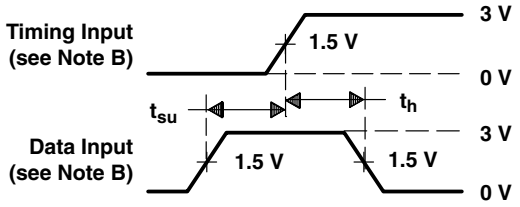
PARAMETER MEASUREMENT INFORMATION



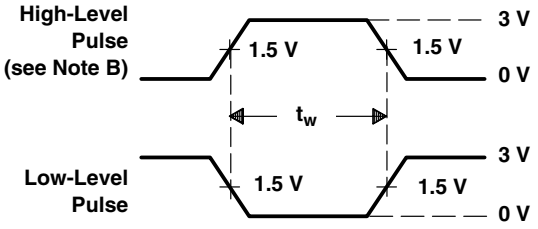
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



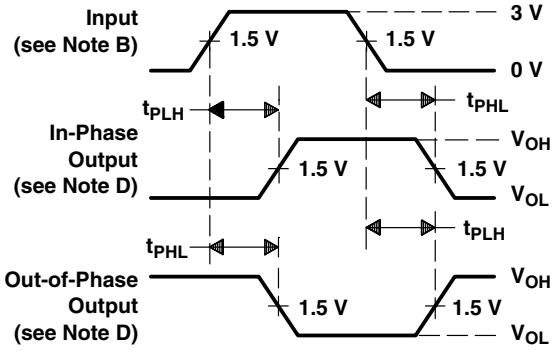
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



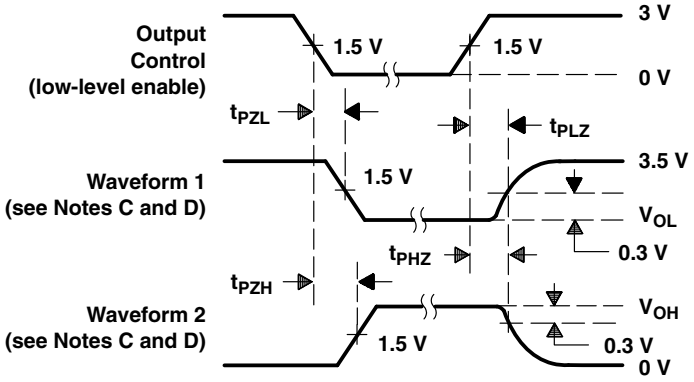
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9093901M2A	ACTIVE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125	5962-9093901M2A SNJ54BCT2240FK	Samples
5962-9093901MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9093901MRA SNJ54BCT2240J	Samples
5962-9093901MSA	ACTIVE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125	5962-9093901MSA SNJ54BCT2240W	Samples
SN74BCT2240DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		
SNJ54BCT2240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9093901M2A SNJ54BCT2240FK	Samples
SNJ54BCT2240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9093901MRA SNJ54BCT2240J	Samples
SNJ54BCT2240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9093901MSA SNJ54BCT2240W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54BCT2240, SN74BCT2240 :

- Catalog: SN74BCT2240
- Military: SN54BCT2240

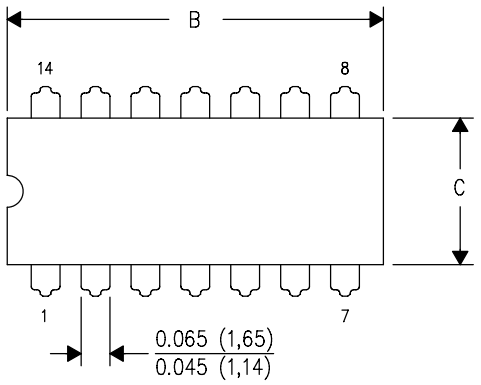
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

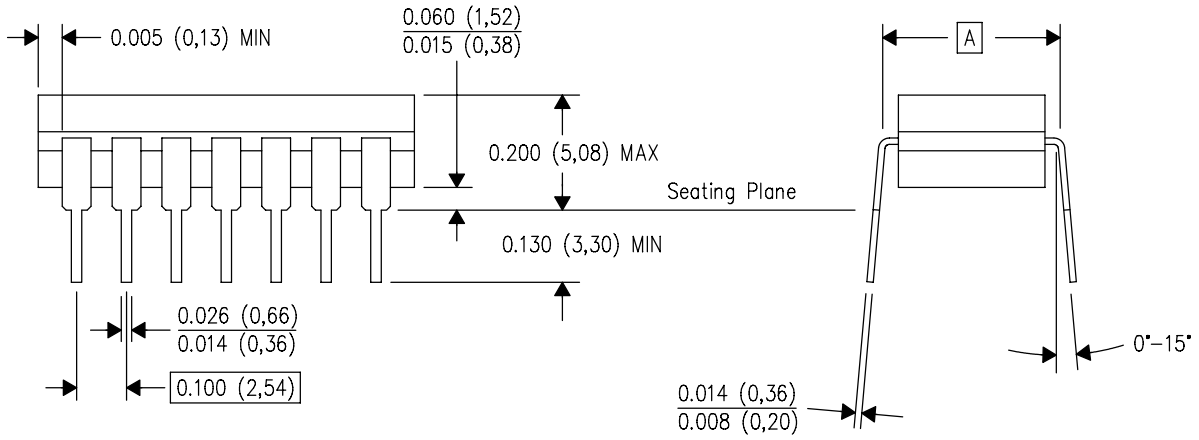
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



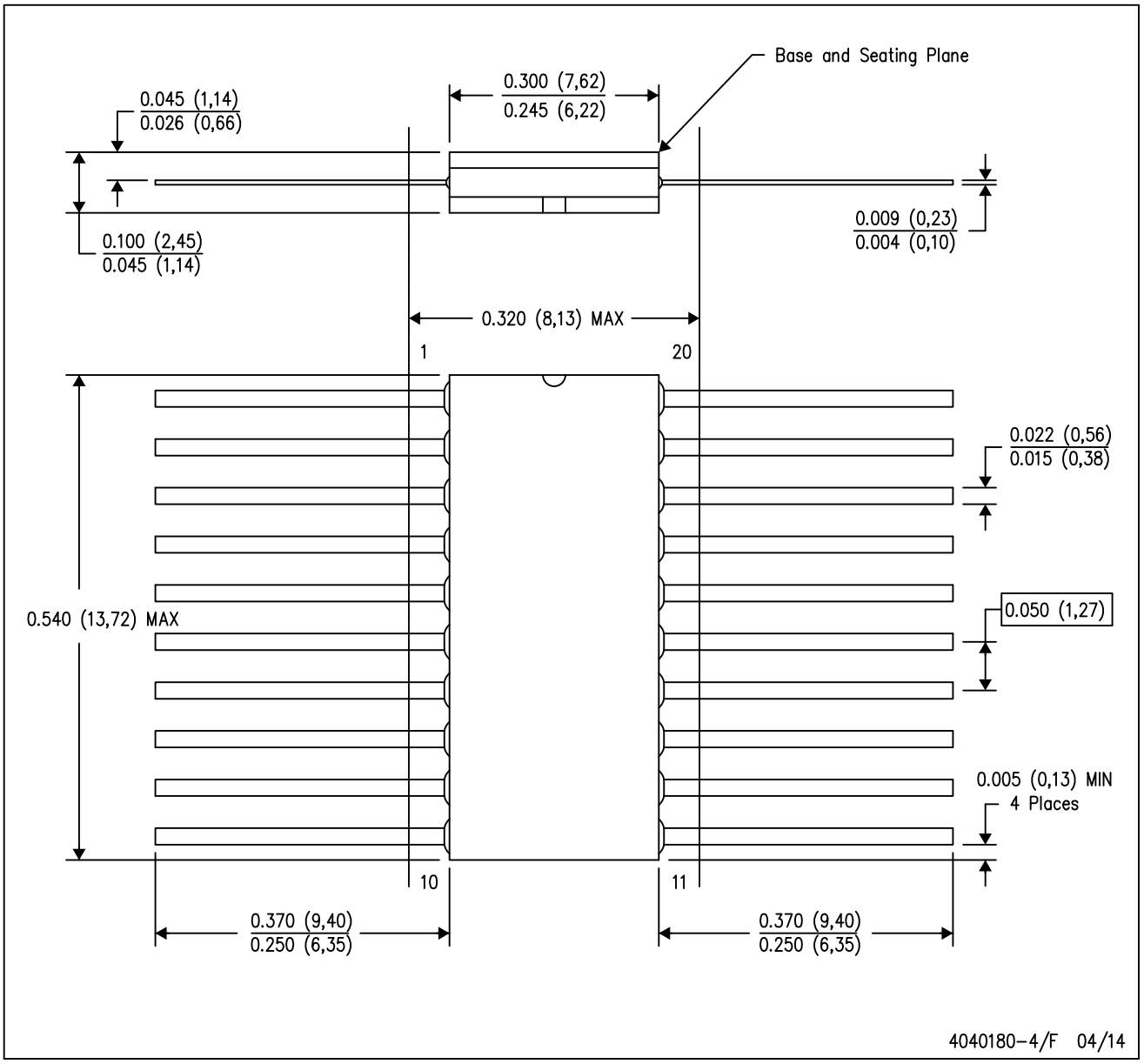
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

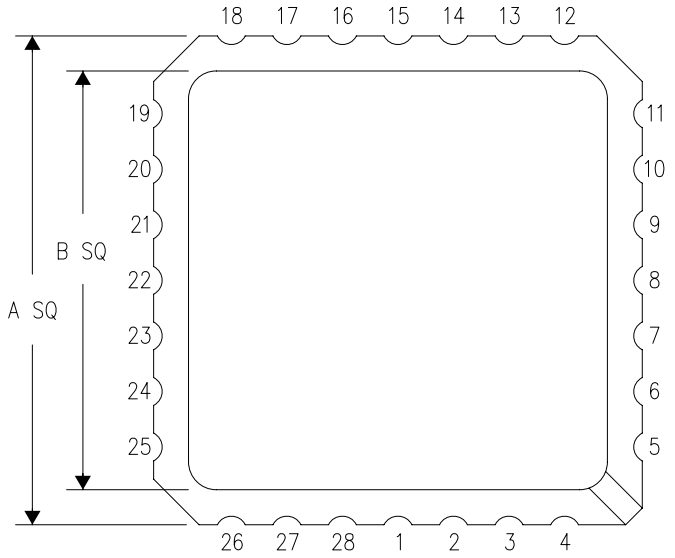
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



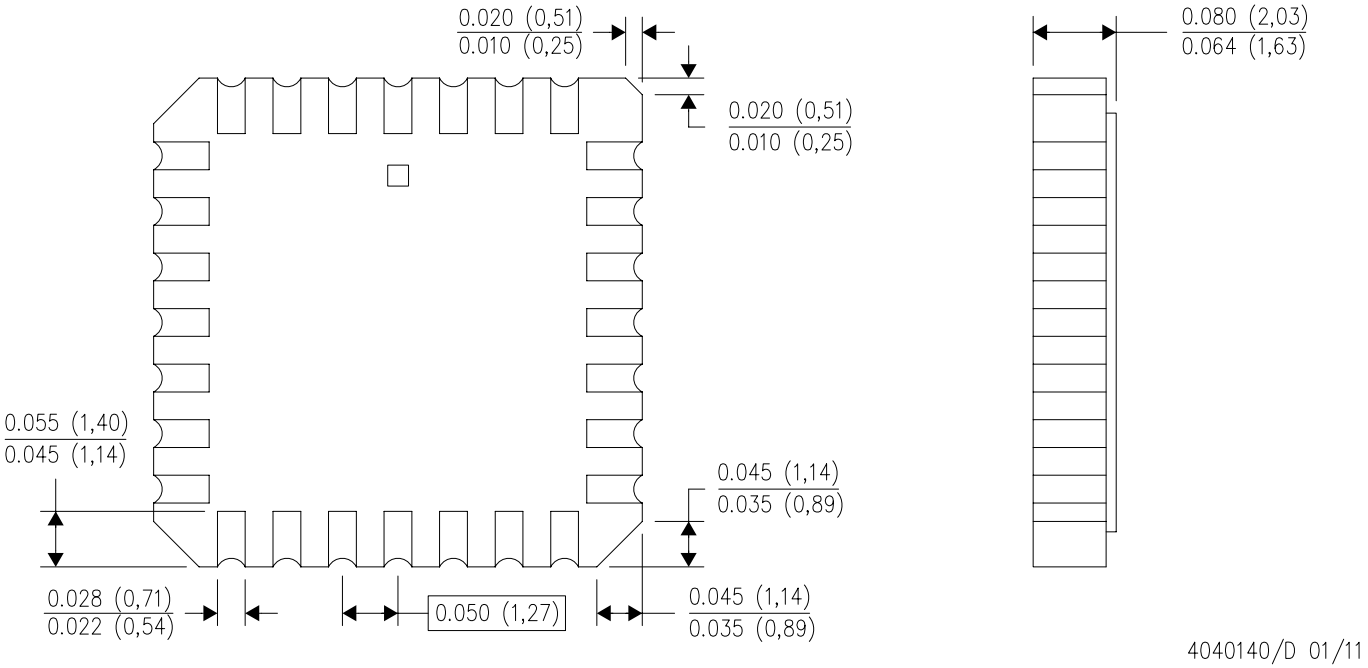
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



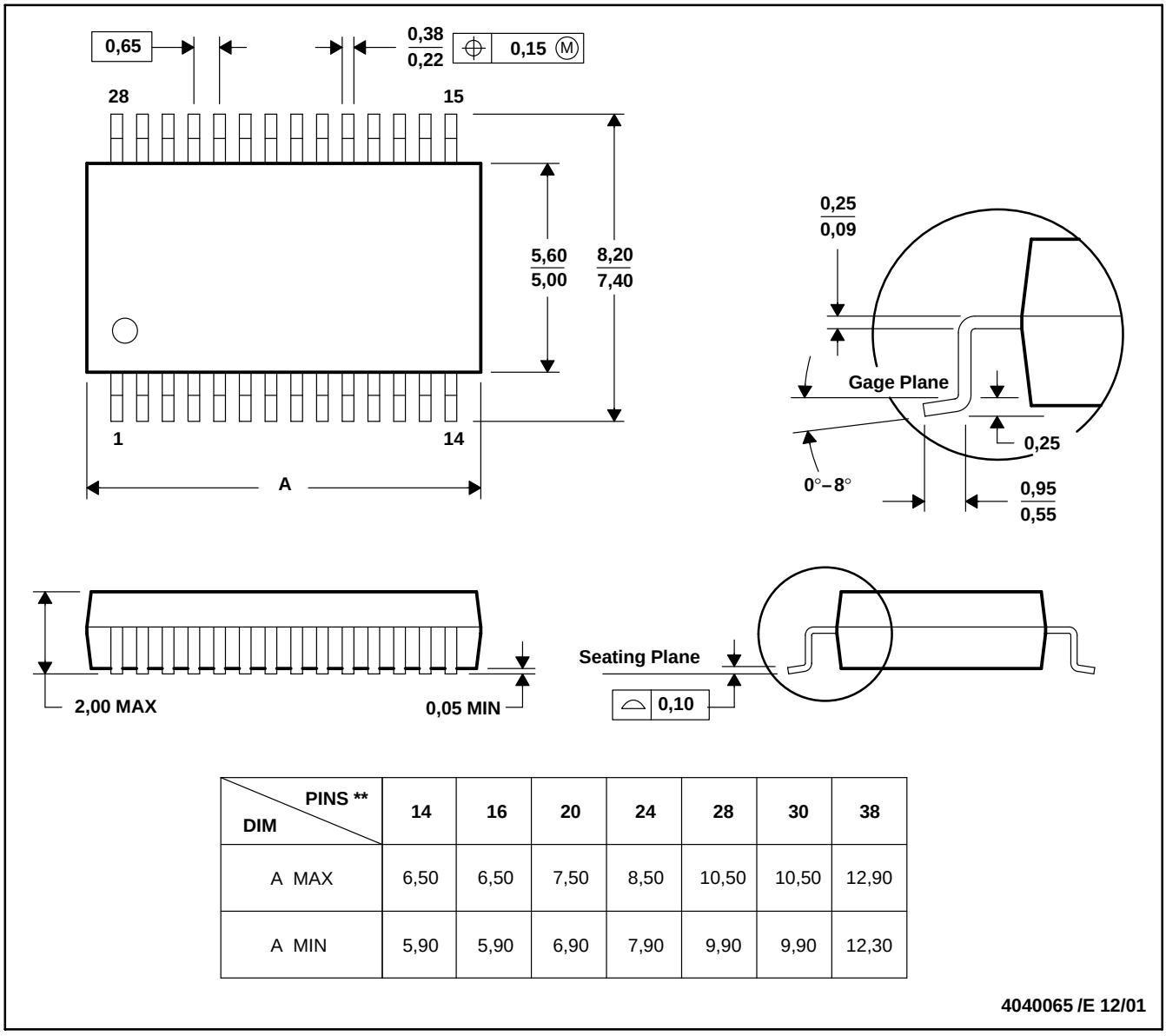
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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