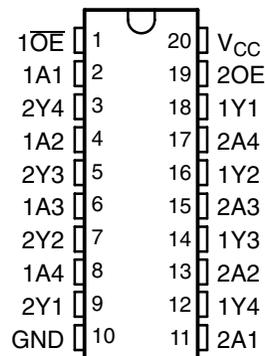


# SN74BCT2241 OCTAL BUFFER AND LINE/MOS DRIVER WITH 3-STATE OUTPUTS

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- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- Output Ports Have Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

DW, N OR NS PACKAGE  
(TOP VIEW)



## description/ordering information

This SN74BCT2241 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'BCT2240 and 'BCT2244 devices, this device provides the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs. This device features high fan-out and improved fan-in.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The outputs, which are designed to source or sink up to 12 mA, include 33- $\Omega$  series resistors to reduce overshoot and undershoot.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT2241N	SN74BCT2241N
	SOIC – DW	Tube	SN74BCT2241DW	BCT2241
		Tape and reel	SN74BCT2241DWR	
	SOP – NS	Tape and reel	SN74BCT2241NSR	BCT2241

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLES

INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

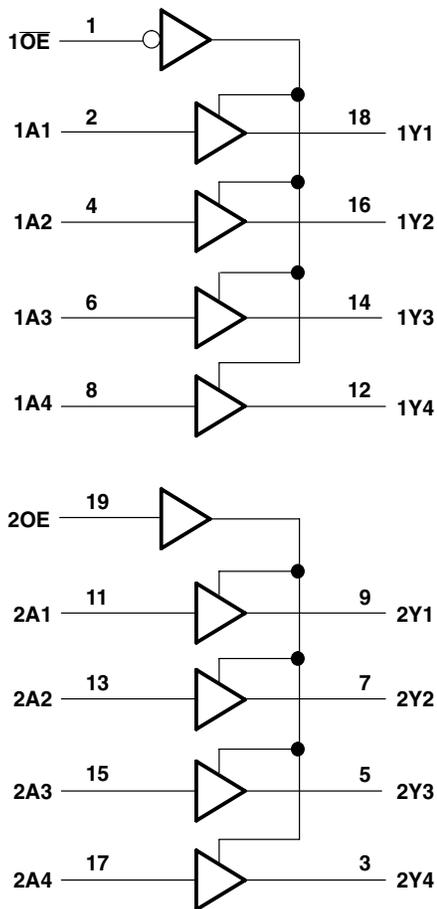
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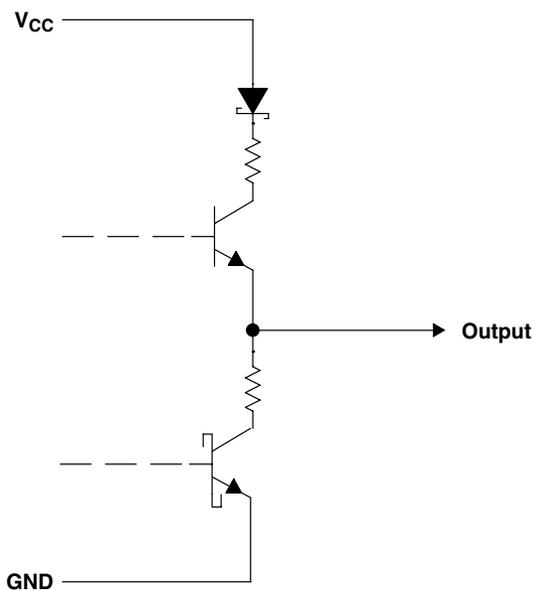
# SN74BCT2241 OCTAL BUFFER AND LINE/MOS DRIVER WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## schematic of Y outputs



# SN74BCT2241 OCTAL BUFFER AND LINE/MOS DRIVER WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ .....	–30 mA
Current into any output in the low state, $I_O$ .....	24 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			–18	mA
$I_{OH}$	High-level output current			–12	mA
$I_{OL}$	Low-level output current			12	mA
$T_A$	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN74BCT2241**  
**OCTAL BUFFER AND LINE/MOS DRIVER**  
**WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3		V
		$I_{OH} = -12\text{ mA}$	2			
	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3\text{ mA}$	2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 1\text{ mA}$		0.15	0.5	V
		$I_{OL} = 12\text{ mA}$		0.42	0.8	
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-1	mA
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$			-50	$\mu\text{A}$
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-100		-225	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open		23	37	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open		48	76	mA
$I_{CCZ}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open		6	9	mA
$C_i$	$V_{CC} = 5\text{ V}$ ,	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$		6		pF
$C_o$	$V_{CC} = 5\text{ V}$ ,	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$		11		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

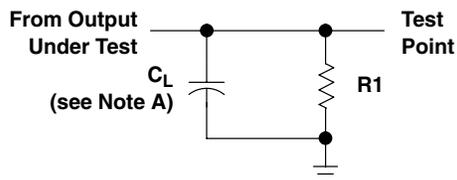
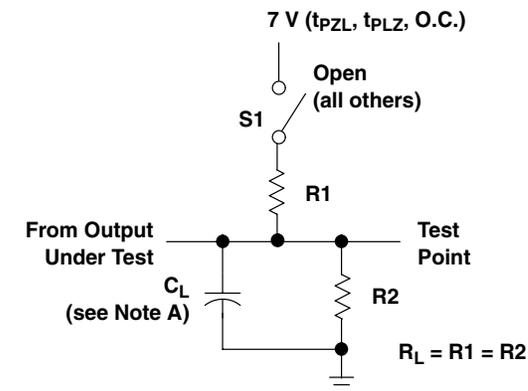
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1.1	3	4.4	1.1	4.9	ns
$t_{PHL}$			2.9	4.9	6.6	2.9	6.9	
$t_{PZH}$	OE or $\overline{OE}$	Y	2.7	6	7.8	2.7	8.9	ns
$t_{PZL}$			4.1	7.7	9.4	4.1	10.3	
$t_{PHZ}$	OE or $\overline{OE}$	Y	2.5	5.2	7.2	2.5	8.7	ns
$t_{PLZ}$			3.2	7.1	9.5	3.2	11.3	



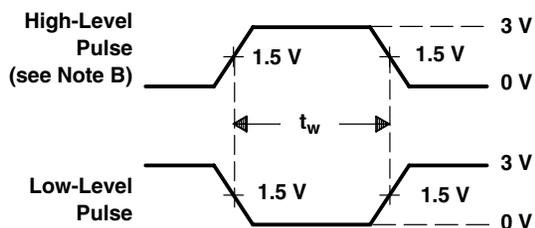
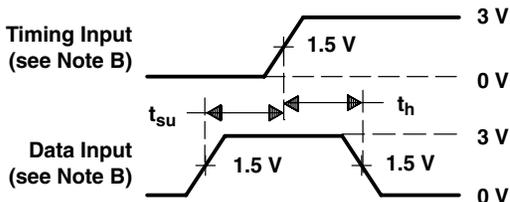
# SN74BCT2241 OCTAL BUFFER AND LINE/MOS DRIVER WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

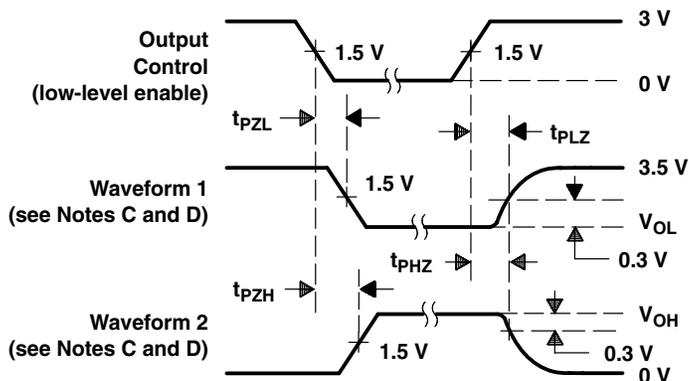
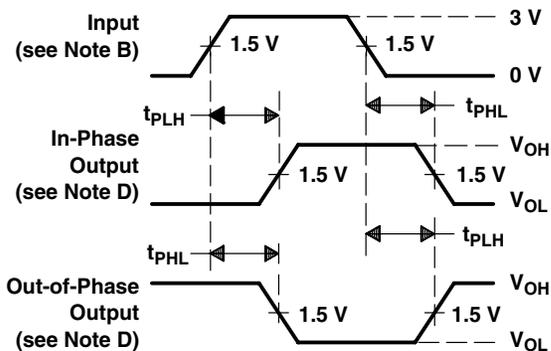


**LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
 F. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74BCT2241DW	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	BCT2241	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

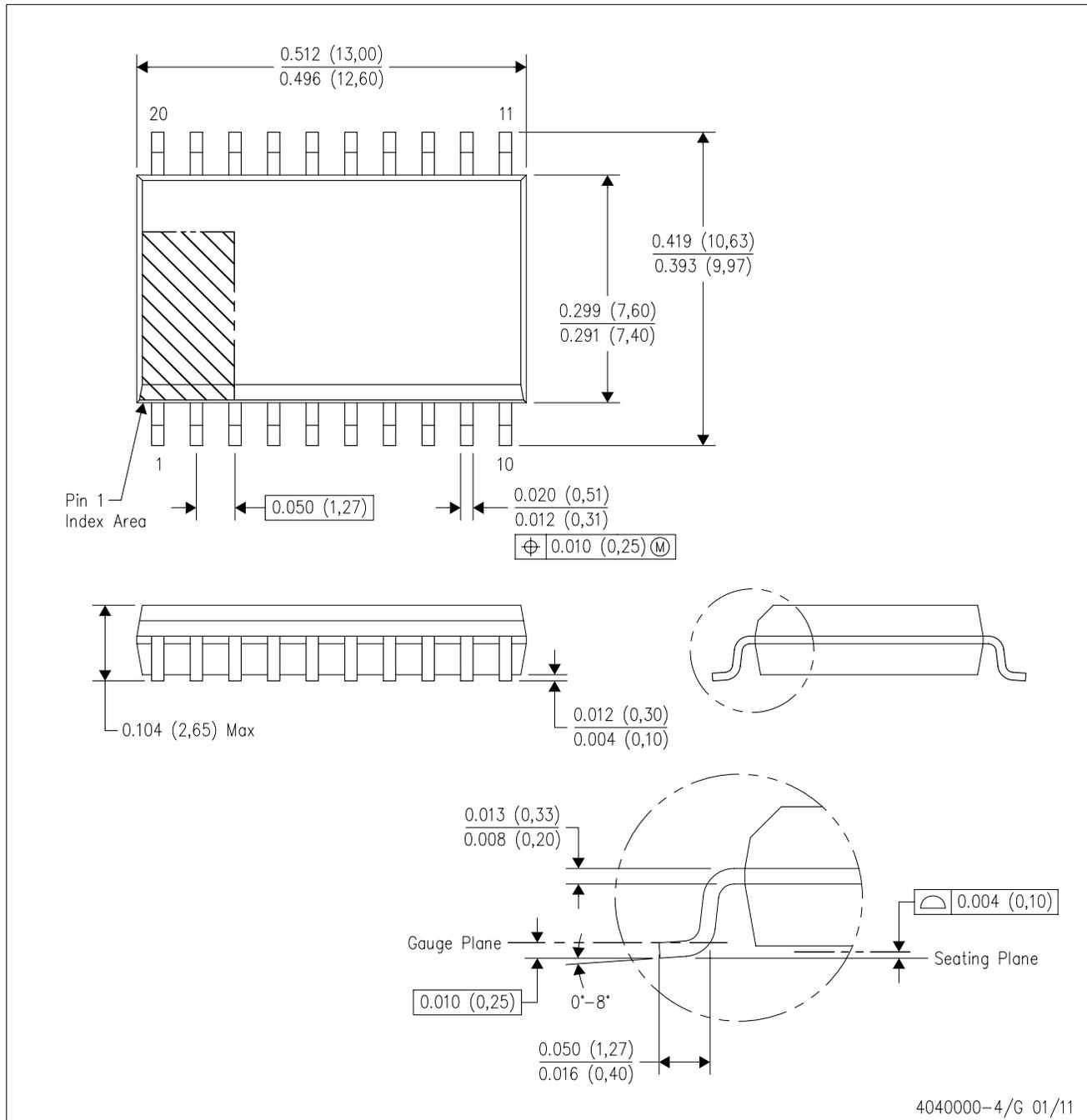
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DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

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