SCES094D-FEBRUARY 1997-REVISED OCTOBER 2004

## **FEATURES**

- Member of the Texas Instruments Widebus™
  Family
- EPIC<sup>™</sup> (Enhanced-Performance Implanted CMOS) Submicron Process
- A-Port Outputs Have Equivalent 50- $\Omega$  Series Resistors and B-Port Outputs Have Equivalent 20- $\Omega$  Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Thin Very Small-Outline Package

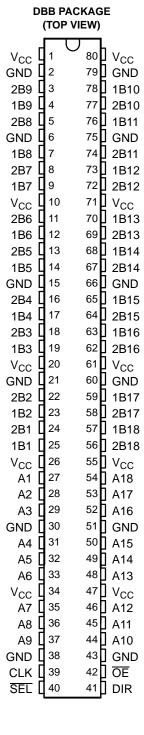
NOTE: For order entry, the DBB package is abbreviated to G. For tape and reel, the DBBR package is abbreviated to GR.

#### **DESCRIPTION**

The SN74ALVCHG162282 is an 18-bit to 36-bit registered bus exchanger. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V)  $V_{\rm CC}$  operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select (SEL) input selects 1B or 2B data for the A outputs.

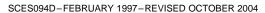
For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output-enable ( $\overline{OE}$ ) and direction-control (DIR) input. DIR is registered to synchronize the bus direction changes with the clock.





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# **DESCRIPTION (CONTINUED)**

The A-port N-channel output transistors are sized at 450  $\mu$ m, and the P-channel output transistors are sized at 700  $\mu$ m. All A-port outputs have equivalent 50- $\Omega$  series resistors. The B-port N-channel output transistors are sized at 225  $\mu$ m, and the P-channel output transistors are sized at 560  $\mu$ m. All B-port outputs have equivalent 20- $\Omega$  series resistors

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The switching characteristics are based on 25-pF (A port) and 80-pF (B port) loads, but are tested with the standard 50-pF load.

The SN74ALVCHG162282 is characterized for operation from 0°C to 70°C.

#### **FUNCTION TABLES**

#### A-TO-B STORAGE (OE = L, DIR = H)

	INPUTS	OUT	PUTS	
SEL	CLK	1B	2B	
Н	X	Χ	1B <sub>0</sub> <sup>(1)</sup>	2B <sub>0</sub> <sup>(1)</sup>
L	$\uparrow$	L	L <sup>(2)</sup>	L
L	$\uparrow$	Н	H <sup>(2)</sup>	Н

- Output level before indicated steady-state input conditions were established
- (2) Two CLK edges are needed to propagate the data.

#### B-TO-A STORAGE (OE = L, DIR = L)

	INP	UTS		OUTPUT
CLK	SEL	1B	2B	Α
1	Н	Х	L	L <sup>(1)</sup>
$\uparrow$	Н	Χ	Н	H <sup>(1)</sup>
$\uparrow$	L	L	Χ	L
$\uparrow$	L	Н	Χ	Н

(1) Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

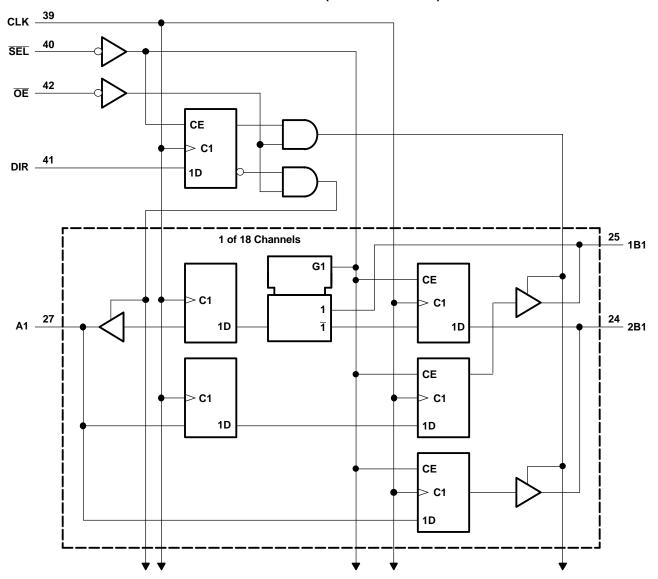
#### **OUTPUT ENABLE**

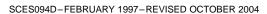
	INPUTS	OUTPUTS		
CLK	ŌĒ	DIR	Α	1B, 2B
1	Н	Х	Z	Z
1	L	Н	Z	Active
1	L	L	Active	Z



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# **LOGIC DIAGRAM (POSITIVE LOGIC)**







## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V
\/	Except I/O ports <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
V <sub>I</sub>	Input voltage range	I/O ports <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
Vo	Output voltage range <sup>(2)(3)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
$\theta_{JA}$	Package thermal impedance (4)			106	°C/W
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

# RECOMMENDED OPERATING CONDITIONS(1)

				MIN	MAX	UNIT
$V_{CC}$	Supply voltage		3	3.6	V	
$V_{IH}$	High-level input voltage $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$					V
$V_{IL}$	Low-level input voltage $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$				0.8	V
VI	Input voltage					V
Vo	Output voltage				V <sub>CC</sub>	V
	High level output ourrent	A to B	V <sub>CC</sub> = 3 V		8	mA
ІОН	High-level output current	B to A	V <sub>CC</sub> = 3 V		6	ША
	Low lovel output ourrent	A to B	V <sub>CC</sub> = 3 V		8	A
I <sub>OL</sub>	Low-level output current	B to A	V <sub>CC</sub> = 3 V		6	mA
Δt/Δν	Input transition rise or fall rate				10	ns/V
$T_A$	Operating free-air temperature			0	70	°C

<sup>(1)</sup> All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

<sup>(3)</sup> The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51.



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## **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

ı	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN TYP(1)	MAX	UNIT
		$I_{OH} = -100 \mu A$	3 V to 3.6 V	V <sub>CC</sub> - 0.2		
$V_{OH}$	A to B	$I_{OH} = -8 \text{ mA}$	3 V	2		V
	B to A	$I_{OH} = -6 \text{ mA}$	3 V	2		
		I <sub>OL</sub> = 100 μA	3 V to 3.6 V		0.2	
$V_{OL}$	A to B	I <sub>OL</sub> = 8 mA	3 V		0.8	V
	B to A	I <sub>OL</sub> = 6 mA	3 V		0.8	
I		$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ
		V <sub>I</sub> = 0.8 V	3 V	75		
I <sub>I(hold)</sub>		V <sub>I</sub> = 2 V	3 V	-75		μΑ
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{(2)}$	3.6 V		±500	
I <sub>OZ</sub> (3)		$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ
I <sub>CC</sub>		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ
$\Delta I_{CC}$		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		750	μΑ
Ci	Control inputs	$V_I = V_{CC}$ or GND	3.3 V	4		pF
C <sub>io</sub>	A or B ports	$V_O = V_{CC}$ or GND	3.3 V	8.5		pF

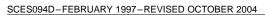
## **TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> = ± 0.3	$V_{CC}$ = 3.3 V $\pm$ 0.3 V		
			MIN	MAX		
f <sub>clock</sub>	Clock frequency			160	MHz	
t <sub>w</sub>	Pulse duration, CLK high or low		2.3		ns	
		A data before CLK↑	1.5			
	Catua tima high ar law	B data before CLK↑	2			
t <sub>su</sub>	Setup time, high or low	Setup time, high or low	DIR before CLK↑	2		ns
		SEL before CLK↑	2			
		A data after CLK↑	0.3			
		B data after CLK↑	0.3			
t <sub>h</sub>	Hold time, high or low	DIR after CLK↑			ns	
		SEL after CLK↑	0.3			

All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to

<sup>(3)</sup> For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.





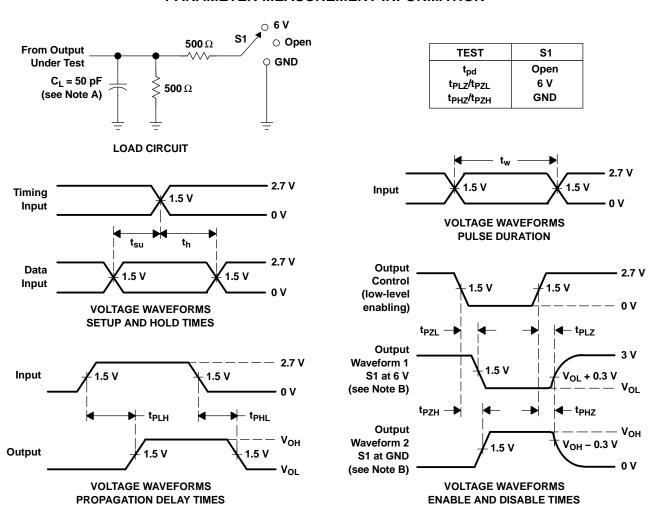
## **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 25 \text{ pF}$  (A port), 80 pF (B port) (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3. ± 0.3	UNIT	
	(INPOT)	(001P01)	MIN	MAX	
f <sub>max</sub>			160		MHz
	CLK	Α	1.5	5	20
t <sub>pd</sub>	CLK	В	1.5	7.4	ns
	CLK	Α	1.5	6.3	
	CLK	В	1.5	9.4	20
t <sub>en</sub>	ŌĒ	A	1.5	6	ns
	OE	В	1.5	9.5	
	CLK	A	1.5	6.4	
	CLK	В	1.5	7.8	no
t <sub>dis</sub>	ŌĒ	A	1.5	5	ns
	OE .	В	1.5	7.6	



#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - D. The output is measured with one input transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms





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#### PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
74ALVCHG162282GRE4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCHG162282GRG4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCHG162282DBBR	OBSOLETE	TSSOP	DBB	80		TBD	Call TI	Call TI
SN74ALVCHG162282GR	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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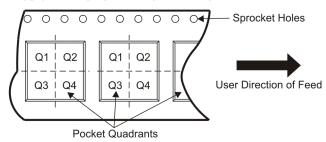
## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

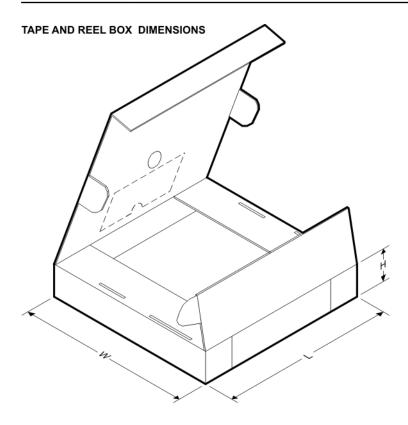
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

	Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN7	4ALVCHG162282GR	TSSOP	DBB	80	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1





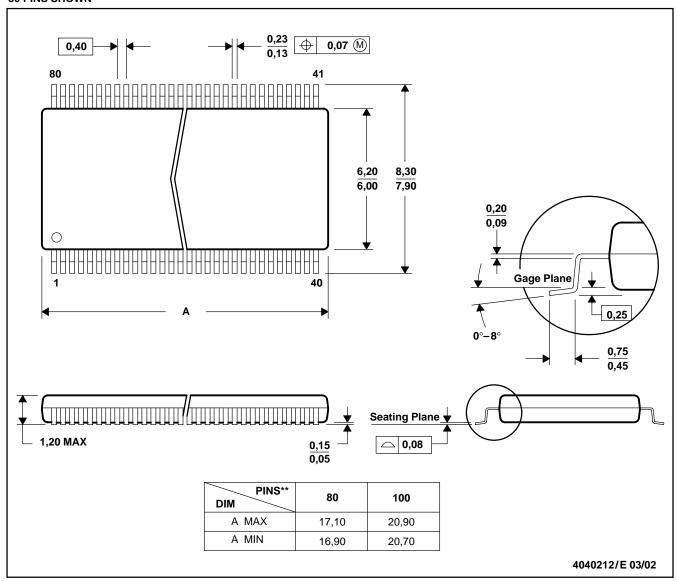
#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCHG162282GR	TSSOP	DBB	80	2000	346.0	346.0	41.0

# DBB (R-PDSO-G\*\*)

#### **80 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC: 80 Pin - MO-153 Variation FF

100 Pin - MO-194 Variation BB

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