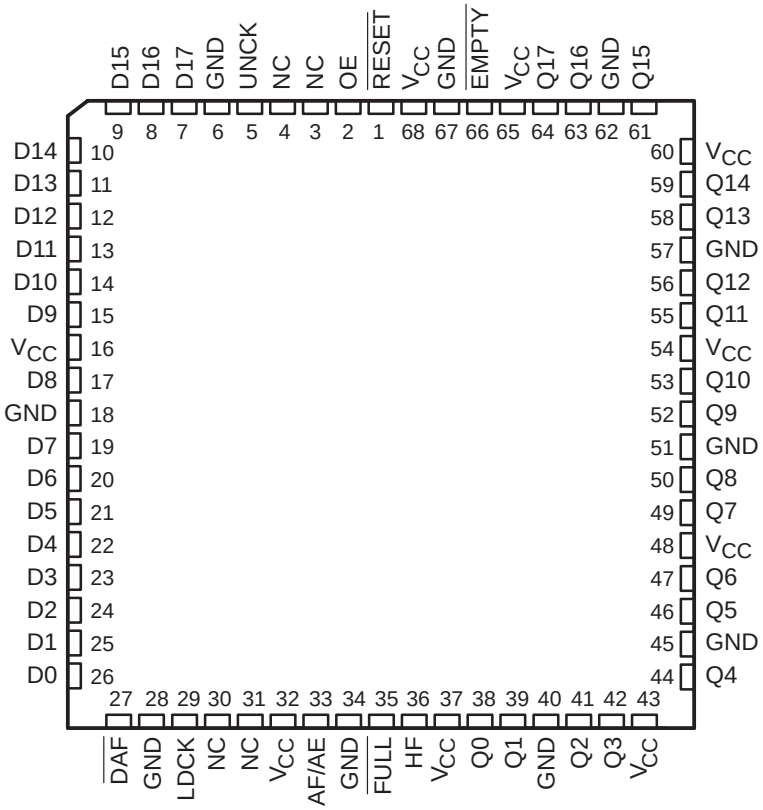
- **Member of the Texas Instruments Widebus™ Family**
- **Low-Power Advanced CMOS Technology**
- **Load and Unload Clocks Can Be Asynchronous or Coincident**
- **1024 Words × 18 Bits**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Empty, Full, and Half-Full Flags**
- **Fast Access Times of 30 ns With a 50-pF Load**
- **Fall-Through Time Is 20 ns Typical**
- **Data Rates up to 40 MHz**
- **High-Output Drive for Direct Bus Interface**
- **3-State Outputs**
- **Package Options Include 68-Pin (FN) and 80-Pin Thin Quad Flat (PN) Packages**

FN PACKAGE
(TOP VIEW)

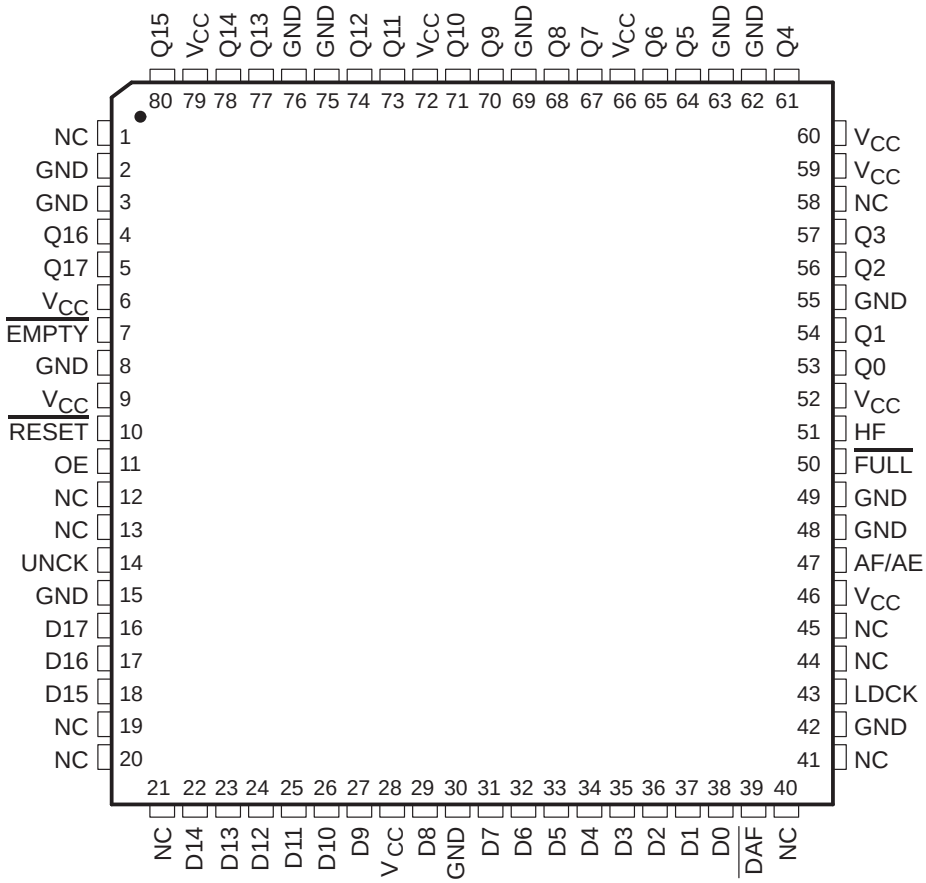


NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7802 is a 1024-word by 18-bit FIFO for high-speed applications. It processes data in a bit-parallel format at rates up to 40 MHz and access times of 30 ns.

Data is written into the FIFO memory on a low-to-high transition on the load-clock (LDCK) input and is read out on a low-to-high transition on the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 1024 the number of words clocked out. When the memory is full, LDCK has no effect on the data in the memory; when the memory is empty, UNCK has no effect.

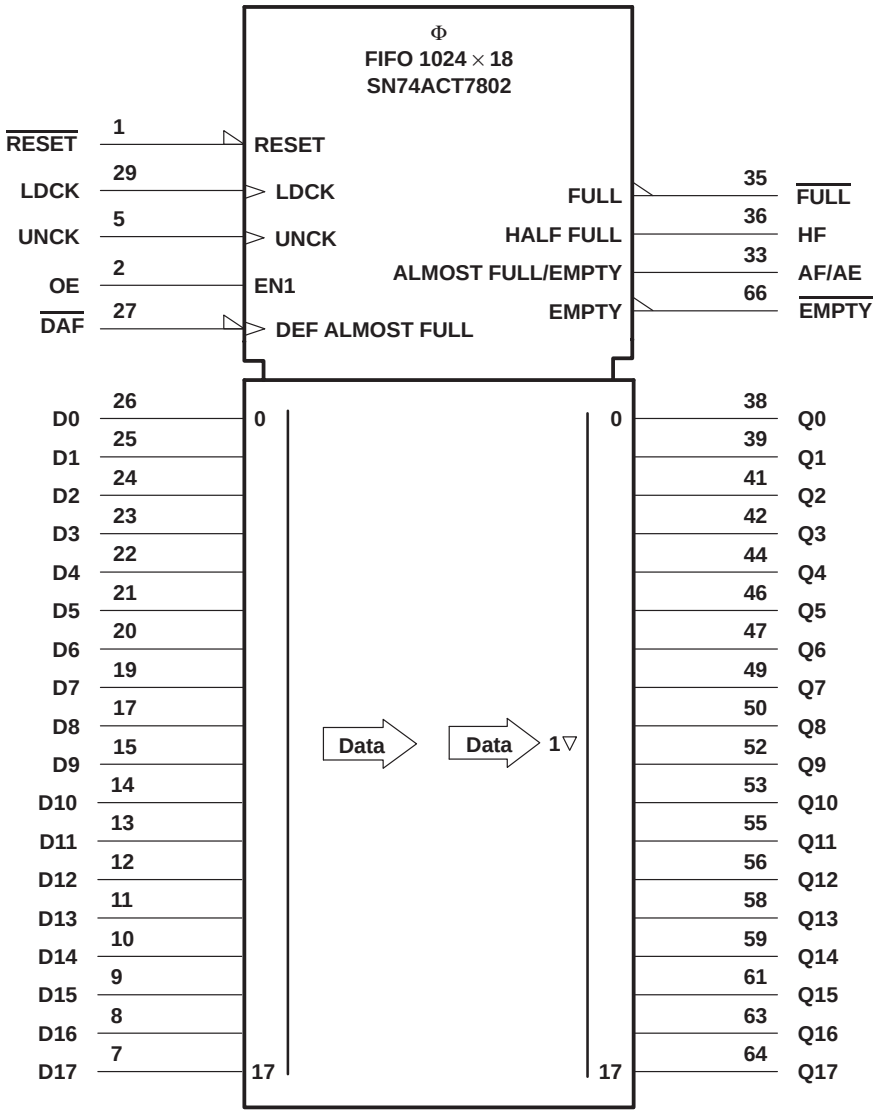
A low level on the reset ($\overline{\text{RESET}}$) input resets the FIFO internal clock stack pointers and sets full ($\overline{\text{FULL}}$) high, almost full/almost empty (AF/AE) high, half full (HF) low, and empty ($\overline{\text{EMPTY}}$) low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The Q outputs are noninverting and are in the high-impedance state when the output-enable (OE) input is low.

When writing to the FIFO after a reset pulse or when the FIFO is empty, the first active transition on LDCK drives $\overline{\text{EMPTY}}$ high and causes the first word written to the FIFO to appear on the Q outputs. An active transition on UNCK is not required to read the first word written to the FIFO. Each subsequent read from the FIFO requires an active transition on UNCK.

The SN74ACT7802 can be cascaded in the word-width direction but not in the word-depth direction.

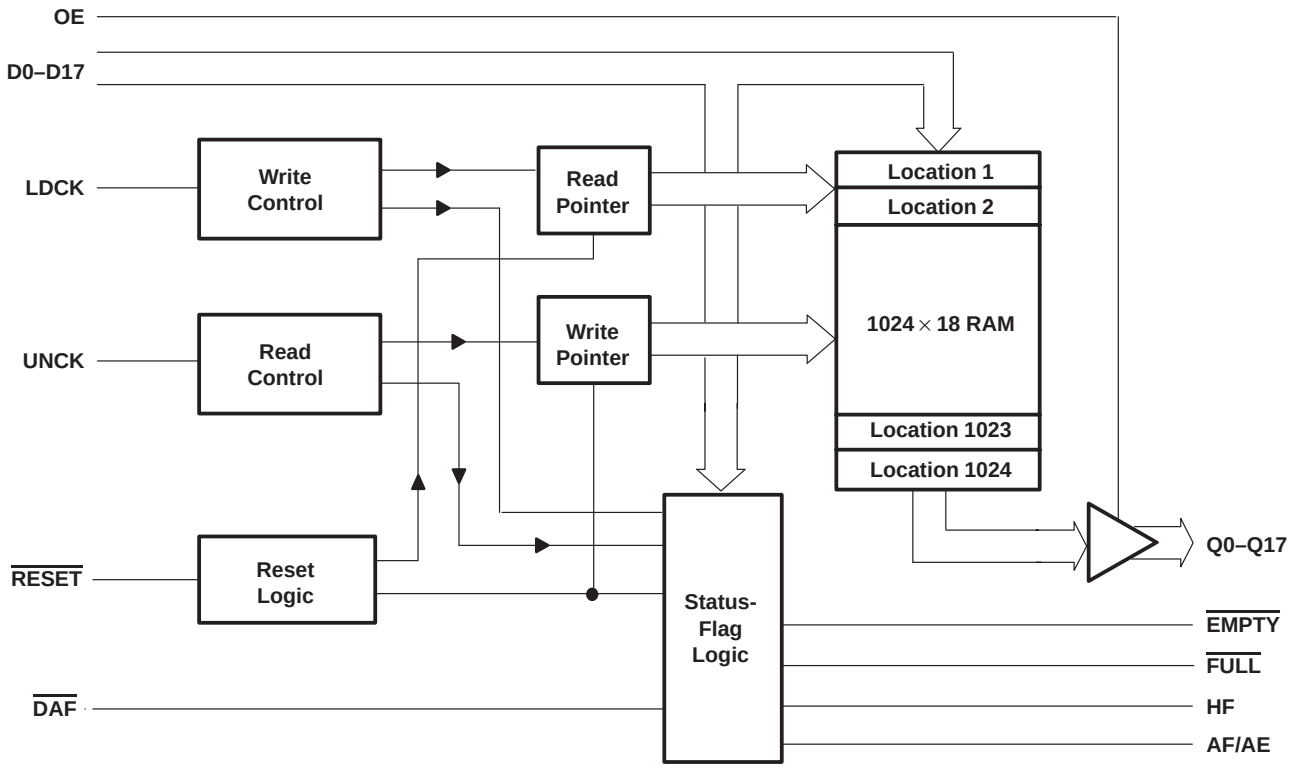
The SN74ACT7802 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AE, or the default value of 256 can be used for the almost-empty almost-full offset (X). AF/AE is high when memory contains X or fewer words or (1024 – X) or more words. AF/AE is high after reset.
$\overline{\text{DAF}}$	27	I	Define almost-full flag. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the AF/AE offset value (X). With DAF held low, a low pulse on RESET defines AF/AE using X.
D0–D17	7–15, 17, 19–26	I	18-bit data input port
$\overline{\text{EMPTY}}$	66	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	35	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	36	O	Half-full flag. HF is high when the FIFO memory contains 512 or more words. HF is low after reset.
LDCK	29	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
OE	2	I	Output enable. When OE is low, the data outputs are in the high-impedance state.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	18-bit data-output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	5	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

† Terminal numbers listed are for the FN package.

offset value values for AF/AE

The FIFO memory status is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, HF, and AF/AE flags. The $\overline{\text{FULL}}$ output is low when the memory is full; the $\overline{\text{EMPTY}}$ output is low when the memory is empty. The HF output is high when the memory contains 512 or more words and low when it contains fewer than 512 words. The level of the AF/AE flag is determined by both the number of words in the FIFO and a user-definable offset X. AF/AE is high when the FIFO is almost full or almost empty, i.e., when it contains X or fewer words or (1024 – X) or more words. The AF/AE offset value is either user-defined or the default value of 256; it is programmed during each reset cycle as follows:

user-defined X:

Take $\overline{\text{DAF}}$ from high to low.

If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low.

With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE flag using X.

default X:

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.

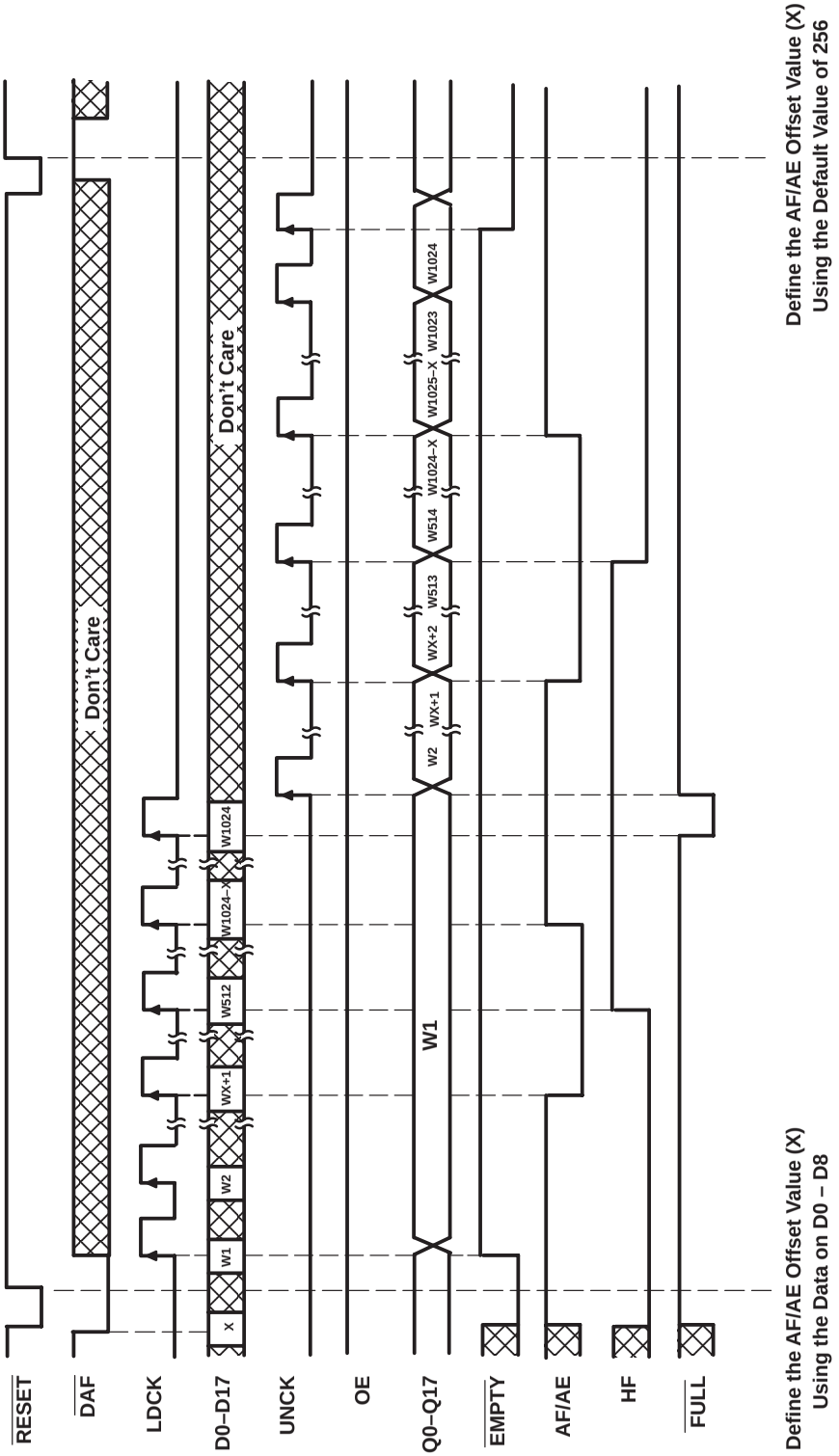


Figure 1. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Voltage range applied to a disabled 3-state output . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): FN package . . . . . 39°C/W
PN package . . . . . 62°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		’ACT7802-25		’ACT7802-40		’ACT7802-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V
I_{OH}	High-level output current		–8		–8		–8	mA
I_{OL}	Low-level output current		16		16		16	mA
T_A	Operating free-air temperature	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –8 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}§	V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}§	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz			4		pF
C_o	V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} tested with outputs open

timing requirements over recommended operating conditions (see Figures 1 and 2)

			'ACT7802-25		'ACT7802-40		'ACT7802-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			40		25		16.7	MHz
t_w	Pulse duration	LDCK high or low	10		14		20		ns
		UNCK high or low	10		14		20		
		$\overline{DAF}$ high	10		10		10		
		$\overline{RESET}$ low	20		25		25		
t_{su}	Setup time	D0–D7 before LDCK↑	4		5		5		ns
		$\overline{RESET}$ inactive (high) before LDCK↑	5		5		5		
		Define AF/AE: D0–D8 before $\overline{DAF}$↓	5		5		5		
		Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑	7		7		7		
		Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑	5		5		5		
t_h	Hold time	D0–D7 after LDCK↑	1		2		2		ns
		Define AF/AE: D0–D8 after $\overline{DAF}$↓	0		0		0		
		Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑	0		0		0		
		Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑	0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 1 and 2)

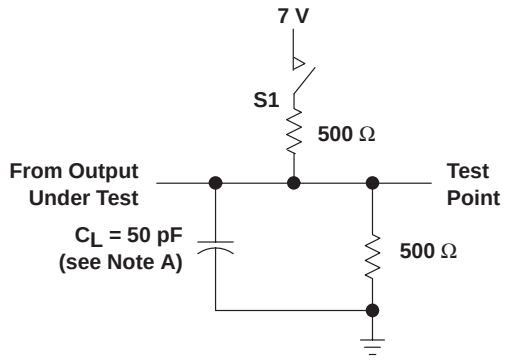
PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7802-25			'ACT7802-40		'ACT7802-60		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		40			25		16.7		MHz
t_{pd}	LDCK↑	Any Q	8	20	30	8	35	8	45	ns
	UNCK↑		12		30	12	35	12	45	
t_{pd}‡	UNCK↑	Any Q		21						ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$	4		18	4	20	4	22	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	2		18	2	20	2	22	ns
	$\overline{RESET}$↓		2		18	2	20	2	22	
	LDCK↑	$\overline{FULL}$	4		18	4	20	4	22	
t_{PLH}	UNCK↑	$\overline{FULL}$	4		17	4	19	4	21	ns
	$\overline{RESET}$↓		2		17	2	19	2	21	
t_{pd}	LDCK↑	AF/AE	2		20	2	22	2	24	ns
	UNCK↑		2		20	2	22	2	24	
t_{PLH}	$\overline{RESET}$↓	AF/AE	2		17	2	19	2	21	ns
	LDCK↑	HF	2		18	2	20	2	22	
t_{PHL}	UNCK↑	HF	2		18	2	20	2	22	ns
	$\overline{RESET}$↓		2		17	2	19	2	21	
t_{en}	OE	Any Q	2		12	2	14	2	16	ns
t_{dis}	OE	Any Q	2		14	2	16	2	18	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured with C_L = 30 pF (see Figure 3).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

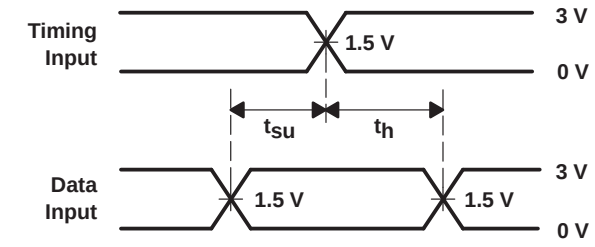
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per channel	C_L = 50 pF, f = 5 MHz	65	pF

PARAMETER MEASUREMENT INFORMATION

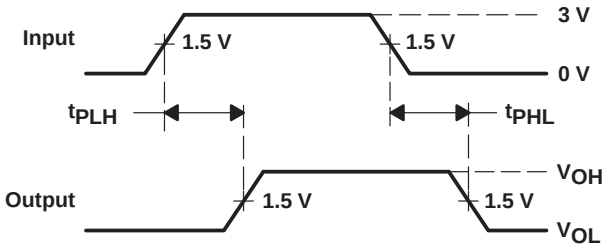


LOAD CIRCUIT

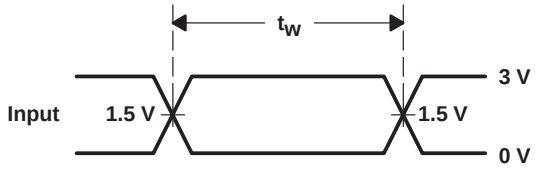
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



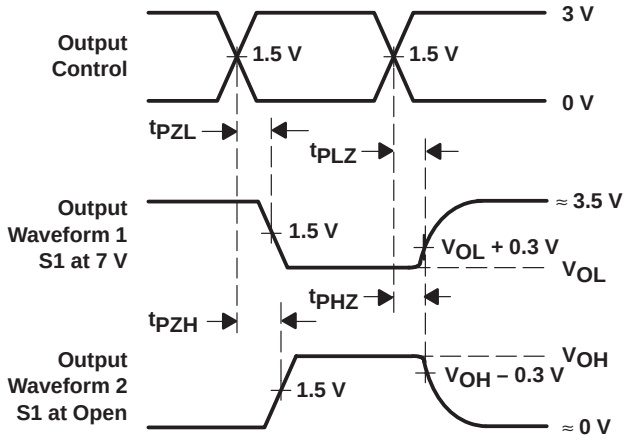
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

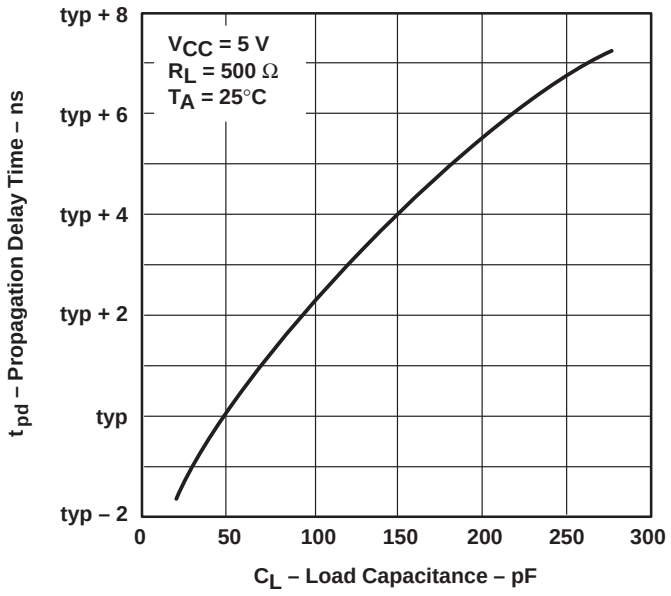


Figure 3

POWER DISSIPATION CAPACITANCE vs SUPPLY VOLTAGE

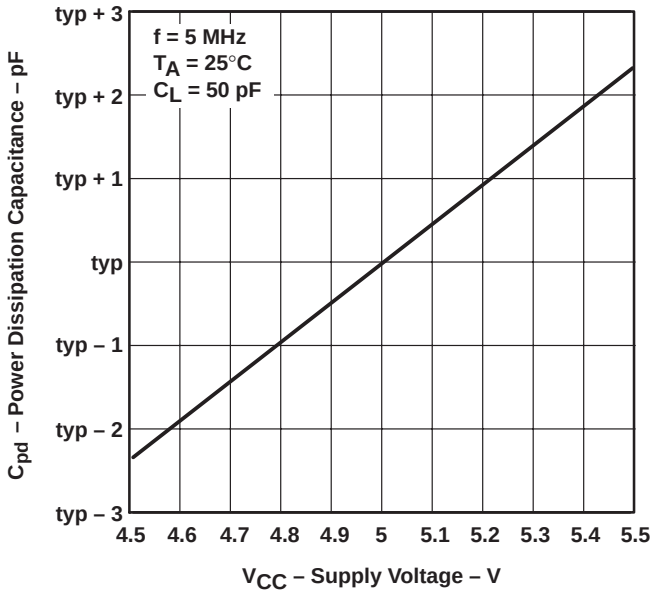


Figure 4

APPLICATION INFORMATION

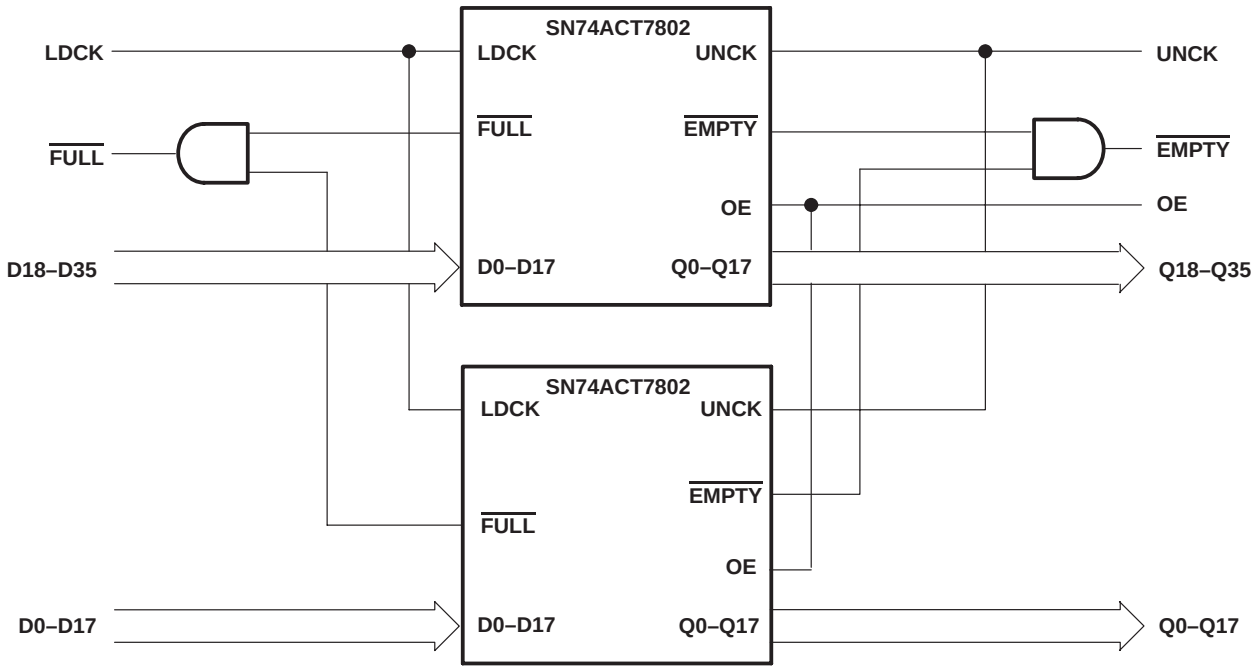


Figure 5. Word-Width Expansion: 1024 × 36 Bit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT7802-25FN	ACTIVE	PLCC	FN	68	18	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	SN74 ACT7802-25FN	Samples
SN74ACT7802-40PN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	ACT7802-40	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

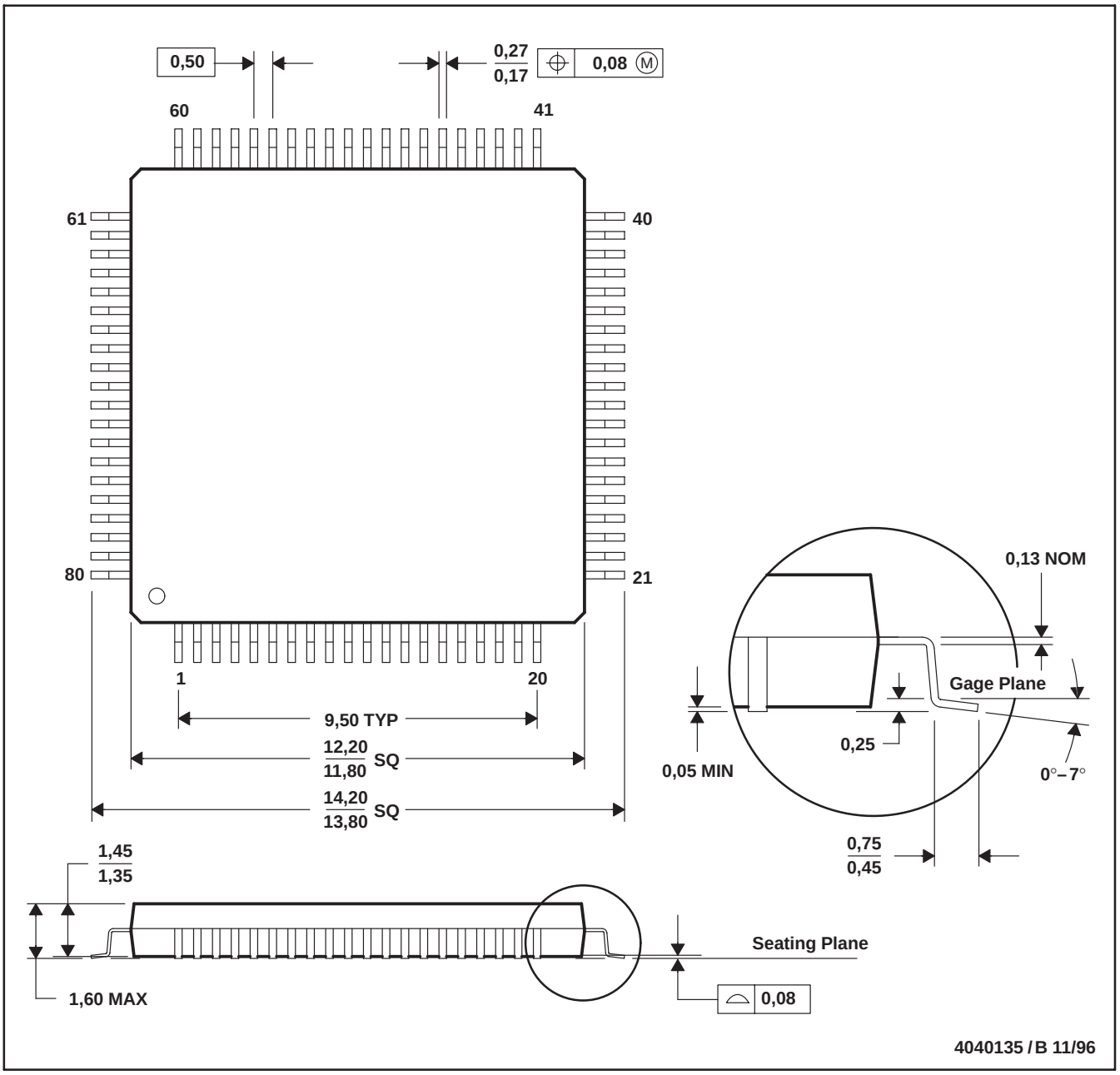
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

GENERIC PACKAGE VIEW

FN 68

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

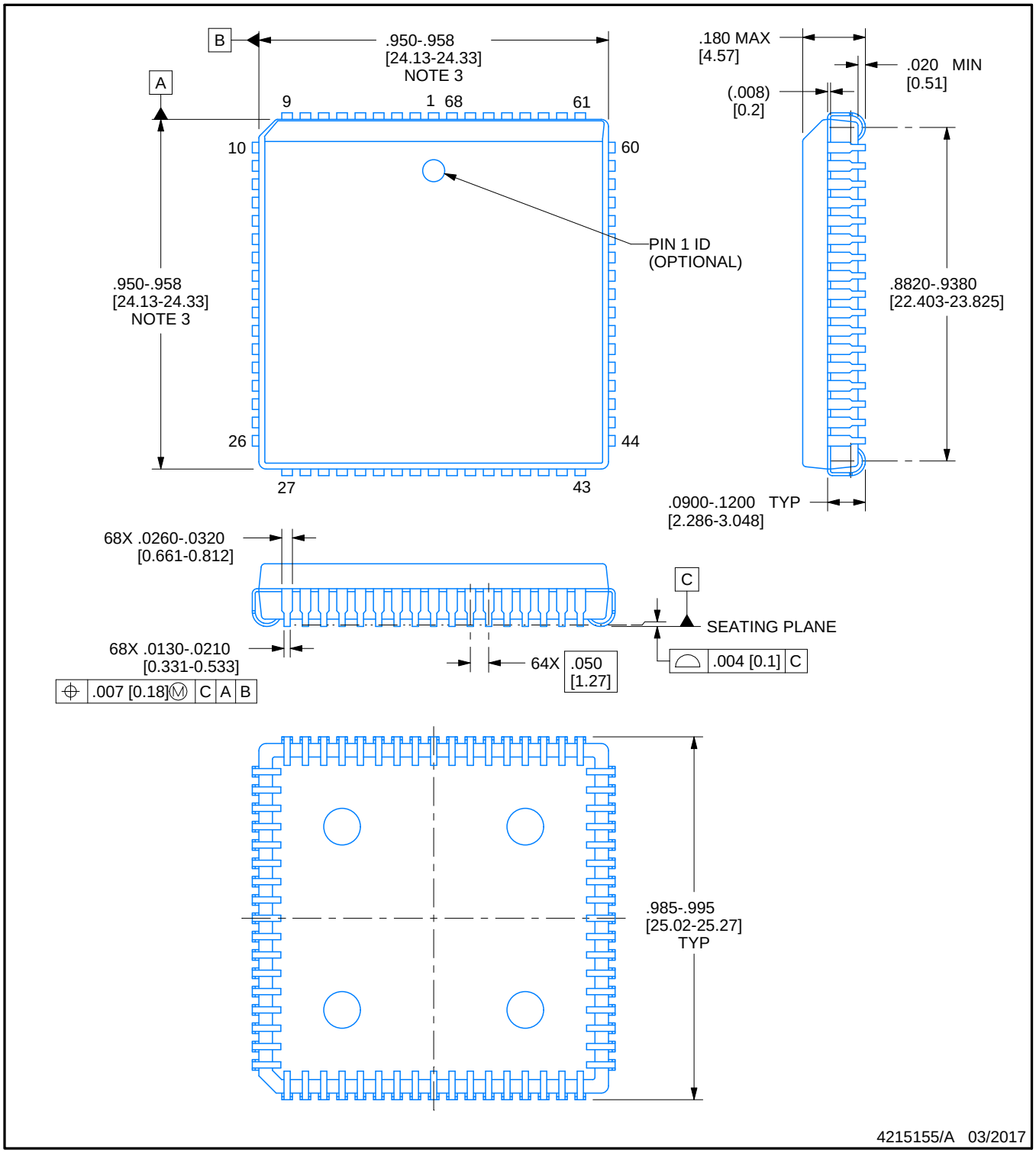
4040005-6/C

PACKAGE OUTLINE

FN0068A

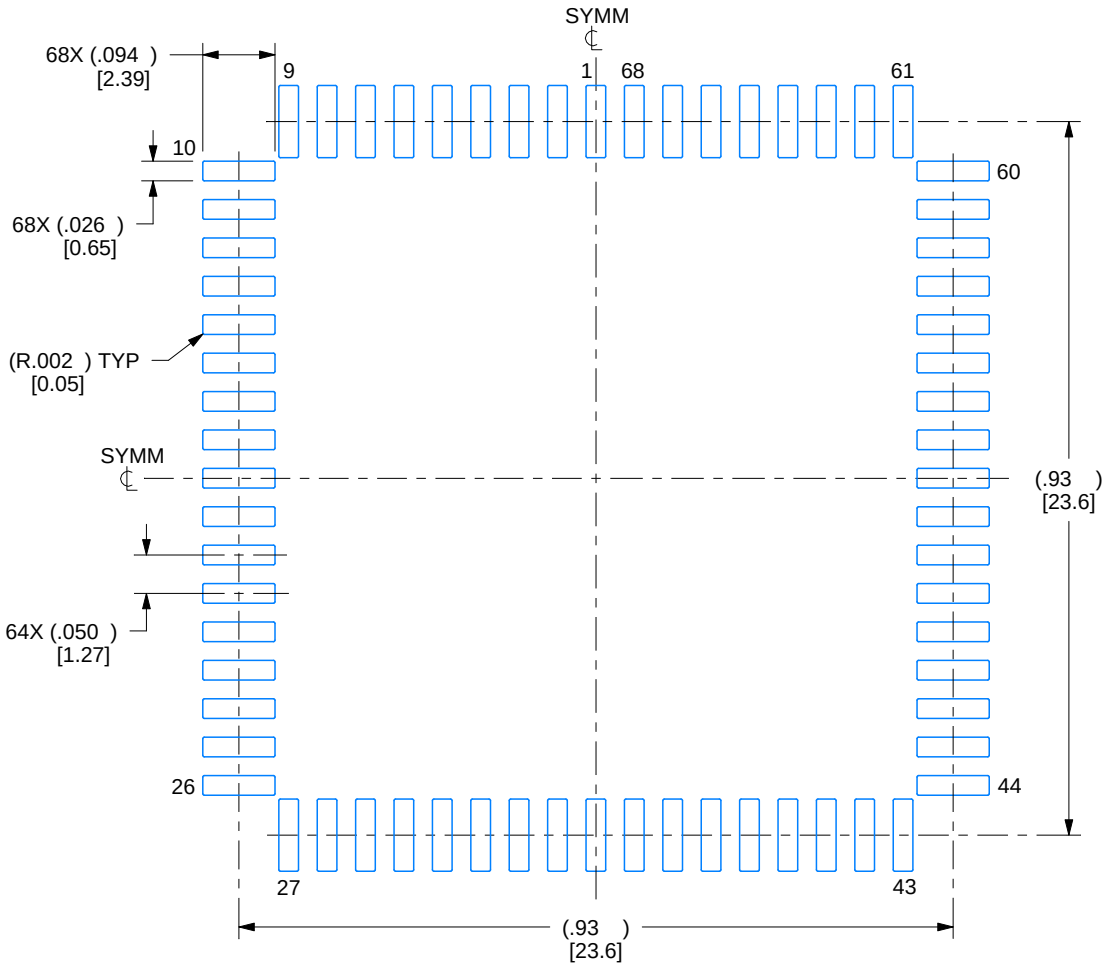
PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



NOTES:

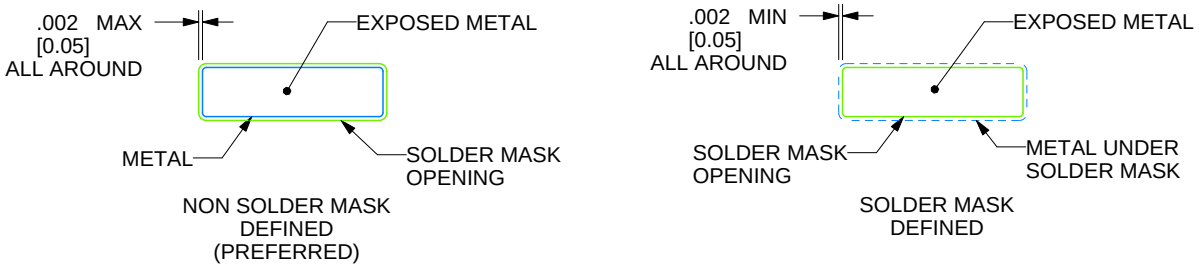
1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:4X

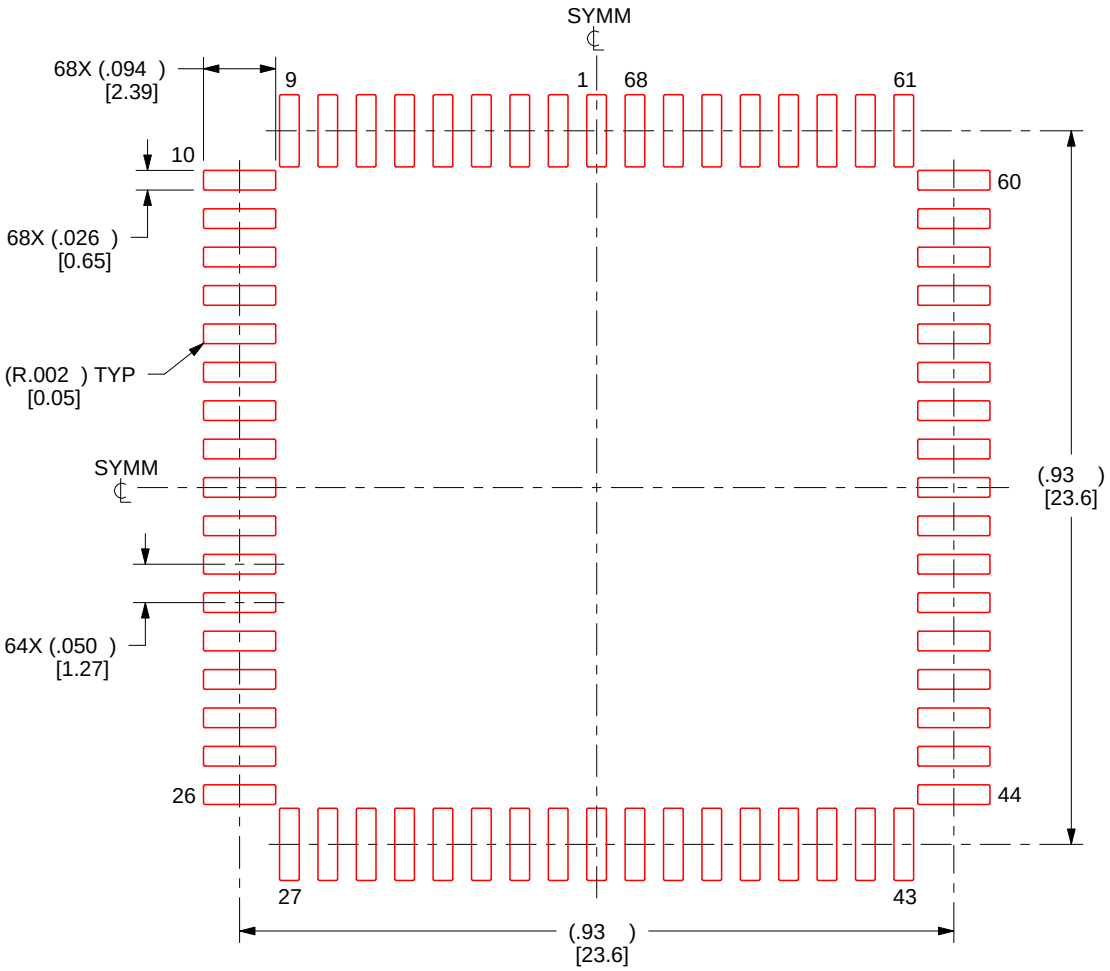


SOLDER MASK DETAILS

4215155/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:4X

4215155/A 03/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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