

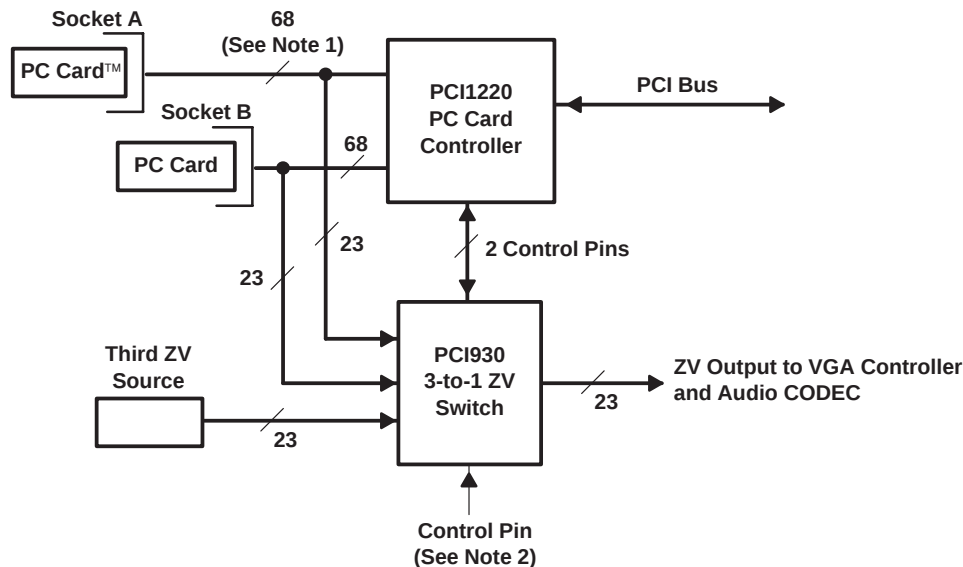
- Zoomed Video Switch – Supports up to 3 ZV Sources
- Designed for Use With the TI™ PCI1220/1221 Leadership PC Card Controllers
- First two (2) ZV Inputs are Controlled by PCI1220/1221 Control Signal Outputs
- 100% Compliant With the PCMCIA Zoomed Video Standard
- Status Bit Indicates ZV Activity – Can be Used to Switch a Fourth External ZV Source
- Switching can be Software Programmed Using Registers in the PCI1220/1221
- Low Power 3.3-Volt Core Logic
- Small Form Factor 128-Pin TQFP Package

description

The 3-to-1 ZV switch is a companion chip to the PCI1220/1221 PC Card controllers; however, it can be used in other applications where multiple ZV sources require external buffering. The ZV switch is a 3:1 multiplexer for the 23 pins defined in the PCMCIA zoomed video interface. The ZV interface includes both the video and audio data as defined by the *Zoomed Video Specification*.

The three ZV source interfaces are referred to as A, B, and C. ZV sources A and B are intended for use with the PCI1220/1221 PC Card zoom video outputs. The third source, C, may be from a variety of external ZV sources.

An advanced CMOS process is used to achieve low system-power consumption.

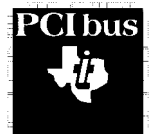


- NOTES: 1. The PC Card interface is 68 pins for CardBus and 16-bit PC Cards. In zoomed-video mode 23 pins are used for routing the zoomed video signals too the VGA controller.
2. Control pin for third ZV source (Can Use GPO From PCI1220).

Figure 1. System-Level Diagram for PCI930 with the PCI1220 PC Card Controller



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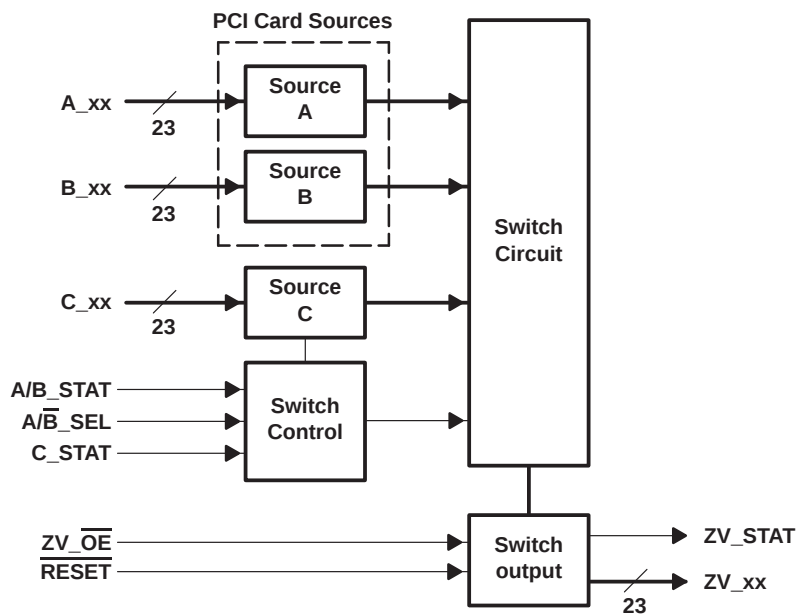
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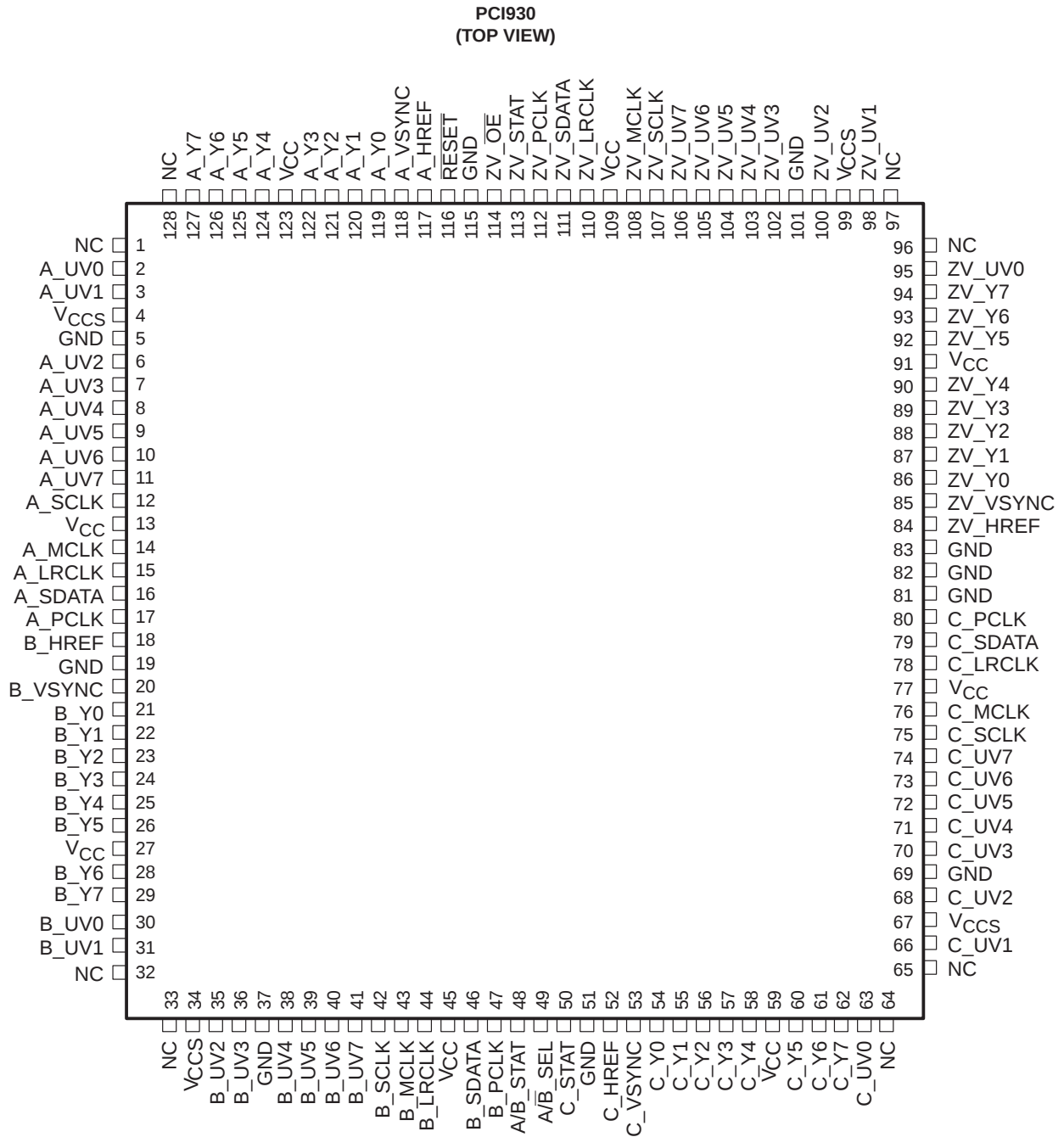
3-TO-1 ZOOMED VIDEO SWITCH

SCPS018B – OCTOBER 1997 – REVISED DECEMBER 1997

functional block diagram



terminal assignments



PCI930

3-TO-1 ZOOMED VIDEO SWITCH

SCPS018B – OCTOBER 1997 – REVISED DECEMBER 1997

Table 1. Terminal Assignments Sorted by Pin Number

TERMINAL NO. NAME	TERMINAL NO. NAME	TERMINAL NO. NAME
1 NC	44 B_LRCLK	87 ZV_Y1
2 A_UV0	45 V _{CC}	88 ZV_Y2
3 A_UV1	46 B_SDATA	89 ZV_Y3
4 V _{CCS}	47 B_PCLK	90 ZV_Y4
5 GND	48 A/B_STAT	91 V _{CC}
6 A_UV2	49 A/B_SEL	92 ZV_Y5
7 A_UV3	50 C_STAT	93 ZV_Y6
8 A_UV4	51 GND	94 ZV_Y7
9 A_UV5	52 C_HREF	95 ZV_UV0
10 A_UV6	53 C_VSYNC	96 NC
11 A_UV7	54 C_Y0	97 NC
12 A_SCLK	55 C_Y1	98 ZV_UV1
13 V _{CC}	56 C_Y2	99 V _{CCS}
14 A_MCLK	57 C_Y3	100 ZV_UV2
15 A_LRCLK	58 C_Y4	101 GND
16 A_SDATA	59 V _{CC}	102 ZV_UV3
17 A_PCLK	60 C_Y5	103 ZV_UV4
18 B_HREF	61 C_Y6	104 ZV_UV5
19 GND	62 C_Y7	105 ZV_UV6
20 B_VSYNC	63 C_UV0	106 ZV_UV7
21 B_Y0	64 NC	107 ZV_SCLK
22 B_Y1	65 NC	108 ZV_MCLK
23 B_Y2	66 C_UV1	109 V _{CC}
24 B_Y3	67 V _{CCS}	110 ZV_LRCLK
25 B_Y4	68 C_UV2	111 ZV_SDATA
26 B_Y5	69 GND	112 ZV_PCLK
27 V _{CC}	70 C_UV3	113 ZV_STAT
28 B_Y6	71 C_UV4	114 ZV_OE
29 B_Y7	72 C_UV5	115 GND
30 B_UV0	73 C_UV6	116 RESET
31 B_UV1	74 C_UV7	117 A_HREF
32 NC	75 C_SCLK	118 A_VSYNC
33 NC	76 C_MCLK	119 A_Y0
34 V _{CCS}	77 V _{CC}	120 A_Y1
35 B_UV2	78 C_LRCLK	121 A_Y2
36 B_UV3	79 C_SDATA	122 A_Y3
37 GND	80 C_PCLK	123 V _{CC}
38 B_UV4	81 GND	124 A_Y4
39 B_UV5	82 GND	125 A_Y5
40 B_UV6	83 GND	126 A_Y6
41 B_UV7	84 ZV_HREF	127 A_Y7
42 B_SCLK	85 ZV_VSYNC	128 NC
43 B_MCLK	86 ZV_Y0	*** ***



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Table 2. Terminal Assignments Sorted by Pin Name

TERMINAL		TERMINAL		TERMINAL	
NO.	NAME	NO.	NAME	NO.	NAME
49	A/B_SEL	24	B_Y3	65	NC
48	A/B_STAT	25	B_Y4	96	NC
117	A_HREF	26	B_Y5	97	NC
15	A_LRCLK	28	B_Y6	128	NC
14	A_MCLK	29	B_Y7	116	RESET
17	A_PCLK	52	C_HREF	13	V _{CC}
12	A_SCLK	78	C_LRCLK	27	V _{CC}
16	A_SDATA	76	C_MCLK	45	V _{CC}
2	A_UV0	80	C_PCLK	59	V _{CC}
3	A_UV1	75	C_SCLK	77	V _{CC}
6	A_UV2	79	C_SDATA	91	V _{CC}
7	A_UV3	50	C_STAT	109	V _{CC}
8	A_UV4	63	C_UV0	123	V _{CC}
9	A_UV5	66	C_UV1	4	V _{CCS}
10	A_UV6	68	C_UV2	34	V _{CCS}
11	A_UV7	70	C_UV3	67	V _{CCS}
118	A_VSYNC	71	C_UV4	99	V _{CCS}
119	A_Y0	72	C_UV5	84	ZV_HREF
120	A_Y1	73	C_UV6	110	ZV_LRCLK
121	A_Y2	74	C_UV7	108	ZV_MCLK
122	A_Y3	53	C_VSYNC	114	ZV_OE
124	A_Y4	54	C_Y0	112	ZV_PCLK
125	A_Y5	55	C_Y1	107	ZV_SCLK
126	A_Y6	56	C_Y2	111	ZV_SDATA
127	A_Y7	57	C_Y3	113	ZV_STAT
18	B_HREF	58	C_Y4	85	ZV_VSYNC
44	B_LRCLK	60	C_Y5	95	ZV_UV0
43	B_MCLK	61	C_Y6	98	ZV_UV1
47	B_PCLK	62	C_Y7	100	ZV_UV2
42	B_SCLK	5	GND	102	ZV_UV3
46	B_SDATA	19	GND	103	ZV_UV4
30	B_UV0	37	GND	104	ZV_UV5
31	B_UV1	51	GND	105	ZV_UV6
35	B_UV2	69	GND	106	ZV_UV7
36	B_UV3	81	GND	86	ZV_Y0
38	B_UV4	82	GND	87	ZV_Y1
39	B_UV5	83	GND	88	ZV_Y2
40	B_UV6	101	GND	89	ZV_Y3
41	B_UV7	115	GND	90	ZV_Y4
20	B_VSYNC	1	NC	92	ZV_Y5
21	B_Y0	32	NC	93	ZV_Y6
22	B_Y1	33	NC	94	ZV_Y7
23	B_Y2	64	NC	***	***

PCI930

3-TO-1 ZOOMED VIDEO SWITCH

SCPS018B – OCTOBER 1997 – REVISED DECEMBER 1997

Table 3. ZV Switch Control and Status Terminals

TERMINAL NAME	NO.	TYPE	FUNCTION
$\overline{\text{RESET}}$	116	I	Chip reset. When asserted (driven low), the chip three-states all outputs. In addition, the PCI930 checks for a pullup resistor on the A/B_STAT pin as denoted under ZV_xx terminal function.
A/B_STAT	48	I	PC Card ZV (Socket 0 or 1) active. This input indicates that either the A or B source from the PC Card controller is active. This signal is used with A/B_SEL to determine which socket ZV source drives the ZV_xx outputs. The A or B source can be passed to ZV_xx if the C source is either of lower precedence, or is not sourcing valid ZV data, as indicated by the C_STAT signal.
A/B_SEL	49	I	Socket A/B select. When this pin and A/B_STAT are high, the PC Card socket A ZV data is valid. When this pin is low, and the A/B_STAT input is high, the PC Card socket B ZV data is valid. This input has no meaning if the A/B_STAT input is low.
C_STAT	50	I	C source status. When this input is high, the ZV source from interface C is valid, and can be driven to the ZV_xx outputs. The C source can be passed to ZV_xx if the A and B sources are either of lower precedence, or A or B is not sourcing valid ZV data.
ZV_OE	114	I	ZV output I/F enable. When this terminal is low, the ZV switch drives the ZV_xx terminals.
ZV_STAT	113	O	ZV output status. This terminal is driven high when the ZV switch drives the ZV_xx terminals.
ZV_xx State	N/A	N/A	When a pullup resistor is present on the A/B_STAT pin during $\overline{\text{RESET}}$, then the ZV_xx interface is three-stated if the ZV_xx interface is inactive. During the default state, no pullup resistor, a reset drives the ZV_xx interface to a logic low state when inactive.

Terminal Functions

Table 4. Power Supply Terminal Functions

NAME	TERMINAL NO.	TYPE	FUNCTION
GND	5, 19, 51, 69, 81, 82, 83, 101, 115	I	Device ground terminals.
V _{CC}	13, 27, 45, 59, 77, 91, 109, 123	I	3.3V power supply input for core.
V _{CCS}	4, 34, 67, 99	I	Rail input for 5V tolerance on zoom video streams

Table 5. ZV Stream Interface

NAME	TERMINAL NO.	TYPE	FUNCTION
HREF	18, 52, 84, 117	†	Horizontal sync to ZV port.
VS _{YNC}	20, 53, 85, 118	†	Vertical sync to ZV port.
Y7:0	A ₋ = 127, 126, 125, 124, 122, 121, 120, 119 B ₋ = 29, 28, 26, 25, 24, 23, 22, 21 C ₋ = 62, 61, 60, 58, 57, 56, 55, 54 ZV ₋ = 94, 93, 92, 90, 89, 88, 87, 86	I I I O	Video data to ZV port YUV:4:2:2 format. Video data to ZV port YUV:4:2:2 format. Video data to ZV port YUV:4:2:2 format. Video data YUV:4:2:2 format.
UV7:0	A ₋ = 11, 10, 9, 8, 7, 6, 3, 2 B ₋ = 41, 40, 39, 38, 36, 35, 31, 30 C ₋ = 74, 73, 72, 71, 70, 68, 66, 63 ZV ₋ = 106, 105, 104, 103, 102, 100, 98, 95	I I I O	Video data to ZV port YUV:4:2:2 format. Video data to ZV port YUV:4:2:2 format. Video data to ZV port YUV:4:2:2 format. Video data YUV:4:2:2 format.
SCLK	12, 42, 75, 107	†	Audio SCLK PCM signal.
MCLK	14, 43, 76, 108	†	Audio MCLK PCM signal.
PCLK	17, 47, 80, 112	†	Pixel clock to ZV port.
LRCLK	15, 44, 78, 110	†	Audio LRCLK PCM signal.
SDATA	16, 46, 79, 111	†	Audio PCM data signal.

† Inputs on A, B, and C source ports; Outputs to ZV_{-xx} interface

control settings for ZV switch routing

Table 6 lists termination conditions that can exercise control over the ZV switch and shows the results.

Table 6. Termination Conditions

FUNCTION	CONDITION	RESULT
ZV _{-xx} inactive state	Pullup resistor on A/B _{-STAT}	ZV _{-xx} three-stated
	No pullup resistor on A/B _{-STAT}	ZV _{-xx} driven L
C precedence control	Pullup resistor on A/B _{-SEL}	C takes precedence over A/B.
	No pullup resistor on A/B _{-SEL}	A/B takes precedence over C.

PCI930

3-TO-1 ZOOMED VIDEO SWITCH

SCPS018B – OCTOBER 1997 – REVISED DECEMBER 1997

Table 7 and Table 8 define the control settings that allow the PCI930 to route the ZV data from the three inputs (A_xx, B_xx, or C_xx) to the output (ZV_xx). The Tables are separated based upon the configuration of the PCI930.

- Table 7: Output when inputs A/B have precedence over C
- Table 8: Output when input C has precedence over A/B

Table 7. Output When Inputs A/B Have Precedence Over Input C

INPUTS			CONTROL SETTINGS				OUTPUT at ZV_xx
A_XX	B_XX	C_XX	A/B_STAT	A/B_SEL	C_STAT	ZV_OE	
X	X	X	X	X	X	1	†
Non ZV data	Non ZV data	Non ZV data	0	X	0	X	†
Non ZV data	Non ZV data	ZV data	0	X	1	X	C_xx
Non ZV data	ZV data	Non ZV data	1	0	X	0	B_xx
Non ZV data	ZV data	ZV data	1	0	X	0	B_xx
			0	X	1	0	C_xx
ZV data	Non ZV data	Non ZV data	1	1	X	0	A_xx
ZV data	Non ZV data	ZV data	1	1	X	0	A_xx
			0	X	1	0	C_xx
ZV data	ZV data	Non ZV data	1	1	X	0	A_xx
			1	0	X	0	B_xx
ZV data	ZV data	ZV data	1	1	X	0	A_xx
			1	0	X	0	B_xx
			0	X	1	0	C_xx

† Inactive state

Table 8. Output When Input C Has Precedence Over A/B

INPUTS			CONTROL SETTINGS				OUTPUT at ZV_xx
A_XX	B_XX	C_XX	A/B_STAT	A/B_SEL	C_STAT	ZV_OE	
X	X	X	X	X	X	1	†
Non ZV data	Non ZV data	Non ZV data	0	X	0	X	†
Non ZV data	Non ZV data	ZV data	X	X	1	0	C_xx
Non ZV data	ZV data	Non ZV data	1	0	0	0	B_xx
Non ZV data	ZV data	ZV data	1	0	0	0	B_xx
			X	X	1	0	C_xx
ZV data	Non ZV data	Non ZV data	1	1	0	0	A_xx
ZV data	Non ZV data	ZV data	1	1	0	0	A_xx
			X	X	1	0	C_xx
ZV data	ZV data	Non ZV data	1	1	0	0	A_xx
			1	0	0	0	B_xx
ZV data	ZV data	ZV data	1	1	0	0	A_xx
			1	0	0	0	B_xx
			X	X	1	0	C_xx

† Inactive state



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typical system configuration with PCI1220 PC Card controller

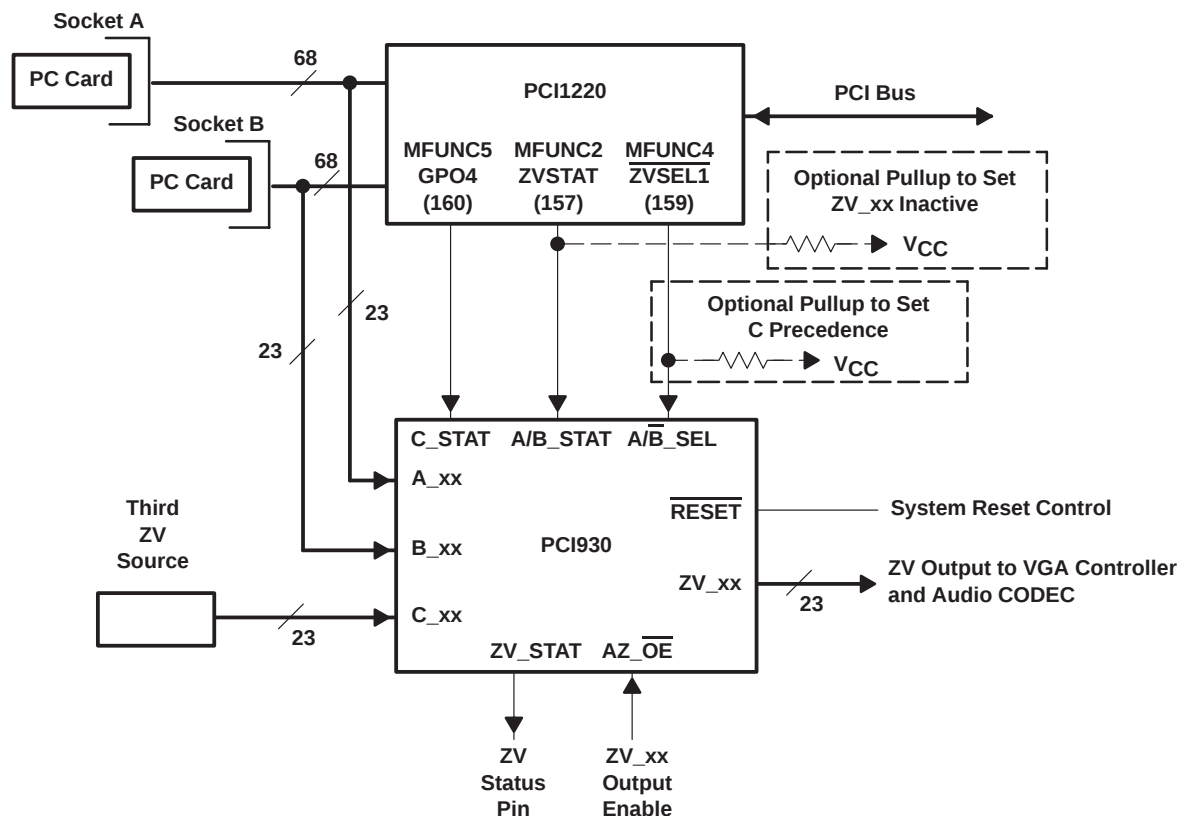


Figure 2. Typical System Configuration for PCI930 With TI PCI1220 PC Card Controller

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6 V
Supply voltage range, V_{CCS}	–0.5 V to 6 V
Input voltage range, V_I	–0.5 V to 6.5 V
Output voltage range, V_O	–0.5 V to $V_{CC} + 0.5$ V
Input Clamp Current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 3)	± 20 mA
Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 4)	± 20 mA
Storage temperature range	–65°C to 150°C
Virtual junction temperature, T_J	150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 3. Applies for external input and bidirectional buffers. $V_I > V_{CC}$ does not apply to fail-safe terminals. ZV terminals are measured with respect to V_{CCS} . The limit specified applies for a DC condition.
4. Applies for external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail-safe terminals. ZV terminals are measured with respect to V_{CCS} . The limit specified applies for a DC condition.

PCI930

3-TO-1 ZOOMED VIDEO SWITCH

SCPS018B – OCTOBER 1997 – REVISED DECEMBER 1997

recommended operating conditions (see Note 5)

PARAMETER		OPERATION	MIN	NOM	MAX	UNIT
V _{CC}	Core voltage – Commercial	3.3 V	3	3.3	3.6	V
V _{CCS}	I/O voltage – Commercial	5 V	4.75	5	5.25	V
V _{IH}	High-level input voltage [†]		2		V _{CCS}	V
V _{IL}	Low-level input voltage [†]		0		0.8	V
V _I	Input voltage		0		V _{CCS}	V
V _O	Output voltage [‡]		0		V _{CCS}	V
t _t	Input transition (rise and fall) time, see Figure 3		0		25	ns
T _A	Operating ambient temperature range		0	25	70	°C
T _J	Virtual junction temperature [§]		0	25	115	°C

NOTE 5: Unused or floating pins (input or I/O) must be held high or low.

[†] Applies for external input and bidirectional buffers without hysteresis

[‡] Applies for external output buffers.

[§] These junction temperatures reflect simulation conditions. Customer is responsible for verifying junction temperature.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V _{OH}	High-level output voltage		I _{OH} = –3.6 mA	2.15		V
V _{OL}	Low-level output voltage		I _{OL} = 6.48 mA		0.5	V
I _{OZL}	3-state-output Hi-Z current [¶]	5.5 V	V _I = GND		–10	μA
I _{OZH}	3-state-output Hi-Z current [¶]	5.5 V	V _I = V _{CC}		10	μA
I _{IL}	Low-level input current [#]		V _I = GND		–1	μA
I _{IH}	High-level input current	input pins	5.5 V	V _I = V _{CC}	1	μA
		A/B_STAT	5.0 V	V _I = 3.0 V	230	
		A/B_SEL	5.0 V	V _I = 3.0 V	230	

[¶] I_{OZ} is not tested on ZV_STAT(pin 113) due to no Z state.

[#] I_{IL} is not tested on A/B_STAT (pin 48), and A/B_SEL (pin 49) due to internal pulldown resistor.

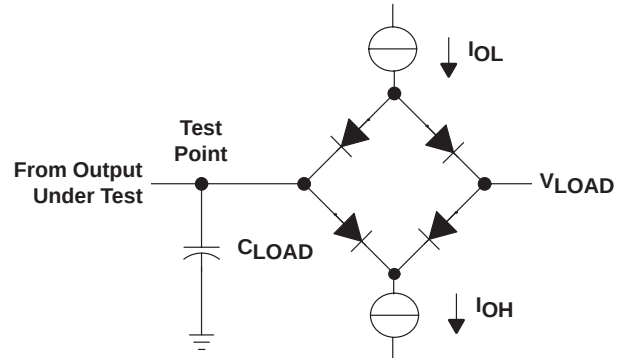
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT PARAMETERS

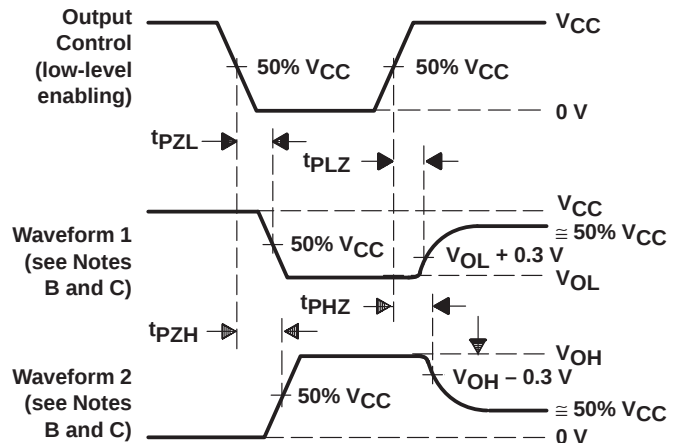
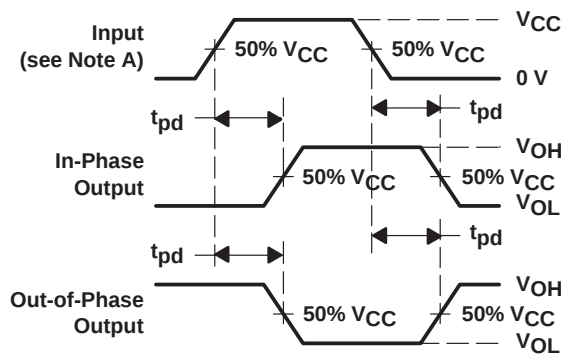
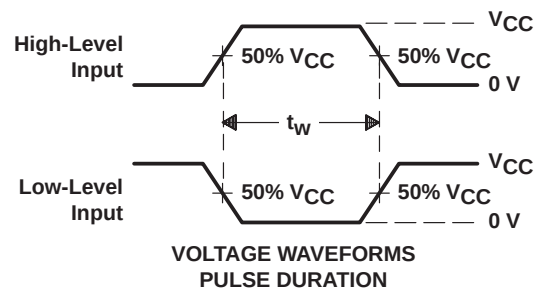
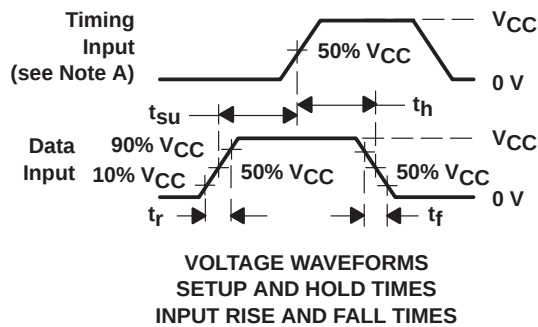
TIMING PARAMETER		$C_{LOAD}^{\dagger}$ (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	50	8	-8	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	50	8	-8	1.5
	t_{PLZ}				
t_{pd}		50	8	-8	‡

$^{\dagger} C_{LOAD}$ includes the typical load-circuit distributed capacitance

$^{\ddagger} \frac{V_{LOAD} - V_{OL}}{I_{OL}} = 50 \Omega$, where $V_{OL} = 0.6 V$, $I_{OL} = 8 mA$



LOAD CIRCUIT



- NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: $PRR = 1 MHz$, $Z_O = 50 \Omega$, $t_r = 6 ns$.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. For t_{PLZ} and t_{PHZ} , V_{OL} and V_{OH} are measured values.

Figure 3. Load Circuit and Voltage Waveforms

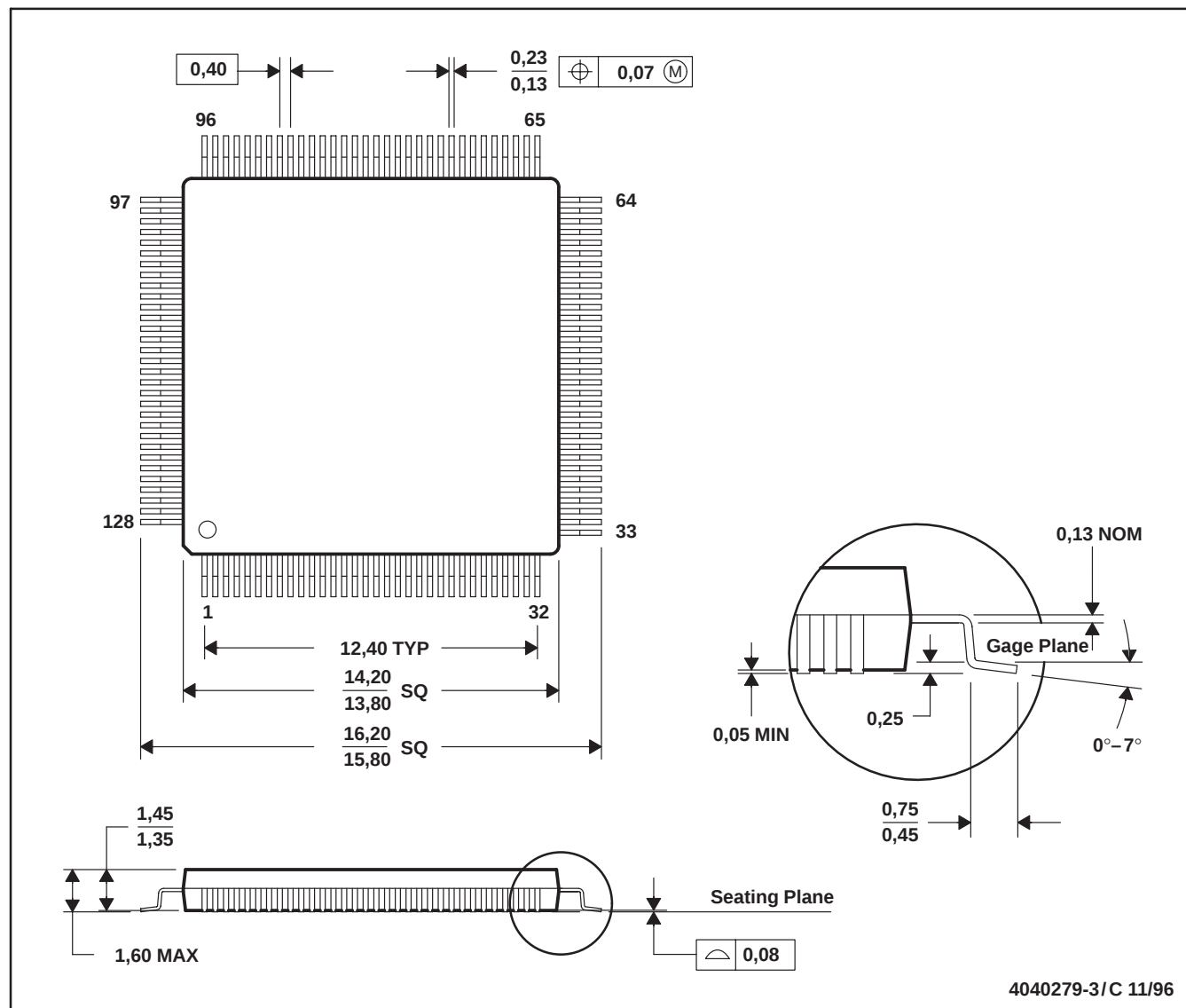
PCI930 3-TO-1 ZOOMED VIDEO SWITCH

SCPS018B – OCTOBER 1997 – REVISED DECEMBER 1997

MECHANICAL DATA

PBK (S-PQFP-G128)

PLASTIC QUAD FLATPACK



NOTES: D. All linear dimensions are in millimeters.
E. This drawing is subject to change without notice.
F. Falls within JEDEC MS-026

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