

NTHD4401P

Power MOSFET

-20 V, -3.0 A, Dual P-Channel, ChipFET™

Features

- Low $R_{DS(on)}$ and Fast Switching Speed in a ChipFET Package
- Leadless ChipFET Package 40% Smaller Footprint than TSOP-6
- ChipFET Package with Excellent Thermal Capabilities where Heat Transfer is Required
- Pb-Free Package is Available

Applications

- Charge Control in Battery Chargers
- Optimized for Battery and Load Management Applications in Portable Equipment
- MP3 Players, Cell Phones, Digital Cameras, PDAs
- Buck and Boost DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	−20	V
Gate-to-Source Voltage			V _{GS}	± 12	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	−2.1	A
		T _A = 85°C		−1.5	
	t ≤ 5 s	T _A = 25°C		−3.0	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.1	W
		T _A = 85°C		0.6	
	t ≤ 5 s	T _A = 25°C		2.1	
Pulsed Drain Current	tp = 10 μs		I _{DM}	−9.0	A
Operating Junction and Storage Temperature			T _J , T _{stg}	−55 to 150	°C
Source Current (Body Diode)			I _S	−2.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

THERMAL RESISTANCE RATINGS

Rating	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	110	$^\circ\text{C/W}$
Junction-to-Ambient - $t \leq 5 \text{ s}$		60	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

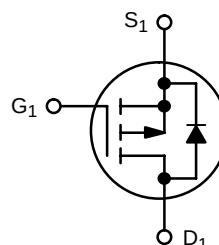
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



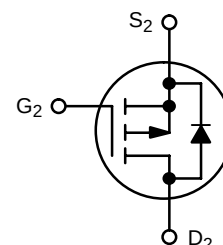
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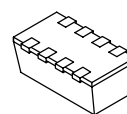
$V_{(BR)DS}$	$R_{DS(on)}$ TYP	I_D MAX
-20 V	130 m Ω @ -4.5 V	-3.0 A
	200 m Ω @ -2.5 V	



P-Channel MOSFET

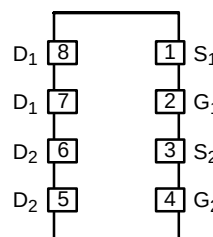


P-Channel MOSFET

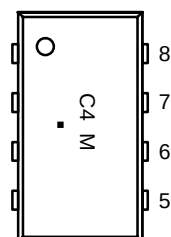


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



C4 = Specific Device Code

M = Month Code

■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD4401PT1	ChipFET	3000/Tape & Reel
NTHD4401PT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD4401P

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(Br)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20	-23		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(Br)DSS}/T_J$			-8.0		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 85^\circ\text{C}$		-5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.6	-0.75	-1.2	V
Gate Threshold Temperature Coefficient	$V_{GS(th)}/T_J$			2.65		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -2.1\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -1.7\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -1.0\text{ A}$		0.130 0.200 0.34	0.155 0.240	Ω
Forward Transconductance	g_{FS}	$V_{DS} = -10\text{ V}, I_D = -2.1\text{ A}$		5.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = -10\text{ V}$		185	300	pF
Output Capacitance	C_{oss}			95	150	
Reverse Transfer Capacitance	C_{rss}			30	50	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V},$ $I_D = -2.1\text{ A}$		3.0	6.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.2		
Gate-to-Source Charge	Q_{GS}			0.5		
Gate-to-Drain Charge	Q_{GD}			0.9		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -16\text{ V},$ $I_D = -2.1\text{ A}, R_G = 2.5\text{ }\Omega$		7.0	12	ns
Rise Time	t_r			13	25	
Turn-Off Delay Time	$t_{d(off)}$			33	50	
Fall Time	t_f			27	40	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}$ $I_S = -2.5\text{ A}$		-0.85	-1.15	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, dI_S/dt = 90\text{ A}/\mu\text{s},$ $I_S = -2.1\text{ A}$		32		ns
Charge Time	t_a			10		
Discharge Time	t_b			22		
Reverse Recovery Charge	Q_{RR}			15		nC

- Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

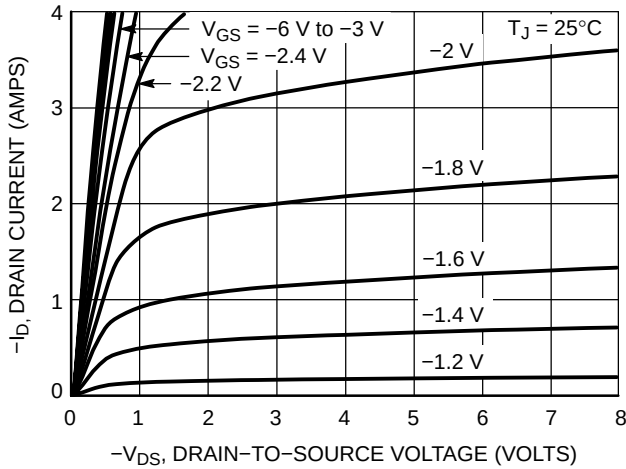


Figure 1. On-Region Characteristics

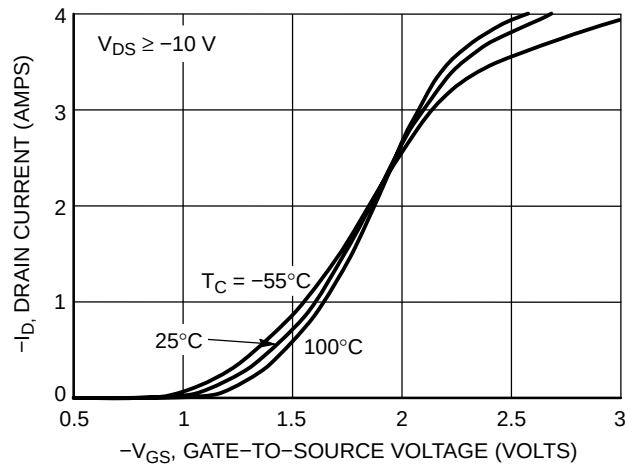


Figure 2. Transfer Characteristics

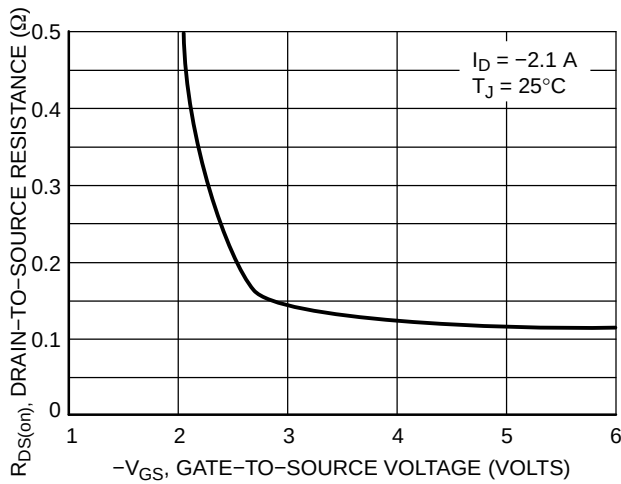


Figure 3. On-Resistance vs. Gate-to-Source Voltage

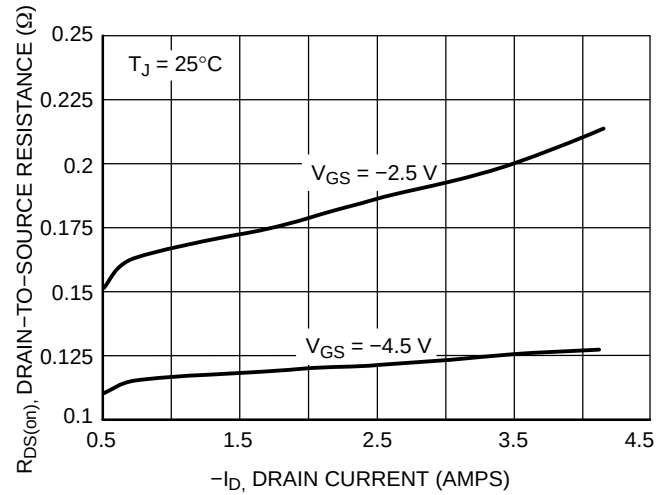


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

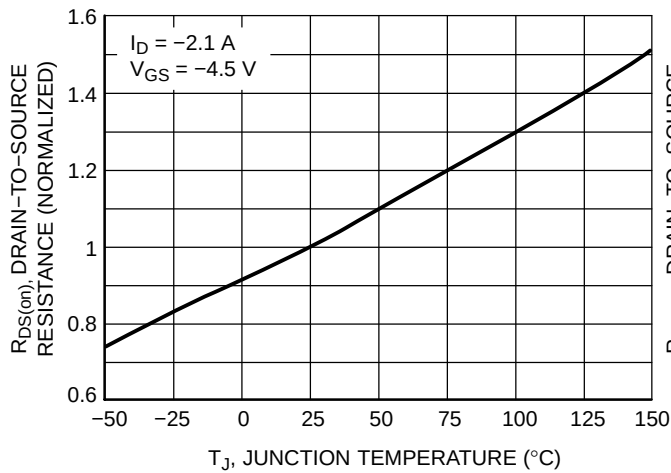


Figure 5. On-Resistance Variation with Temperature

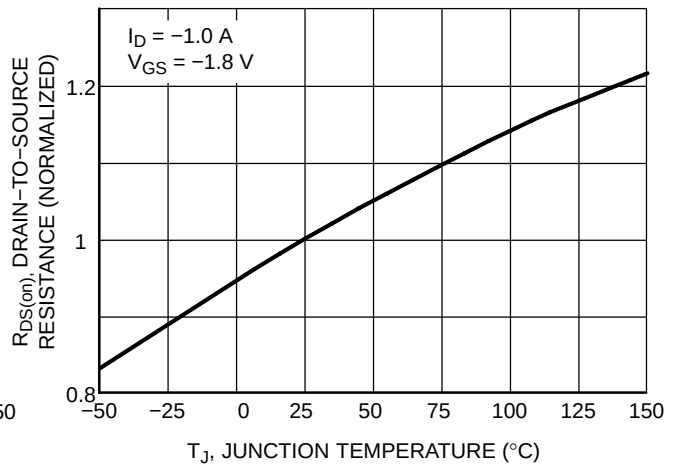


Figure 6. On-Resistance Variation with Temperature

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

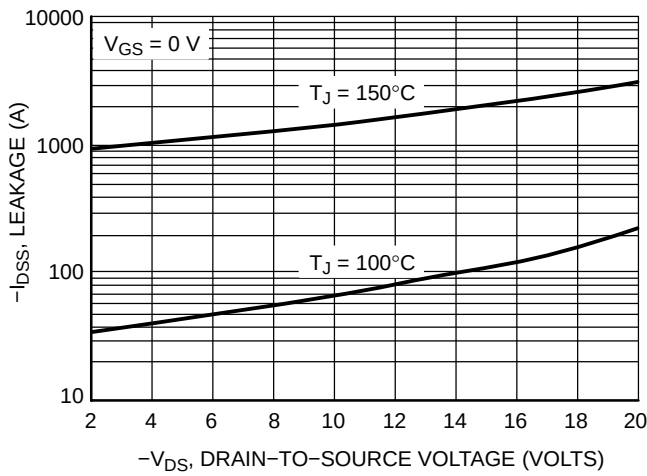


Figure 7. Drain-to-Source Leakage Current vs. Voltage

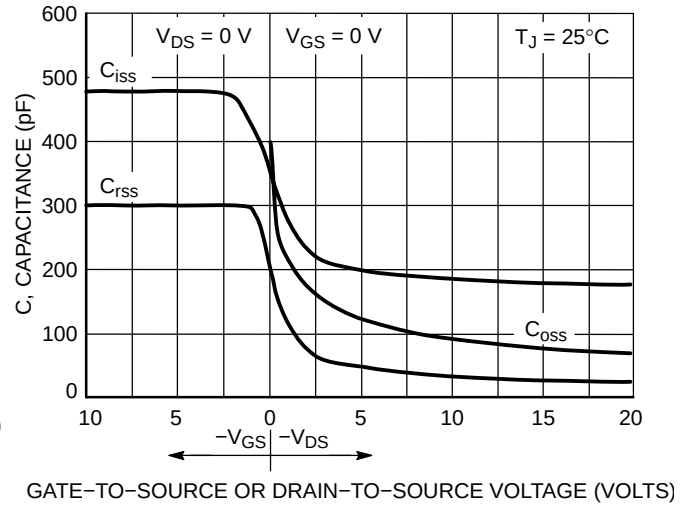


Figure 8. Capacitance Variation

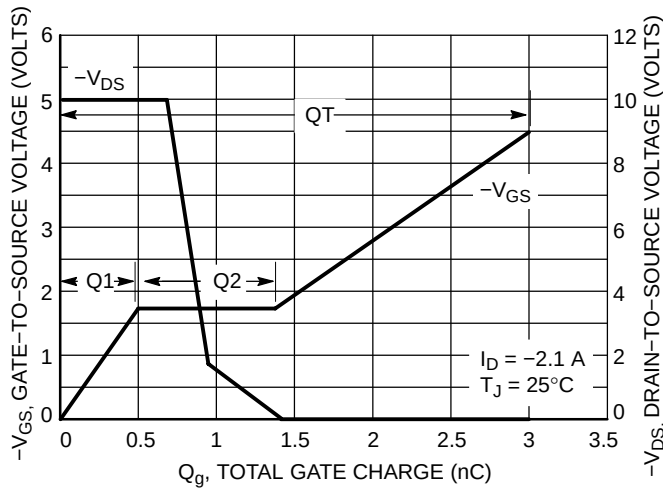


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

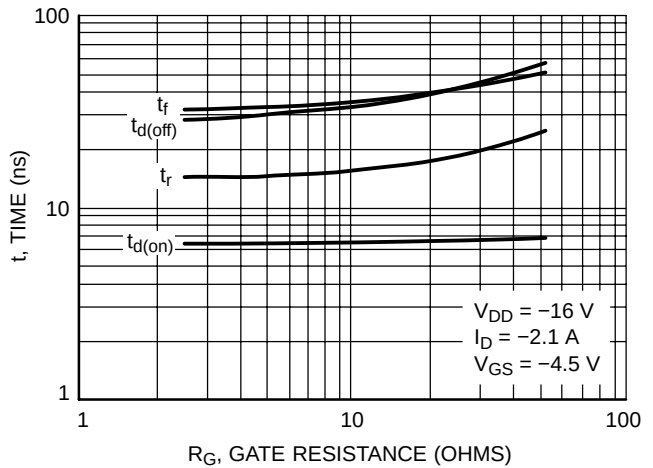


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

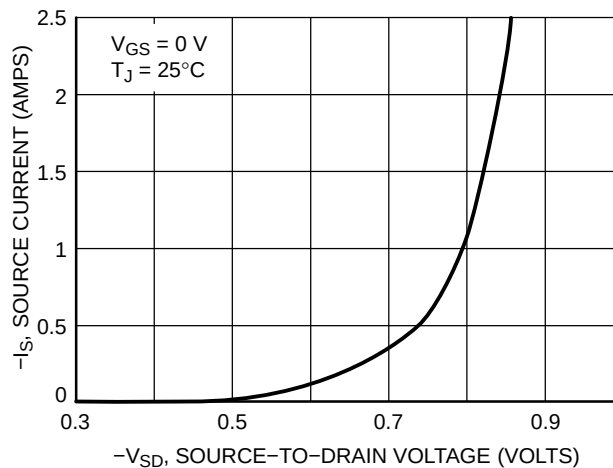


Figure 11. Diode Forward Voltage vs. Current

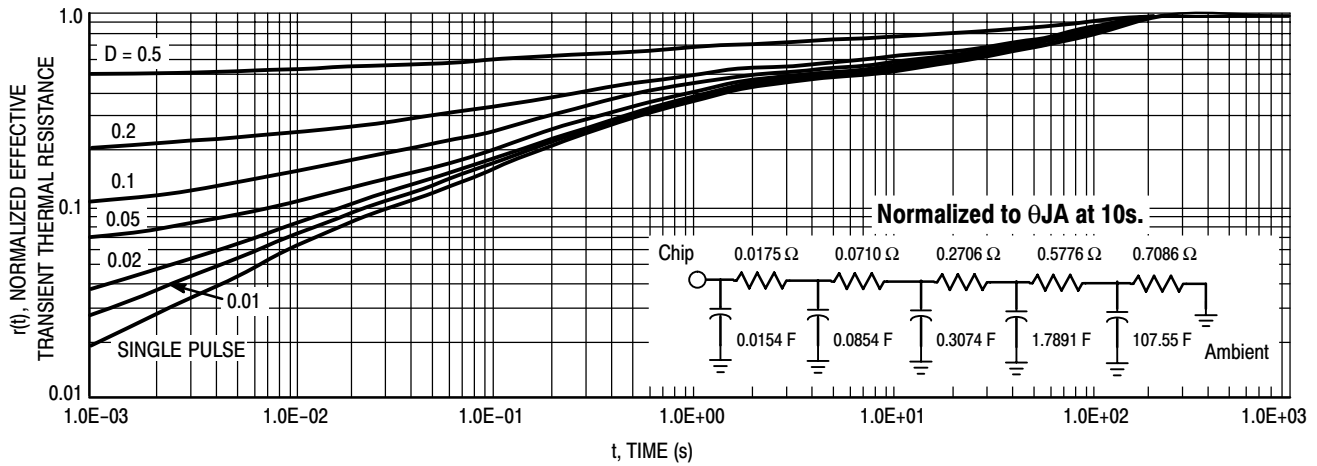


Figure 12. Thermal Response

SOLDERING FOOTPRINT*

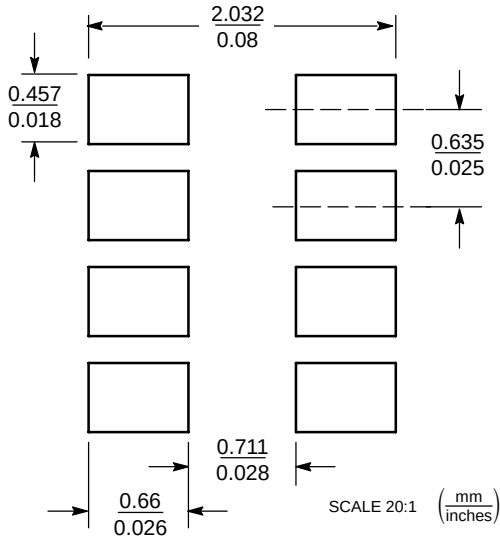


Figure 13. Basic

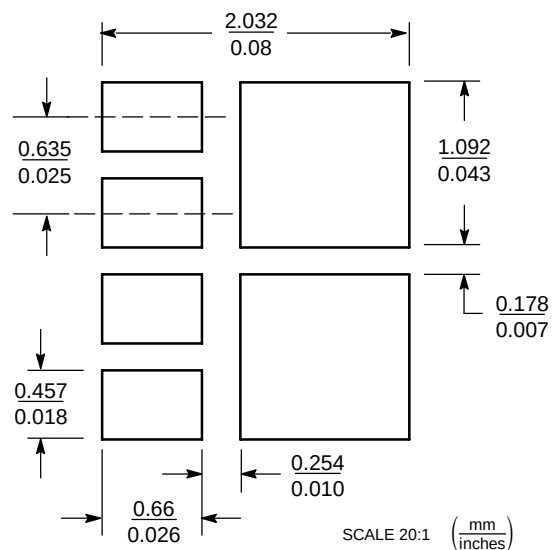


Figure 14. Style 2

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 13. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

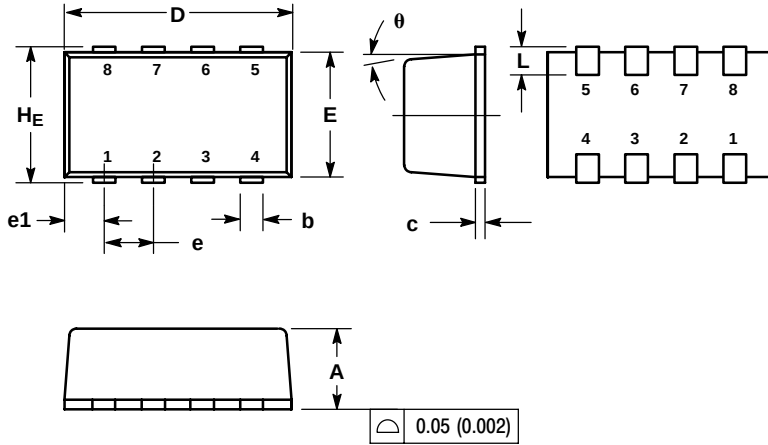
The minimum recommended pad pattern shown in Figure 14 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

NTHD4401P

PACKAGE DIMENSIONS

ChipFET™
CASE 1206A-03
ISSUE G



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
theta	5° NOM			5° NOM		

STYLE 2:

- PIN 1. SOURCE 1
- GATE 1
- SOURCE 2
- GATE 2
- DRAIN 2
- DRAIN 2
- DRAIN 1
- DRAIN 1

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